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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-2fgg484i

Figure 1-2 • Axcelerator Family Interconnect Elements

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

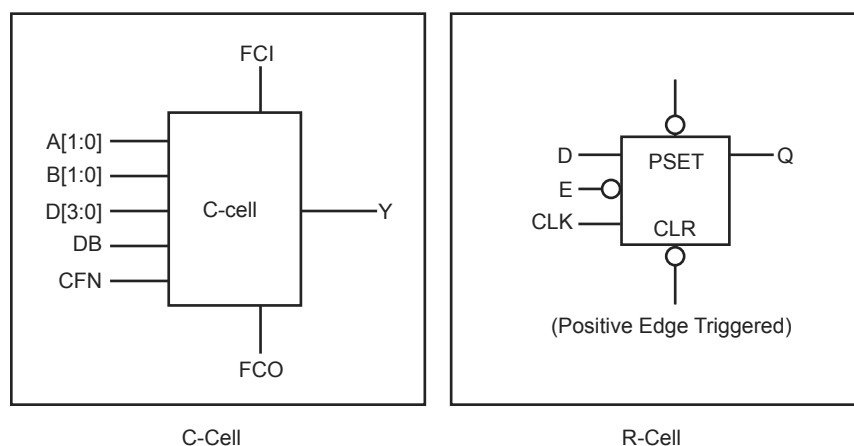


Figure 1-3 • AX C-Cell and R-Cell

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

$$P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po}$$

C_{load} = the output load (technology dependent)
 V_{CCI} = the output voltage (technology dependent)
 po = the number of outputs
 F_{po} = the average output frequency

$$P_{\text{memory}} = P_{11} * N_{\text{block}} * FR_{\text{CLK}} + P_{12} * N_{\text{block}} * FW_{\text{CLK}}$$

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
 F_{RCLK} = the read-clock frequency of the memory
 F_{WCLK} = the write-clock frequency of the memory

$$P_{\text{PLL}} = P_{13} * F_{\text{CLK}}$$

F_{RefCLK} = the clock frequency of the clock input of the PLL
 F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
 F_s = 100 MHz
 s = 1080

$$\Rightarrow P_{\text{HCLK}} = (P_1 + P_2 * s + P_3 * \text{sqrt}[s]) * F_s = 79 \text{ mW}$$

and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{R-cells}} = P_7 * ms * F_s = 173 \text{ mW}$$

mc = 1 (1 C-cell in this shift-register)
and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{C-cells}} = P_8 * mc * F_s = 0.14 \text{ mW}$$

$F_{pi} \sim 0 \text{ MHz}$

and $pi = 1$ (1 reset input => this is why $F_{pi} = 0$)

$$\Rightarrow P_{\text{inputs}} = P_9 * pi * F_{pi} = 0 \text{ mW}$$

$F_{po} = 50 \text{ MHz}$

and $po = 1$

$$\Rightarrow P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po} = 27.10 \text{ mW}$$

No RAM/FIFO in this shift-register

$$\Rightarrow P_{\text{memory}} = 0 \text{ mW}$$

No PLL in this shift-register

$$\Rightarrow P_{\text{PLL}} = 0 \text{ mW}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}} = 276 \text{ mW}$$

$$P_{\text{dc}} = 7.5\text{mA} * 1.5\text{V} = 11.25 \text{ mW}$$

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}} = 11.25 \text{ mW} + 276\text{mW} = 290.30 \text{ mW}$$

Table 2-8 • I/O Standards Supported by the Axcelerator Family

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVC MOS 2.5 V	2.5	N/A	N/A
LVC MOS 1.8 V	1.8	N/A	N/A
LVC MOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Note: *2.5 V GTL+ is not supported across the full military temperature range.

Table 2-9 • Supply Voltages

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5 V	1.5 V	3.3 V	1.5 V
1.5 V	1.8 V	3.3 V	1.8 V
1.5 V	2.5 V	3.3 V	2.5 V
1.5 V	3.3 V	3.3 V	3.3 V

Table 2-10 • I/O Features Comparison

I/O Assignment	Clamp Diode	Hot Insertion	5 V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes ¹	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes ^{1, 2}	Enabled/Disabled	
LVC MOS 2.5 V	No	Yes	No	Enabled/Disabled	
LVC MOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVC MOS 1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled ³
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled ⁴

Notes:

1. Can be implemented with an IDT bus switch.
2. Can be implemented with an external resistor.
3. The OE input of the output buffer must be deasserted permanently (handled by software).
4. The OE input of the output buffer must be asserted permanently (handled by software).

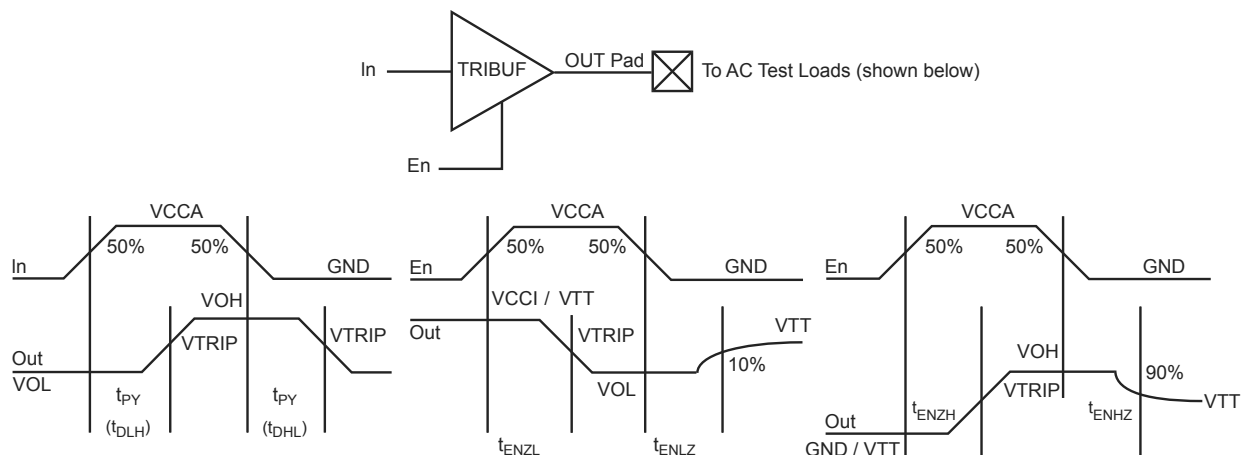


Figure 2-10 • Output Buffer Delays

3.3 V LVTTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-20 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.8	2.0	3.6	0.4	2.4	24	-24

AC Loadings

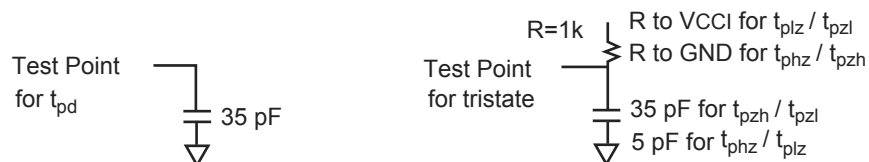


Figure 2-15 • AC Test Loads

Table 2-21 • AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	3.0	1.40	N/A	35

Note: * Measuring Point = VTRIP

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength =3 (16 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		11.03		12.56		14.77	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		11.42		13.01		15.29	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		11.04		12.58		14.79	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.86		1.88		1.88	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.50		2.51		2.52	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-36 • 3.3 V PCI-X I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI-X Output Module Timing								
t _{DP}	Input Buffer	1.57		1.79		2.10		ns
t _{PY}	Output Buffer	2.10		2.40		2.82		ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low	1.61		1.62		1.63		ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High	1.59		1.60		1.61		ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z	2.65		3.02		3.55		ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z	3.11		3.55		4.17		ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register	0.67		0.77		0.90		ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Models and Waveforms

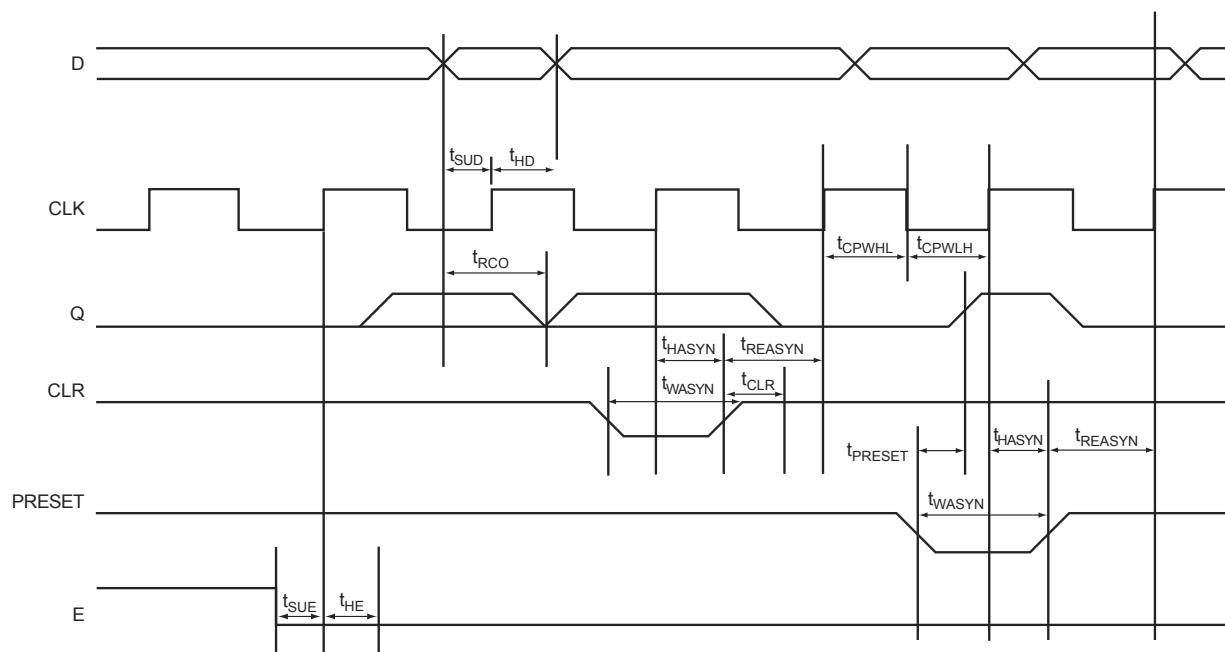


Figure 2-32 • R-Cell Delays

Timing Characteristics

Table 2-63 • R-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
R-Cell Propagation Delays								
t _{RCO}	Sequential Clock-to-Q		0.67		0.77		0.90	ns
t _{CLR}	Asynchronous Clear-to-Q		0.67		0.77		0.90	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.36		0.36		0.36	ns
t _{SUD}	Flip-Flop Data Input Set-Up		0.34		0.34		0.34	ns
t _{SUE}	Flip-Flop Enable Input Set-Up		0.00		0.00		0.00	ns
t _{HD}	Flip-Flop Data Input Hold		0.67		0.77		0.90	ns
t _{HE}	Flip-Flop Enable Input Hold		0.67		0.77		0.90	ns
t _{WASYN}	Asynchronous Pulse Width	0.48		0.48		0.48		ns
t _{REASYN}	Asynchronous Recovery Time		0.23		0.27		0.31	ns
t _{HASYN}	Asynchronous Removal Time		0.36		0.36		0.36	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.36		0.36		0.36		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.36		0.36		0.36		ns

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-70 • AX125 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-71 • AX250 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t _{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Implementation Example:

Figure 2-47 shows a complex clock distribution example. The reference clock (RefCLK) of PLLE is being sourced from non-clock signal pins (INBUF to PLLINT). The CLK1 output of PLLE is being fed to the RefCLK input of PLLF. The CLK2 output of PLLE is driving logic (via PLLOUT). In turn, this logic is driving the global resource CLKE. PLLF is driving both CLKF and CLKG global resources.

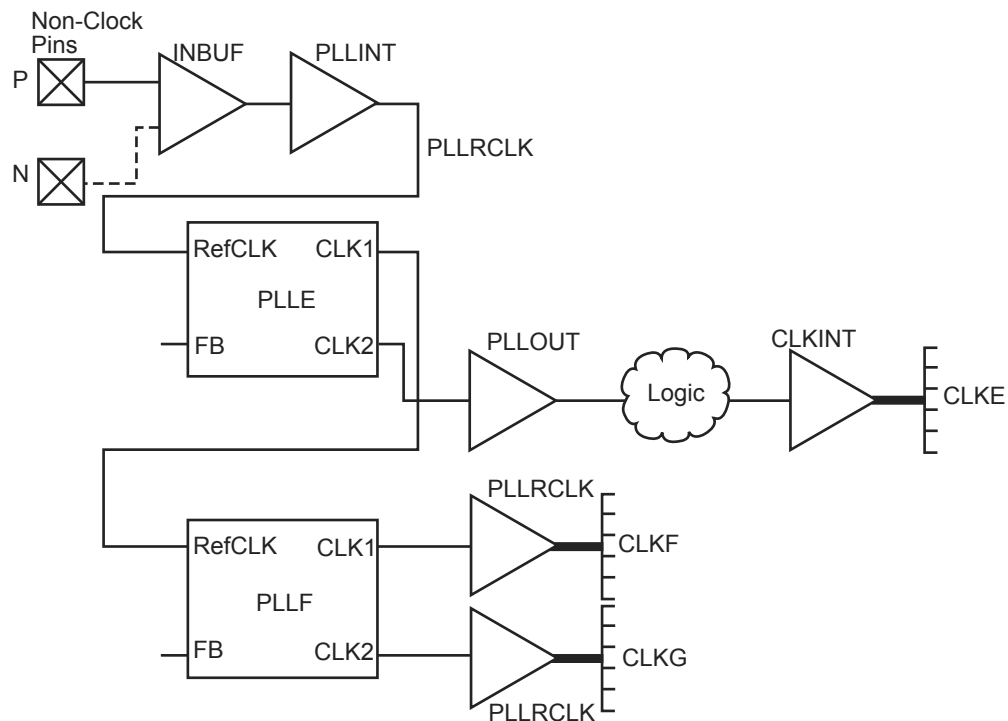


Figure 2-47 • Complex Clock Distribution Example

Table 2-98 • One FIFO Block

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

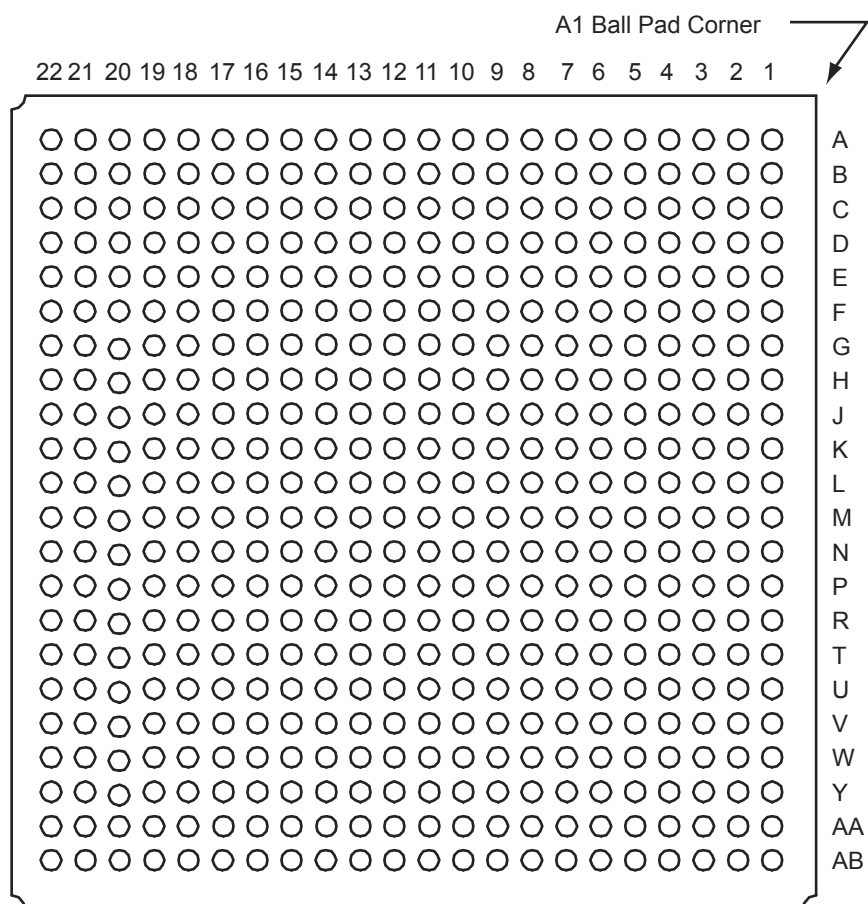
		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		11.40		12.98		15.26	ns
t _{WHD}	Write Hold		0.22		0.25		0.30	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		0.88		0.88		0.88	ns
t _{WCKP}	Minimum WCLK Period	1.63		1.63		1.63		ns
t _{RSU}	Read Setup		11.63		13.25		15.58	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.77		0.77		0.77	ns
t _{RCKL}	RCLK Low		0.93		0.93		0.93	ns
t _{RCKP}	Minimum RCLK period	1.70		1.70		1.70		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		1.32		1.51		1.77	ns
t _{RCK2RD2}	RCLK-To-OUT (Non-Pipelined)		2.16		2.46		2.90	ns

Note: Timing data for this single block FIFO has a depth of 4,096. For all other combinations, use Microsemi's timing software.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0					
IO00NB0F0	E6	IO18NB0F1	C10	IO36NB1F3	H15
IO00PB0F0	F6	IO18PB0F1	C9	IO36PB1F3	G15
IO01NB0F0	G8	IO19NB0F1	E11	IO37NB1F3	C17
IO01PB0F0	G7	IO19PB0F1	F11	IO37PB1F3	C16
IO02NB0F0	D7	IO20NB0F1	G12	IO38NB1F3	B18
IO02PB0F0	E7	IO20PB0F1	H12	IO38PB1F3	B17
IO03NB0F0	D5	IO21NB0F1	D11	IO39NB1F3	A18
IO03PB0F0	E5	IO21PB0F1	D10	IO39PB1F3	A17
IO04NB0F0	G9	IO22NB0F2	A10	IO40NB1F3	H16
IO04PB0F0	H9	IO22PB0F2	A9	IO40PB1F3	G16
IO05NB0F0	E8	IO23NB0F2	B11	IO41NB1F4	B19
IO05PB0F0	F8	IO23PB0F2	B10	IO41PB1F4	A19
IO06NB0F0	C6	IO24NB0F2	G13	IO42NB1F4	C19
IO06PB0F0	D6	IO24PB0F2	H13	IO42PB1F4	C18
IO07NB0F0	B5	IO25NB0F2	C12	IO43NB1F4	D18
IO07PB0F0	C5	IO25PB0F2	C11	IO43PB1F4	D17
IO08NB0F0	A6	IO26NB0F2	E12	IO44NB1F4	H17
IO08PB0F0	A5	IO26PB0F2	D12	IO44PB1F4	G17
IO09NB0F0	E9	IO27NB0F2	E13	IO45NB1F4	F17
IO09PB0F0	F9	IO27PB0F2	F13	IO45PB1F4	E17
IO10NB0F0	G10	IO28NB0F2	G14	IO46NB1F4	B20
IO10PB0F0	H10	IO28PB0F2	H14	IO46PB1F4	A20
IO11NB0F0	B7	IO29NB0F2	A12	IO47NB1F4	C21
IO11PB0F0	B6	IO29PB0F2	B12	IO47PB1F4	C20
IO12NB0F1	C8	IO30NB0F2/HCLKAN	C13	IO48NB1F4	H18
IO12PB0F1	C7	IO30PB0F2/HCLKAP	D13	IO48PB1F4	G18
IO13NB0F1	E10	IO31NB0F2/HCLKBN	F14	IO49NB1F4	F18
IO13PB0F1	F10	IO31PB0F2/HCLKBP	E14	IO49PB1F4	E18
IO14NB0F1	G11	Bank 1		IO50NB1F4	D20
IO14PB0F1	H11	IO32NB1F3/HCLKCN	C14	IO50PB1F4	D19
IO15NB0F1	D9	IO32PB1F3/HCLKCP	B14	IO51NB1F4	A22
IO15PB0F1	D8	IO33NB1F3/HCLKDN	D16	IO51PB1F4	A21
IO16NB0F1	A8	IO33PB1F3/HCLKDP	D15	IO52NB1F4	B22
IO16PB0F1	A7	IO34NB1F3	B16	IO52PB1F4	B21
IO17NB0F1	B9	IO34PB1F3	A16	IO53NB1F4	F19
IO17PB0F1	B8	IO35NB1F3	E15	IO53PB1F4	E19
		IO35PB1F3	F15	IO54NB1F5	F20

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	B27	GND	R11	VCCA	K11
GND	B3	GND	R12	VCCA	K17
GND	C1	GND	R13	VCCA	K18
GND	C2	GND	R14	VCCA	L10
GND	C25	GND	R15	VCCA	L18
GND	C26	GND	R16	VCCA	U10
GND	C27	GND	R17	VCCA	U18
GND	C3	GND	T11	VCCA	V10
GND	E27	GND	T12	VCCA	V11
GND	L11	GND	T13	VCCA	V17
GND	L12	GND	T14	VCCA	V18
GND	L13	GND	T15	VCCPLA	A13
GND	L14	GND	T16	VCCPLB	J13
GND	L15	GND	T17	VCCPLC	B15
GND	L16	GND	U11	VCCPLD	C15
GND	L17	GND	U12	VCCPLE	AG14
GND	M11	GND	U13	VCCPLF	AF14
GND	M12	GND	U14	VCCPLG	AB13
GND	M13	GND	U15	VCCPLH	AG13
GND	M14	GND	U16	VCCDA	A11
GND	M15	GND	U17	VCCDA	AB12
GND	M16	GND/LP	J8	VCCDA	AC12
GND	M17	NC	U3	VCCDA	AC25
GND	N11	PRA	J14	VCCDA	AD16
GND	N12	PRB	D14	VCCDA	AD17
GND	N13	PRC	V14	VCCDA	E16
GND	N14	PRD	AB14	VCCDA	E2
GND	N15	TCK	E4	VCCDA	E24
GND	N16	TDI	D4	VCCDA	F12
GND	N17	TDO	J9	VCCDA	F16
GND	P11	TMS	H8	VCCDA	F7
GND	P12	TRST	E3	VCCDA	K14
GND	P13	VCCA	AA21	VCCDA	P10
GND	P14	VCCA	AD5	VCCDA	P18
GND	P15	VCCA	E1	VCCDA	W14
GND	P16	VCCA	G22	VCCDA	W9
GND	P17	VCCA	K10	VCCIB0	A4

FG484



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG484	
AX500 Function	Pin Number
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
Bank 6	
IO126NB6F12	V2
IO126PB6F12	W2

FG484	
AX500 Function	Pin Number
IO127NB6F12	P7
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7

FG484	
AX500 Function	Pin Number
IO146NB6F13	M3
IO146PB6F13	N3
Bank 7	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3

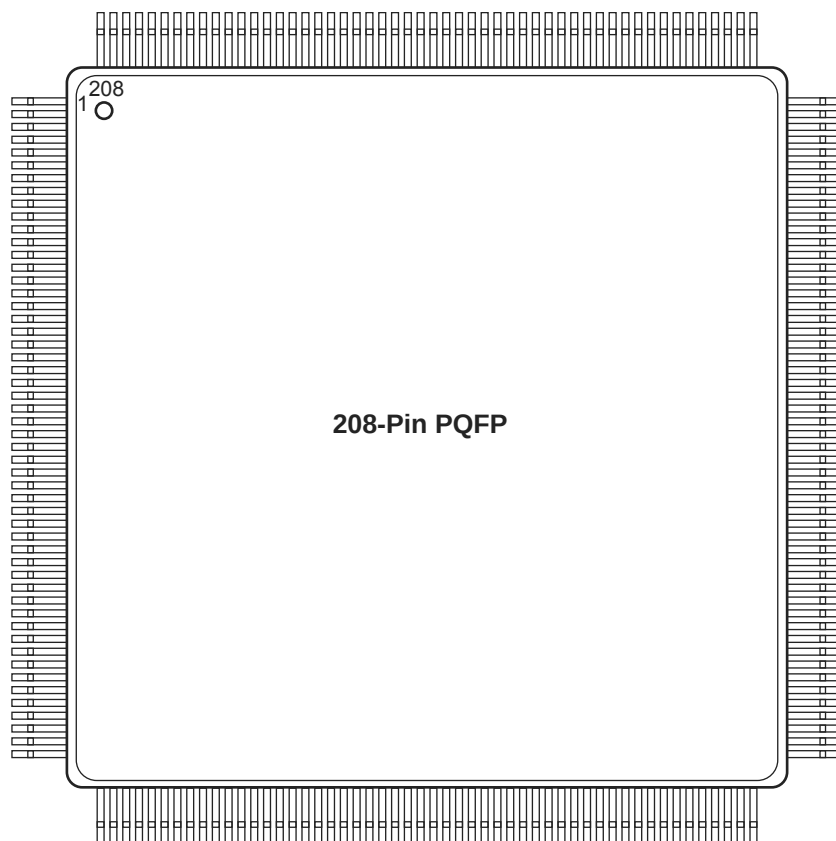
FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO153PB7F14	M6	GND	A8	GND	L11
IO154NB7F14	K2	GND	AC23	GND	L12
IO154PB7F14	L2	GND	AC4	GND	L13
IO155NB7F14	K3	GND	AD24	GND	L14
IO155PB7F14	L3	GND	AD3	GND	L15
IO156NB7F14	L5	GND	AE2	GND	L16
IO156PB7F14	L4	GND	AE25	GND	L17
IO157NB7F14	L6	GND	AF1	GND	M10
IO157PB7F14	L7	GND	AF13	GND	M11
IO158NB7F15	J1	GND	AF14	GND	M12
IO158PB7F15	K1	GND	AF19	GND	M13
IO159NB7F15	J4	GND	AF26	GND	M14
IO159PB7F15	K4	GND	AF8	GND	M15
IO160NB7F15	H2	GND	B2	GND	M16
IO160PB7F15	J2	GND	B25	GND	M17
IO161NB7F15	K6	GND	B26	GND	N1
IO161PB7F15	K5	GND	C24	GND	N10
IO162NB7F15	H3	GND	C3	GND	N11
IO162PB7F15	J3	GND	G20	GND	N12
IO163NB7F15	G2	GND	G7	GND	N13
IO163PB7F15	G1	GND	H1	GND	N14
IO164NB7F15	G4	GND	H19	GND	N15
IO164PB7F15	H4	GND	H26	GND	N16
IO165NB7F15	F3	GND	H8	GND	N17
IO165PB7F15	G3	GND	J18	GND	N26
IO166NB7F15	E2	GND	J9	GND	P1
IO166PB7F15	F2	GND	K10	GND	P10
IO167NB7F15	F5	GND	K11	GND	P11
IO167PB7F15	G5	GND	K12	GND	P12
Dedicated I/O		GND	K13	GND	P13
GND	A1	GND	K14	GND	P14
GND	A13	GND	K15	GND	P15
GND	A14	GND	K16	GND	P16
GND	A19	GND	K17	GND	P17
GND	A26	GND	L10	GND	P26

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO51PB1F4	E21	IO68PB2F6	K24	IO86NB2F8	N28
IO52NB1F4	F22	IO69NB2F6	F27	IO86PB2F8	N27
IO52PB1F4	E22	IO69PB2F6	E27	IO87NB2F8	P29
IO53NB1F4	B25	IO70NB2F6	J26	IO87PB2F8	P30
IO53PB1F4	B24	IO70PB2F6	J25	IO88NB2F8	P25
IO54NB1F5	D24	IO71NB2F6	H27	IO88PB2F8	P24
IO54PB1F5	D23	IO71PB2F6	G27	IO89NB2F8	P28
IO55NB1F5	F23	IO72NB2F6	J28	IO89PB2F8	P27
IO55PB1F5	E23	IO72PB2F6	H28	IO90NB2F8	P22
IO56NB1F5	H21	IO73NB2F6	G28	IO90PB2F8	P23
IO56PB1F5	G21	IO73PB2F6	F28	IO91NB2F8	R26
IO57NB1F5	D25	IO74NB2F7	L23	IO91PB2F8	P26
IO57PB1F5	C25	IO74PB2F7	L24	IO92NB2F8	R24
IO58NB1F5	F24	IO75NB2F7	L26	IO92PB2F8	R25
IO58PB1F5	E24	IO75PB2F7	K26	IO93NB2F8	R29
IO59NB1F5	D26	IO76NB2F7	M25	IO93PB2F8	R30
IO59PB1F5	C26	IO76PB2F7	L25	IO94NB2F8	R22
IO60NB1F5	G23	IO77NB2F7	K27	IO94PB2F8	R23
IO60PB1F5	G22	IO77PB2F7	J27	IO95NB2F8	T27
IO61NB1F5	B27	IO78NB2F7	M27	IO95PB2F8	R27
IO61PB1F5	A27	IO78PB2F7	L27	Bank 3	
IO62NB1F5	F25	IO79NB2F7	K30	IO96NB3F9	T29
IO62PB1F5	E25	IO79PB2F7	K29	IO96PB3F9	T30
IO63NB1F5	H23	IO80NB2F7	M23	IO97NB3F9	U29
IO63PB1F5	H22	IO80PB2F7	M24	IO97PB3F9	U30
Bank 2		IO81NB2F7	M28	IO98NB3F9	T22
IO64NB2F6	K23	IO81PB2F7	L28	IO98PB3F9	T23
IO64PB2F6	J23	IO82NB2F7	N26	IO99NB3F9	U26
IO65NB2F6	J24	IO82PB2F7	M26	IO99PB3F9	T26
IO65PB2F6	H24	IO83NB2F7	N25	IO100NB3F9	U24
IO66NB2F6	H26	IO83PB2F7	N24	IO100PB3F9	T24
IO66PB2F6	H25	IO84NB2F7	N22	IO101NB3F9	V28
IO67NB2F6	G26	IO84PB2F7	N23	IO101PB3F9	U28
IO67PB2F6	G25	IO85NB2F8	M29	IO102NB3F9	U23
IO68NB2F6	K25	IO85PB2F8	L29	IO102PB3F9	U22

PQ208



Note

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CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
VCCA	U17	VCCIB2	D23	VCCIB7	E4
VCCA	U9	VCCIB2	E22	VCCIB7	K9
VCCA	Y4	VCCIB2	K17	VCCIB7	L9
VCCDA	A12	VCCIB2	L17	VCCIB7	M10
VCCDA	AA13	VCCIB2	M16	VCCPLA	E12
VCCDA	AA15	VCCIB3	AA22	VCCPLB	J12
VCCDA	AA7	VCCIB3	AB23	VCCPLC	E14
VCCDA	AC11	VCCIB3	AC24	VCCPLD	H14
VCCDA	AD11	VCCIB3	AC25	VCCPLE	Y14
VCCDA	AE17	VCCIB3	P16	VCCPLF	U14
VCCDA	B15	VCCIB3	R17	VCCPLG	Y12
VCCDA	C15	VCCIB3	T17	VCCPLH	U12
VCCDA	C6	VCCIB4	AB21	VCOMPLA	F12
VCCDA	D13	VCCIB4	AC22	VCOMPLB	H12
VCCDA	E13	VCCIB4	AD23	VCOMPLC	F14
VCCDA	E19	VCCIB4	AE23	VCOMPLD	J14
VCCDA	G5	VCCIB4	T14	VCOMPLE	AA14
VCCDA	N21	VCCIB4	U15	VCOMPLF	V14
VCCDA	N5	VCCIB4	U16	VCOMPLG	AA12
VCCDA	W21	VCCIB5	AB5	VCOMPLH	V12
VCCIB0	A3	VCCIB5	AC4	VPUMP	E20
VCCIB0	B3	VCCIB5	AD3		
VCCIB0	C4	VCCIB5	AE3		
VCCIB0	D5	VCCIB5	T12		
VCCIB0	J10	VCCIB5	U10		
VCCIB0	J11	VCCIB5	U11		
VCCIB0	K12	VCCIB6	AA4		
VCCIB1	A23	VCCIB6	AB3		
VCCIB1	B23	VCCIB6	AC1		
VCCIB1	C22	VCCIB6	AC2		
VCCIB1	D21	VCCIB6	P10		
VCCIB1	J15	VCCIB6	R9		
VCCIB1	J16	VCCIB6	T9		
VCCIB1	K14	VCCIB7	C1		
VCCIB2	C24	VCCIB7	C2		
VCCIB2	C25	VCCIB7	D3		