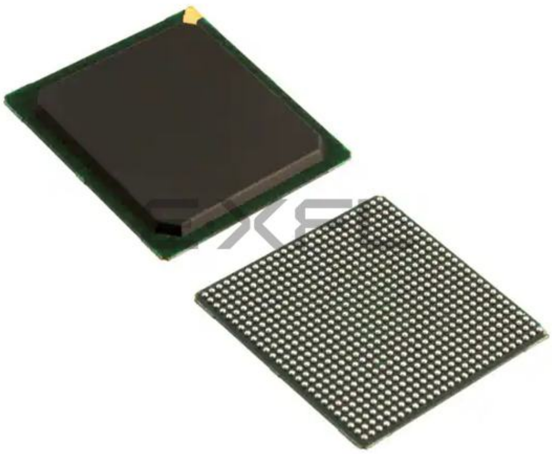

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	418
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-2fgg676

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The maximum power dissipation allowed for Military temperature and Mil-Std 883B devices is specified as a function of θ_{jc}.

Table 2-6 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0m/s	θ_{ja} 2.5m/s	Units
Chip Scale Package (CSP)	180	N/A	57.8	51.0	50	°C/W
Plastic Quad Flat Pack (PQFP)	208	8.0	26	23.5	20.9	°C/W
Plastic Ball Grid Array (PBGA)	729	2.2	13.7	10.6	9.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.0	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	324	3.0	25.8	22.1	20.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	208	2.0	22	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA)[2]	624	6.5	8.9	8.5	8	°C/W

Notes:

1. *θ_{jc} for the 208-pin and 352-pin CQFP refers to the thermal resistance between the junction and the bottom of the package.*
2. *θ_{jc} for the 624-pin CCGA refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board (θ_{jb}) for CCGA 624 package is 3.4°C/W.*

Timing Characteristics

Axcelerator devices are manufactured in a CMOS process, therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-7 should be applied to all timing data contained within this datasheet.

Table 2-7 • **Temperature and Voltage Timing Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, VCCA = 1.425V)**

VCCA	Junction Temperature						
	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
1.4 V	0.83	0.86	0.91	0.96	1.02	1.05	1.15
1.425 V	0.82	0.84	0.90	0.94	1.00	1.04	1.13
1.5 V	0.78	0.80	0.85	0.89	0.95	0.98	1.07
1.575 V	0.74	0.76	0.81	0.85	0.90	0.94	1.02
1.6 V	0.73	0.75	0.80	0.84	0.89	0.92	1.01

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 175°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4V and 1.6V.*

All timing numbers listed in this datasheet represent sample timing characteristics of Axcelerator devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Microsemi's Designer software after place-and-route.

Timing Characteristics

Table 2-22 • 3.3 V LVTTL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 1 (8 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		14.28		16.27		19.13	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		15.25		17.37		20.42	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		14.26		16.24		19.09	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.56		1.57		1.58	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		1.95		1.96		1.97	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		039		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-22 **• 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		12.14		13.83		16.26	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

PLLRCLK and PLLHCLK

PLLRCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 2-44).

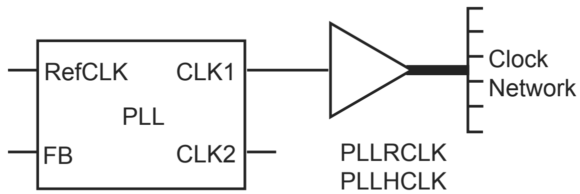


***Figure 2-44* • PLLRCLK and PLLHCLK**

Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc. (Figure 2-45).

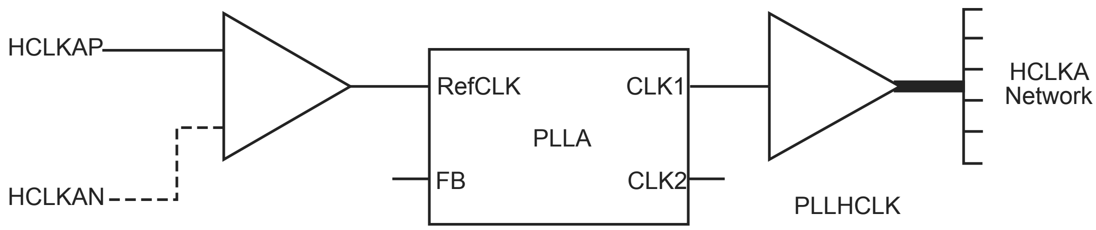


***Figure 2-45* • Example of HCLKA Driven from a PLL with External Clock Source**

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 2-46).

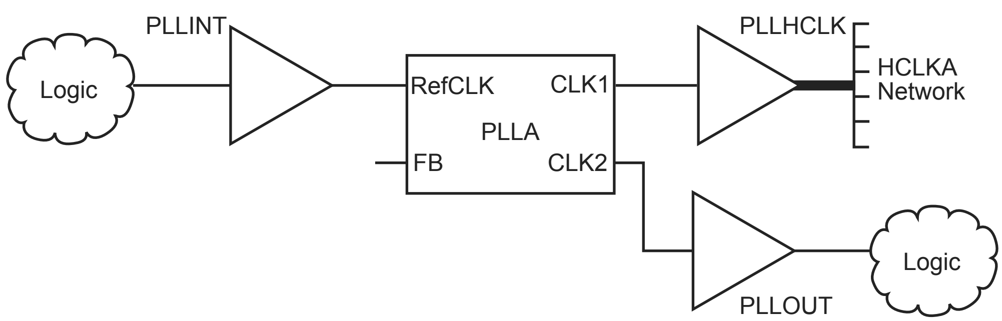


***Figure 2-46* • Example of PLLINT and PLLOUT Usage**

Axcelerator Clock Management System

Introduction

Each member of the Axcelerator family[6] contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20µs

Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 µF and 10 µF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

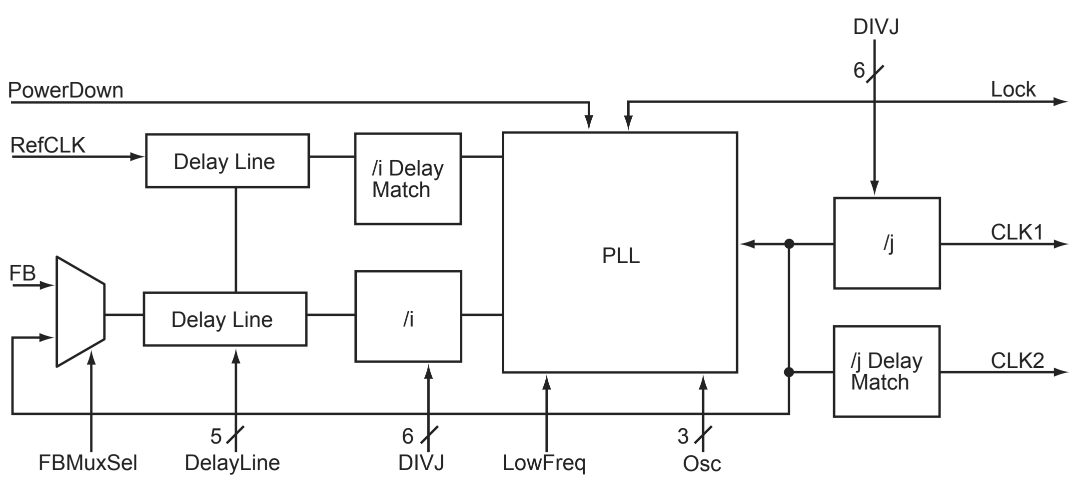


Figure 2-48 • **PLL Block Diagram**

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

6. *AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.*

PLL Configurations

The following rules apply to the different PLL inputs and outputs:

Reference Clock

The RefCLK can be driven by (Figure 2-50):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. CLK1 output of an adjacent PLL
3. [H]CLKxP (single-ended or voltage-referenced)
4. [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Feedback Clock

The feedback clock can be driven by (Figure 2-51 on page 2-78):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
3. An internal signal from the PLL block

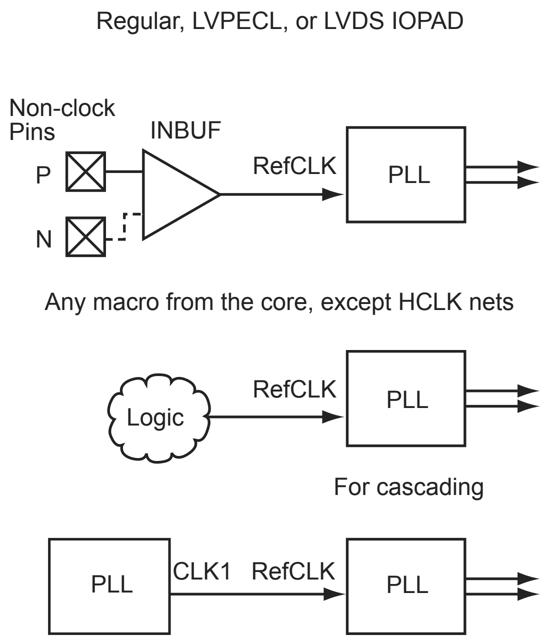


***Figure 2-50* • Reference Clock Connections**

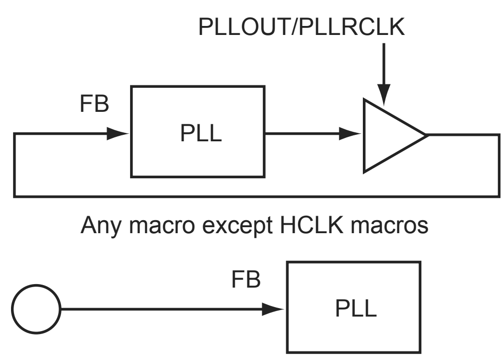


***Figure 2-51* • Feedback Clock Connections**

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

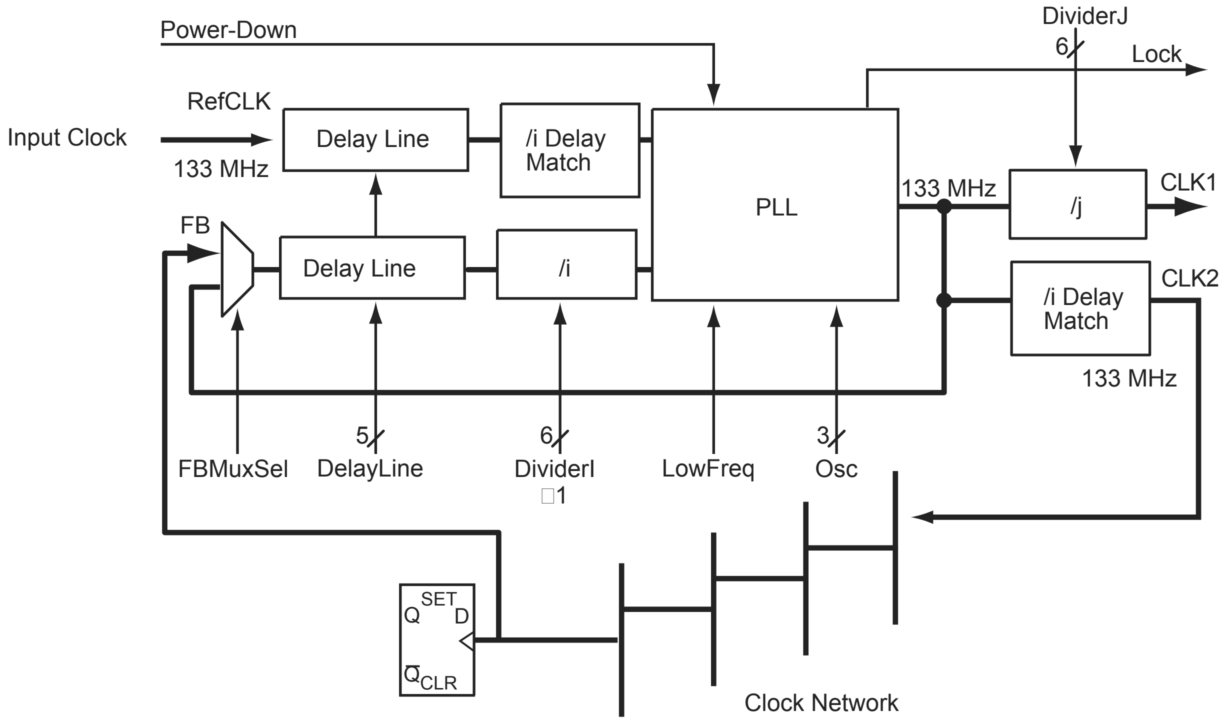


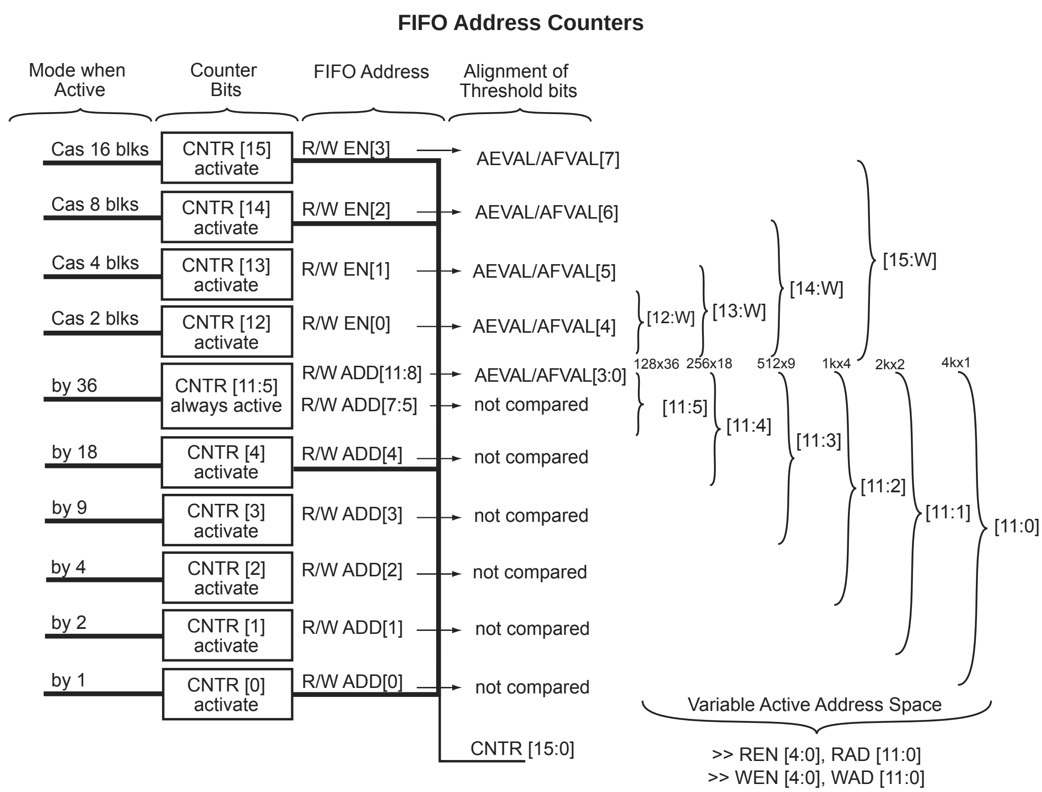
Figure 2-56 • **Using the PLL for Clock Deskewing**

FIFO Flag Logic

The FIFO is user configurable into various DEPTHs and WIDTHs. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.



Note: Inactive counter bits are set to zero.

Figure 2-62 • **FIFO Address Counters**

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

Table 2-94 **• FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

Figure 2-63 illustrates flag generation.

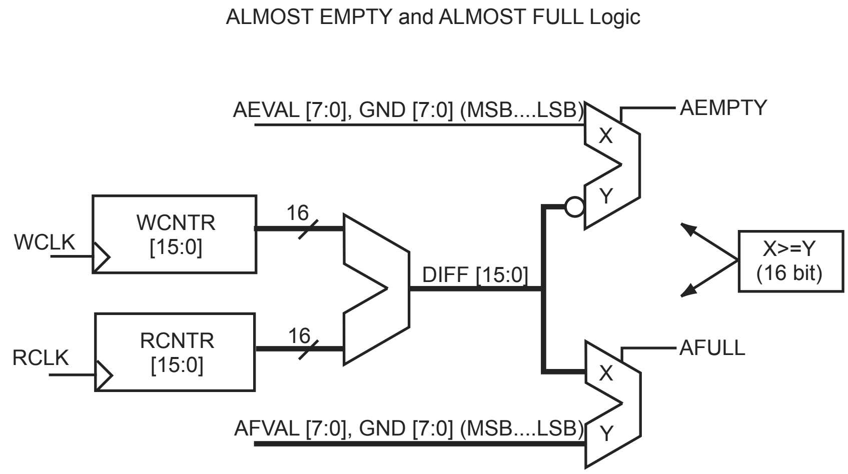


***Figure 2-63* • ALMOST-EMPTY and ALMOST-FULL Logic**

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-95).

***Table 2-95* • Number of Available Configuration Bits**

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-100.

FG324	
AX125 Function	Pin Number
GND	R4
GND	T16
GND	T3
GND	U17
GND	U2
GND	V1
GND	V18
GND/LP	E5
NC	A10
NC	A11
NC	A12
NC	A13
NC	A8
NC	A9
NC	B12
NC	F15
NC	F4
NC	G15
NC	G4
NC	H14
NC	H15
NC	H5
NC	J1
NC	J14
NC	J15
NC	J5
NC	K14
NC	K15
NC	K5
NC	L14
NC	L15
NC	L5
NC	M4
NC	M5
NC	N17

FG324	
AX125 Function	Pin Number
NC	N4
NC	N5
NC	R12
NC	R13
NC	R6
NC	R7
NC	T12
NC	T6
NC	U16
NC	V17
PRA	E9
PRB	D9
PRC	P10
PRD	R10
TCK	E6
TDI	D7
TDO	D5
TMS	D4
TRST	D6
VCCA	E15
VCCA	G10
VCCA	G11
VCCA	G5
VCCA	G8
VCCA	G9
VCCA	H12
VCCA	H7
VCCA	J12
VCCA	J7
VCCA	K12
VCCA	K7
VCCA	L12
VCCA	L7
VCCA	M10
VCCA	M11

FG324	
AX125 Function	Pin Number
VCCA	M8
VCCA	M9
VCCA	P4
VCCA	R15
VCCPLA	D8
VCCPLB	E7
VCCPLC	B11
VCCPLD	E11
VCCPLE	R11
VCCPLF	P12
VCCPLG	U8
VCCPLH	P8
VCCDA	B3
VCCDA	D14
VCCDA	E10
VCCDA	J2
VCCDA	K16
VCCDA	P15
VCCDA	P9
VCCDA	R5
VCCIB0	F7
VCCIB0	F8
VCCIB0	F9
VCCIB1	F10
VCCIB1	F11
VCCIB1	F12
VCCIB2	G13
VCCIB2	H13
VCCIB2	J13
VCCIB3	K13
VCCIB3	L13
VCCIB3	M13
VCCIB4	N10
VCCIB4	N11
VCCIB4	N12

FG484	
AX1000 Function	Pin Number
Bank 0	
IO01NB0F0	E3
IO01PB0F0	D3
IO02NB0F0	E7
IO02PB0F0	E6
IO05NB0F0	D2
IO05PB0F0	E2
IO06NB0F0	C5
IO06PB0F0	C4
IO12NB0F1	D7
IO12PB0F1	D6
IO13NB0F1	B5
IO13PB0F1	B4
IO14NB0F1	E9
IO14PB0F1	E8
IO15NB0F1	C7
IO15PB0F1	C6
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	B7
IO17PB0F1	B6
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	C9
IO19PB0F1	C8
IO20NB0F1	D9
IO20PB0F1	D8
IO21NB0F1	B9
IO21PB0F1	B8
IO22NB0F2	A9
IO22PB0F2	A8
IO23NB0F2	B10
IO23PB0F2	A10
IO26NB0F2	A14
IO26PB0F2	A13

FG484	
AX1000 Function	Pin Number
IO29NB0F2	B12
IO29PB0F2	B11
IO30NB0F2/HCLKAN	E11
IO30PB0F2/HCLKAP	E10
IO31NB0F2/HCLKBN	D12
IO31PB0F2/HCLKBP	D11
Bank 1	
IO32NB1F3/HCLKCN	F13
IO32PB1F3/HCLKCP	F12
IO33NB1F3/HCLKDN	E14
IO33PB1F3/HCLKDP	E13
IO34NB1F3	C13
IO34PB1F3	C12
IO37NB1F3	B14
IO37PB1F3	B13
IO38NB1F3	A16
IO38PB1F3	A15
IO40NB1F3	C15
IO42NB1F4	A18
IO42PB1F4	A17
IO43NB1F4	B16
IO43PB1F4	B15
IO44NB1F4	B18
IO44PB1F4	B17
IO45NB1F4	B19
IO45PB1F4	A19
IO46NB1F4	C19
IO46PB1F4	C18
IO48NB1F4	F15
IO48PB1F4	F14
IO49NB1F4	D16
IO49PB1F4	D15
IO50NB1F4	C17
IO50PB1F4	C16
IO51NB1F4	E22

FG484	
AX1000 Function	Pin Number
IO51PB1F4	D22
IO52NB1F4	E16
IO52PB1F4	E15
IO57NB1F5	E21
IO57PB1F5	D21
IO60NB1F5	G16
IO60PB1F5	G15
IO61NB1F5	D18
IO61PB1F5	E17
IO63NB1F5	E20
IO63PB1F5	D20
Bank 2	
IO64NB2F6	F18
IO64PB2F6	F17
IO67NB2F6	F19
IO67PB2F6	E19
IO68NB2F6	J16
IO68PB2F6	H16
IO70NB2F6	J17
IO70PB2F6	H17
IO74NB2F7	J18
IO74PB2F7	H18
IO75NB2F7	G20
IO75PB2F7	F20
IO79NB2F7	H19
IO79PB2F7	G19
IO80NB2F7	L16
IO80PB2F7	K16
IO84NB2F7	L17
IO84PB2F7	K17
IO85NB2F8	G21
IO85PB2F8	F21
IO86NB2F8	G22
IO86PB2F8	F22
IO87NB2F8	J20

FG676	
AX1000 Function	Pin Number
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11

FG676	
AX1000 Function	Pin Number
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11

FG676	
AX1000 Function	Pin Number
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG1152	
AX2000 Function	Pin Number
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H31
NC	H33
NC	J1
NC	J3
NC	J34
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17

FG1152	
AX2000 Function	Pin Number
PRB	F18
PRC	AD18
PRD	AH18
TCK	J9
TDI	F7
TDO	L10
TMS	H8
TRST	E6
VCCA	AA13
VCCA	AA22
VCCA	AB14
VCCA	AB15
VCCA	AB16
VCCA	AB17
VCCA	AB18
VCCA	AB19
VCCA	AB20
VCCA	AB21
VCCA	AF8
VCCA	AK28
VCCA	G30
VCCA	G5
VCCA	N14
VCCA	N15
VCCA	N16
VCCA	N17
VCCA	N18
VCCA	N19
VCCA	N20
VCCA	N21
VCCA	P13
VCCA	P22
VCCA	R13
VCCA	R22
VCCA	T13

FG1152	
AX2000 Function	Pin Number
VCCA	T22
VCCA	U13
VCCA	U22
VCCA	V13
VCCA	V22
VCCA	W13
VCCA	W22
VCCA	Y13
VCCA	Y22
VCCDA	AF26
VCCDA	AF9
VCCDA	AG17
VCCDA	AG18
VCCDA	AH14
VCCDA	AH15
VCCDA	AH17
VCCDA	AH20
VCCDA	AH21
VCCDA	AK29
VCCDA	AK6
VCCDA	E15
VCCDA	E29
VCCDA	E7
VCCDA	F15
VCCDA	F21
VCCDA	F5
VCCDA	G20
VCCDA	H17
VCCDA	H18
VCCDA	H28
VCCDA	J18
VCCDA	V27
VCCDA	V6
VCCIB0	A5
VCCIB0	B5

FG1152	
AX2000 Function	Pin Number
VCCIB0	C5
VCCIB0	D5
VCCIB0	L12
VCCIB0	L13
VCCIB0	L14
VCCIB0	M13
VCCIB0	M14
VCCIB0	M15
VCCIB0	M16
VCCIB0	M17
VCCIB1	A30
VCCIB1	B30
VCCIB1	C30
VCCIB1	D30
VCCIB1	L21
VCCIB1	L22
VCCIB1	L23
VCCIB1	M18
VCCIB1	M19
VCCIB1	M20
VCCIB1	M21
VCCIB1	M22
VCCIB2	E31
VCCIB2	E32
VCCIB2	E33
VCCIB2	E34
VCCIB2	M24
VCCIB2	N23
VCCIB2	N24
VCCIB2	P23
VCCIB2	P24
VCCIB2	R23
VCCIB2	T23
VCCIB2	U23
VCCIB3	AA23

FG1152	
AX2000 Function	Pin Number
VCCIB3	AA24
VCCIB3	AB23
VCCIB3	AB24
VCCIB3	AC24
VCCIB3	AK31
VCCIB3	AK32
VCCIB3	AK33
VCCIB3	AK34
VCCIB3	V23
VCCIB3	W23
VCCIB3	Y23
VCCIB4	AC18
VCCIB4	AC19
VCCIB4	AC20
VCCIB4	AC21
VCCIB4	AC22
VCCIB4	AD21
VCCIB4	AD22
VCCIB4	AD23
VCCIB4	AL30
VCCIB4	AM30
VCCIB4	AN30
VCCIB4	AP30
VCCIB5	AC13
VCCIB5	AC14
VCCIB5	AC15
VCCIB5	AC16
VCCIB5	AC17
VCCIB5	AD12
VCCIB5	AD13
VCCIB5	AD14
VCCIB5	AL5
VCCIB5	AM5
VCCIB5	AN5
VCCIB5	AP5

FG1152	
AX2000 Function	Pin Number
VCCIB6	AA11
VCCIB6	AA12
VCCIB6	AB11
VCCIB6	AB12
VCCIB6	AC11
VCCIB6	AK1
VCCIB6	AK2
VCCIB6	AK3
VCCIB6	AK4
VCCIB6	V12
VCCIB6	W12
VCCIB6	Y12
VCCIB7	E1
VCCIB7	E2
VCCIB7	E3
VCCIB7	E4
VCCIB7	M11
VCCIB7	N11
VCCIB7	N12
VCCIB7	P11
VCCIB7	P12
VCCIB7	R12
VCCIB7	T12
VCCIB7	U12
VCCPLA	J16
VCCPLB	K17
VCCPLC	J19
VCCPLD	L18
VCCPLE	AK19
VCCPLF	AE18
VCCPLG	AK16
VCCPLH	AF17
VCOMPLA	H16
VCOMPLB	L17
VCOMPLC	H19

FG1152	
AX2000 Function	**Pin Number**
VCOMPLD	K18
VCOMPLE	AH19
VCOMPLF	AF18
VCOMPLG	AH16
VCOMPLH	AD17
VPUMP	J26

CG624	
AX1000 Function	Pin Number
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5
GND/LP	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5
GND	V1
GND	V25
GND	V5
NC	A14
NC	AA20
NC	AB13
NC	AD4
NC	AE12
NC	F21
NC	G10
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
VCCA	AB20
VCCA	F22
VCCA	F4
VCCA	J17
VCCA	J9
VCCA	K10
VCCA	K11
VCCA	K15
VCCA	K16
VCCA	L10
VCCA	L16
VCCA	R10
VCCA	R16
VCCA	T10
VCCA	T11
VCCA	T15
VCCA	T16

CG624	
AX2000 Function	Pin Number
IO310NB7F29	N10
IO310PB7F29	N9
IO311NB7F29	K1
IO311PB7F29	L1
IO313NB7F29	M5
IO316NB7F29	L6
IO316PB7F29	L5
IO317NB7F29	K2
IO317PB7F29	L2
IO318NB7F29	K4
IO318PB7F29	L4
IO320NB7F29	J3
IO321NB7F30	J2
IO321PB7F30	J1
IO323NB7F30	L7
IO323PB7F30	M7
IO324NB7F30	M9
IO324PB7F30	M8
IO327NB7F30	F1
IO327PB7F30	G1
IO328NB7F30	K7
IO328PB7F30	K6
IO329NB7F30	D1
IO329PB7F30	E1
IO331PB7F30	G2
IO332NB7F31	H3
IO332PB7F31	H2
IO333NB7F31	E2
IO333PB7F31	F2
IO334NB7F31	H4
IO334PB7F31	J4
IO335NB7F31	H5

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO335PB7F31	H6
IO337NB7F31	D2
IO338NB7F31	J6
IO338PB7F31	J5
IO339NB7F31	F3
IO339PB7F31	E3
IO340NB7F31	G4*
IO340PB7F31	G3*
IO341NB7F31	K8
IO341PB7F31	L8
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5
GND	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

Revision	Changes	Page
Revision 12 (v2.4)	Revised ordering information and timing data to reflect phase out of –3 speed grade options.	
	Table 2-3 was updated.	2
Revision 11 (v2.3)	The "Packaging Data" section is new.	iv
	Table 2-2 was updated.	2-1
	"VCCDA Supply Voltage" was updated.	2-9
	"PRA/B/C/D Probe A, B, C and D" was updated.	2-10
	The "User I/Os" was updated.	2-11
Revision 10 (v2.2)	Figure 1-3 was updated.	1-2
	Table 2-2 was updated.	2-1
	The "Power-Up/Down Sequence" section was updated.	2-1
	Table 2-4 was updated.	2-3
	Table 2-5 was updated.	2-4
	The "Timing Characteristics" section was added.	2-7
	Table 2-7 was updated.	2-7
	Figure 2-1 was updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) equations in the "Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) in the "Routed Clock – Using LVTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The "Global Pins" section was updated.	2-10
	The "User I/Os" section was updated.	2-11
	Table 2-17 was updated.	2-19
	Figure 2-8 was updated.	2-20
	Figure 2-13 and Figure 2-14 were updated.	2-24
	The following timing parameters were renamed in I/O timing characteristic tables from Table 2-22 to Table 2-60: t_{IOCLKQ} > t_{ICLKQ} t_{IOCLKY} > t_{OCLKQ}	2-26 to 2-52
	Timing numbers were updated from Table 2-22 to Table 2-78.	2-26 to 2-69
	The "R-Cell" section was updated.	2-58
	Figure 2-59 was updated.	2-89
	Figure 2-60 was updated.	2-89
	Figure 2-67 was updated.	2-100
	Figure 2-68 was updated.	2-101
	Table 2-89 to Table 2-93 were updated.	2-90 to 2-94
	Table 2-98 to Table 2-102 were updated.	2-102 to 2-106