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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax1000-2fgg896

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

Table 2-8 • **I/O Standards Supported by the Axcelerator Family**

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVCMOS 2.5 V	2.5	N/A	N/A
LVCMOS 1.8 V	1.8	N/A	N/A
LVCMOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

*Note: *2.5 V GTL+ is not supported across the full military temperature range.*

Table 2-9 • **Supply Voltages**

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5 V	1.5 V	3.3 V	1.5 V
1.5 V	1.8 V	3.3 V	1.8 V
1.5 V	2.5 V	3.3 V	2.5 V
1.5 V	3.3 V	3.3 V	3.3 V

Table 2-10 • **I/O Features Comparison**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1, 2]	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled[3]
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled[4]

Notes:

1. *Can be implemented with an IDT bus switch.*
2. *Can be implemented with an external resistor.*
3. *The OE input of the output buffer must be deasserted permanently (handled by software).*
4. *The OE input of the output buffer must be asserted permanently (handled by software).*

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		12.14		13.83		16.26	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		3.30		3.76		4.42	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.74		4.26		5.00	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.06		3.49		4.10	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.29		2.30		2.31	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Class II

Table 2-47 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min,. V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	15.2	-15.2

AC Loadings

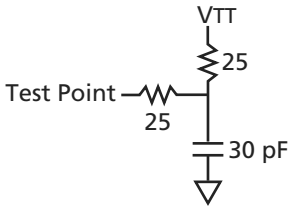


Figure 2-22 • AC Test Loads

Table 2-48 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
VREF – 0.75	VREF + 0.75	VREF	1.25	30

*Note: * Measuring Point = V_{trip}*

Timing Characteristics

Table 2-49 • 2.5 V SSTL2 Class II I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V SSTL2 Class II I/O Module Timing								
t_{DP}	Input Buffer		1.89		2.16		2.53	ns
t_{PY}	Output Buffer		2.39		2.72		3.20	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-75 • **AX125 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-76 • **AX250 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t_{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

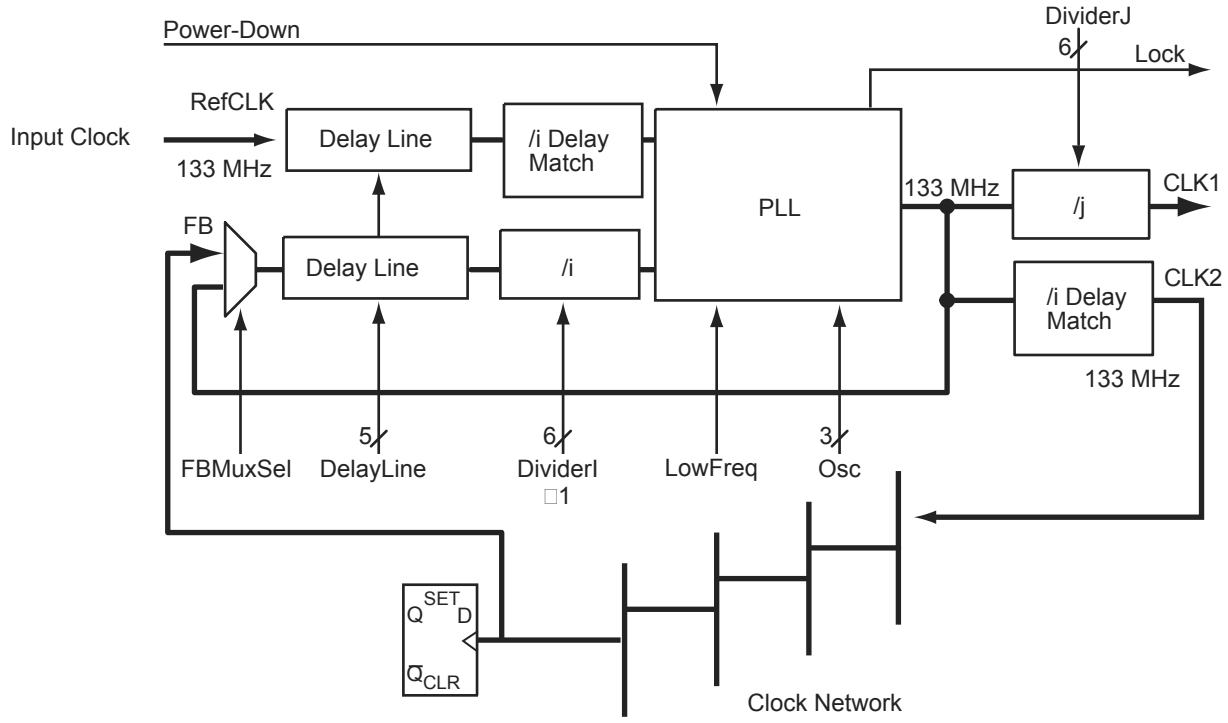


Figure 2-56 • **Using the PLL for Clock Deskewing**

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111". If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:

   The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microsemi identity, part number, and version number in a specific JTAG format.

2. USERCODE:

   The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.

3. Boundary-Scan Register (BSR):

   Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.

4. Bypass Register (BYR):

   This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

Special Fuses

Security

Microsemi antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden

FG256-Pin FBGA	
AX125 Function	**Pin Number**
VCCA	L10
VCCA	L7
VCCA	L8
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A2
VCCDA	C13
VCCDA	D9
V_{CCDA}	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10

FG256-Pin FBGA	
AX125 Function	**Pin Number**
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

FG256	
AX250 Function	**Pin Number**
Bank 6	
IO91NB6F6	L4
IO91PB6F6	M4
IO92NB6F6	L3
IO92PB6F6	M3
IO94NB6F6	P2
IO94PB6F6	N2
IO97NB6F6	J4
IO97PB6F6	K4
IO98NB6F6	N1
IO98PB6F6	P1
IO100NB6F6	L2
IO100PB6F6	M2
IO102NB6F6	L1
IO102PB6F6	M1
IO103NB6F6	J3
IO103PB6F6	K3
IO104NB6F6	J2
IO104PB6F6	K2
Bank 7	
IO107NB7F7	J1
IO107PB7F7	K1
IO108NB7F7	G2
IO108PB7F7	H2
IO111NB7F7	G3
IO111PB7F7	H3
IO112NB7F7	E1
IO112PB7F7	F1
IO113NB7F7	G1
IO114NB7F7	E2
IO114PB7F7	F2
IO115NB7F7	G4
IO115PB7F7	H4
IO116NB7F7	C1
IO116PB7F7	D1

FG256	
AX250 Function	**Pin Number**
IO117NB7F7	C2
IO117PB7F7	B1
IO118NB7F7	D2
IO118PB7F7	D3
IO119NB7F7	E3
IO119PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6

FG256	
AX250 Function	**Pin Number**
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6
VCCA	L10
VCCA	L7
VCCA	L8

FG256	
AX250 Function	**Pin Number**
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A11
VCCDA	A2
VCCDA	C13
VCCDA	D9
VCCDA	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCDA	R11
VCCDA	R5
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10

FG256	
AX250 Function	**Pin Number**
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

FG484	
AX250 Function	**Pin Number**
NC	A19
NC	A4
NC	A5
NC	AA11
NC	AA12
NC	AA18
NC	AA19
NC	AA4
NC	AB16
NC	AB17
NC	AB4
NC	AB7
NC	AB8
NC	B11
NC	B12
NC	B17
NC	B18
NC	B19
NC	B4
NC	B5
NC	C10
NC	C11
NC	C14
NC	C15
NC	C18
NC	C19
NC	D1
NC	D2
NC	D21
NC	D3
NC	E1
NC	E2
NC	E21
NC	E3
NC	F22
NC	F3

FG484	
AX250 Function	**Pin Number**
NC	G22
NC	G3
NC	H3
NC	J3
NC	K21
NC	K22
NC	N22
NC	P22
NC	R19
NC	R22
NC	T1
NC	T22
NC	U1
NC	U2
NC	U21
NC	U22
NC	V1
NC	V2
NC	V21
NC	V22
NC	V3
NC	W1
NC	W2
NC	W21
NC	W22
NC	W3
NC	Y10
NC	Y11
NC	Y12
NC	Y13
NC	Y15
NC	Y16
NC	Y17
NC	Y18
NC	Y8
NC	Y9

FG484	
AX250 Function	**Pin Number**
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10

FG484	
AX500 Function	Pin Number
IO54PB2F5	H22
IO55NB2F5	L17
IO55PB2F5	K17
IO56NB2F5	K21
IO56PB2F5	K22
IO58NB2F5	L20
IO58PB2F5	K20
IO59NB2F5	L18
IO59PB2F5	K18
IO60NB2F5	M21
IO60PB2F5	L21
IO61NB2F5	L16
IO61PB2F5	K16
IO62NB2F5	M19
IO62PB2F5	L19
Bank 3	
IO63NB3F6	N16
IO63PB3F6	M16
IO64NB3F6	P22
IO64PB3F6	N22
IO65NB3F6	N20
IO65PB3F6	M20
IO66NB3F6	P21
IO66PB3F6	N21
IO67NB3F6	N18
IO67PB3F6	N19
IO68NB3F6	T22
IO68PB3F6	R22
IO69NB3F6	N17
IO69PB3F6	M17
IO70NB3F6	T21
IO70PB3F6	R21
IO71NB3F6	P18
IO71PB3F6	P19
IO72NB3F6	R20

FG484	
AX500 Function	Pin Number
IO72PB3F6	P20
IO73PB3F6	R19
IO74NB3F7	V21
IO74PB3F7	U21
IO75NB3F7	V22
IO75PB3F7	U22
IO76NB3F7	U20
IO76PB3F7	T20
IO77NB3F7	R17
IO77PB3F7	P17
IO78NB3F7	W21
IO78PB3F7	W22
IO79NB3F7	T18
IO79PB3F7	R18
IO80NB3F7	W20
IO80PB3F7	V20
IO81NB3F7	U19
IO81PB3F7	T19
IO82NB3F7	U18
IO82PB3F7	V19
IO83NB3F7	R16
IO83PB3F7	P16
Bank 4	
IO84NB4F8	AB18
IO84PB4F8	AB19
IO85NB4F8	T15
IO85PB4F8	T16
IO86NB4F8	AA18
IO86PB4F8	AA19
IO87NB4F8	W17
IO87PB4F8	V17
IO88NB4F8	Y19
IO88PB4F8	W18
IO89NB4F8	U14
IO89PB4F8	U15

FG484	
AX500 Function	Pin Number
IO90NB4F8	Y17
IO90PB4F8	Y18
IO91NB4F8	V15
IO91PB4F8	V16
IO92PB4F8	AB17
IO93NB4F8	Y15
IO93PB4F8	Y16
IO94NB4F9	AA16
IO94PB4F9	AA17
IO95NB4F9	AB14
IO95PB4F9	AB15
IO96NB4F9	W15
IO96PB4F9	W16
IO97NB4F9	AA13
IO97PB4F9	AB13
IO98NB4F9	AA14
IO98PB4F9	AA15
IO100NB4F9	Y14
IO100PB4F9	W14
IO101NB4F9	Y12
IO101PB4F9	Y13
IO102NB4F9	AA11
IO102PB4F9	AA12
IO103NB4F9/CLKEN	V12
IO103PB4F9/CLKEP	V13
IO104NB4F9/CLKFN	W11
IO104PB4F9/CLKFP	W12
Bank 5	
IO105NB5F10/CLKGN	U10
IO105PB5F10/CLKGP	U11
IO106NB5F10/CLKHN	V9
IO106PB5F10/CLKHP	V10
IO107NB5F10	Y10
IO107PB5F10	Y11
IO108NB5F10	AA9

FG484	
AX500 Function	**Pin Number**
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	**Pin Number**
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	**Pin Number**
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG676	
AX500 Function	Pin Number
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A11
NC	A21

FG676	
AX500 Function	Pin Number
NC	A22
NC	A24
NC	A25
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
NC	AC25
NC	AD1
NC	AD11
NC	AD16
NC	AD25
NC	AE1
NC	AF2
NC	AF25
NC	B11
NC	B24
NC	B4
NC	C16

FG676	
AX500 Function	Pin Number
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
NC	G21
NC	G22
NC	H21
NC	H22
NC	H23
NC	H5
NC	H6

FG896	
AX1000 Function	Pin Number
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

FG896	
AX1000 Function	Pin Number
GND	W19
GND	Y11
GND	Y20
GND/LP	E4
NC	A16
NC	A26
NC	A4
NC	A6
NC	AA30
NC	AB1
NC	AB30
NC	AC2
NC	AC29
NC	AD1
NC	AD2
NC	AD30
NC	AE1
NC	AE15
NC	AE16
NC	AE2
NC	AE30
NC	AF1
NC	AF2
NC	AF29
NC	AF30
NC	AG1
NC	AG2
NC	AG29
NC	AG30
NC	AH27
NC	AH4
NC	AJ14
NC	AJ15
NC	AJ16
NC	AJ27

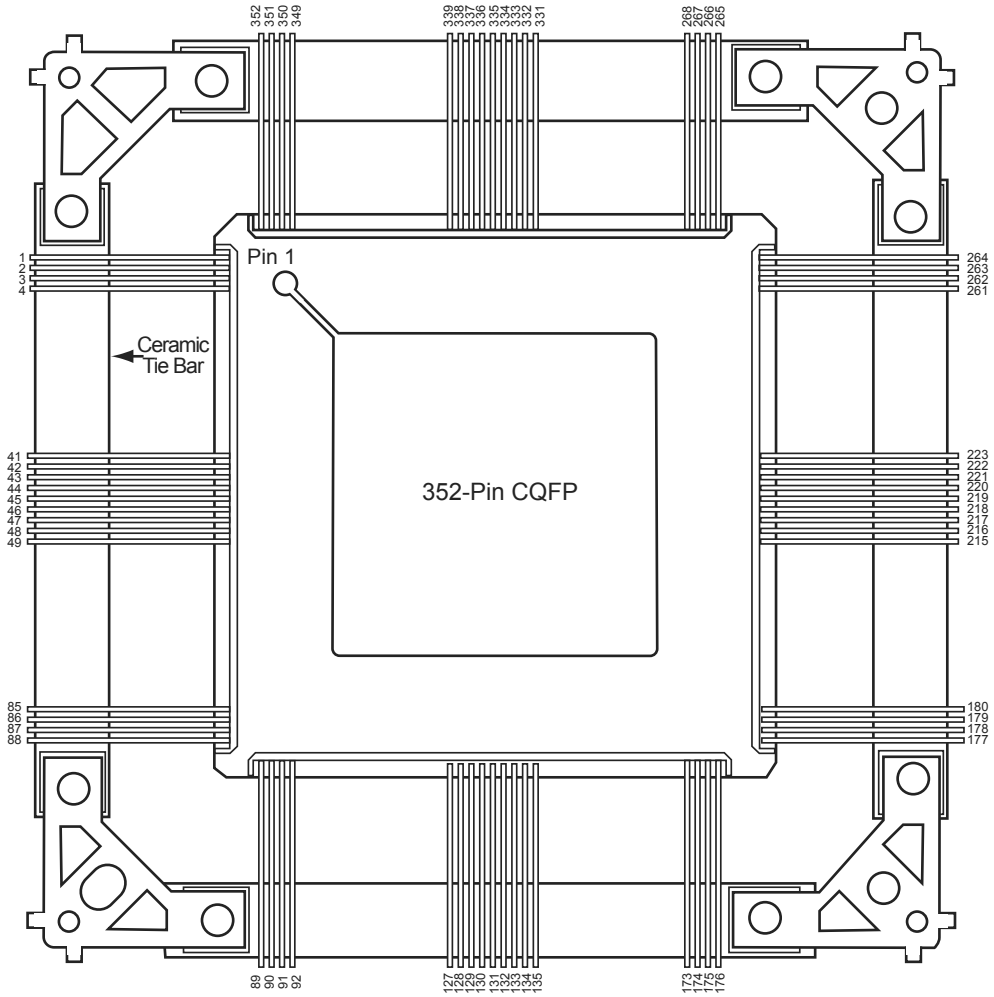
FG896	
AX1000 Function	Pin Number
NC	AJ4
NC	AK14
NC	AK15
NC	AK16
NC	AK17
NC	AK22
NC	AK4
NC	AK5
NC	B16
NC	B18
NC	B21
NC	B23
NC	B26
NC	B4
NC	B6
NC	B8
NC	C27
NC	D1
NC	D2
NC	D29
NC	D30
NC	E1
NC	E2
NC	E29
NC	E30
NC	F15
NC	F16
NC	F29
NC	F30
NC	G1
NC	G29
NC	G30
NC	H29
NC	J1
NC	J30

PQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

PQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

PQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ352



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

CQ352	
AX250 Function	Pin Number
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282

CQ352	
AX250 Function	Pin Number
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224

CQ352	
AX250 Function	Pin Number
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

Revision	Changes	Page
Revision 17 (continued)	The C180 package was removed from product tables and the "Package Pin Assignments" section (PDN 0909).	3-1
	Package names used in the"Axcelerator Family Product Profile" and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	i, 3-1
	The "Introduction" section for "User I/Os" was updated as follows: "The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os" (SARs 24181, 24309).	2-11
	Power values in Table 2-4 • Default CLOAD/VCCI were updated to reflect those of SmartPower (SAR 33945).	2-3
	Two parameter names were corrected in Figure 2-10 • Output Buffer Delays. One occurrence of t_{ENLZ} was changed to t_{ENZL} and one occurrence of t_{ENHZ} was changed to t_{ENZH} (SAR 33890).	2-22
	The "Timing Model" section was updated with new timing values. Timing tables in the "I/O Specifications" section were updated to include enable paths. Values in the timing tables in the "Voltage-Referenced I/O Standards" section and "Differential Standards" section were updated. Table 2-63 • R-Cell was updated (SAR 33945).	2-8, 2-26 to 2-53
	Figure 2-11 • Timing Model was replaced (SAR 33043).	2-23
	The timing tables for "RAM" and "FIFO" were updated (SAR 33945).	2-90 to 2-106
	"Data Registers (DRs)" values were modified for IDCODE and USERCODE (SARs 18257, 26406).	2-108
	The package diagram for the "CQ208" package was incorrect and has been replaced with the correct diagram (SARs 23865, 26345).	3-89
Revision 16 (v2.8, Oct. 2009)	The datasheet was updated to include AX2000-CQ2526 information.	N/A
	MIL-STD-883 Class B is no longer supported by Axcelerator FPGAs and as a result was removed.	N/A
	A footnote was added to the "Introduction" in the "Axcelerator Clock Management System" section.	2-75
Revision 15 (v2.7, Nov. 2008)	RoHS-compliant information was added to the "Ordering Information".	ii
	ACTgen was changed to SmartGen because ACTgen is obsolete.	N/A
Revision 14 (v2.6)	In Table 2-4, the units for the P_{LOAD}, P_{10}, and $P_{I/O}$ were updated from mW/MHz to mW/MHz.	2-3
	In the "Pin Descriptions"section, the HCLK and CLK descriptions were updated to include tie-off information.	2-9
	The "Global Resource Distribution" section was updated.	2-70
	The " CG624" table was updated.	3-116
Revision 13 (v2.5)	A note was added to Table 2-2.	2-1
	In the "Package Thermal Characteristics", the temperature was changed from 150°C to 125°C.	2-6