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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

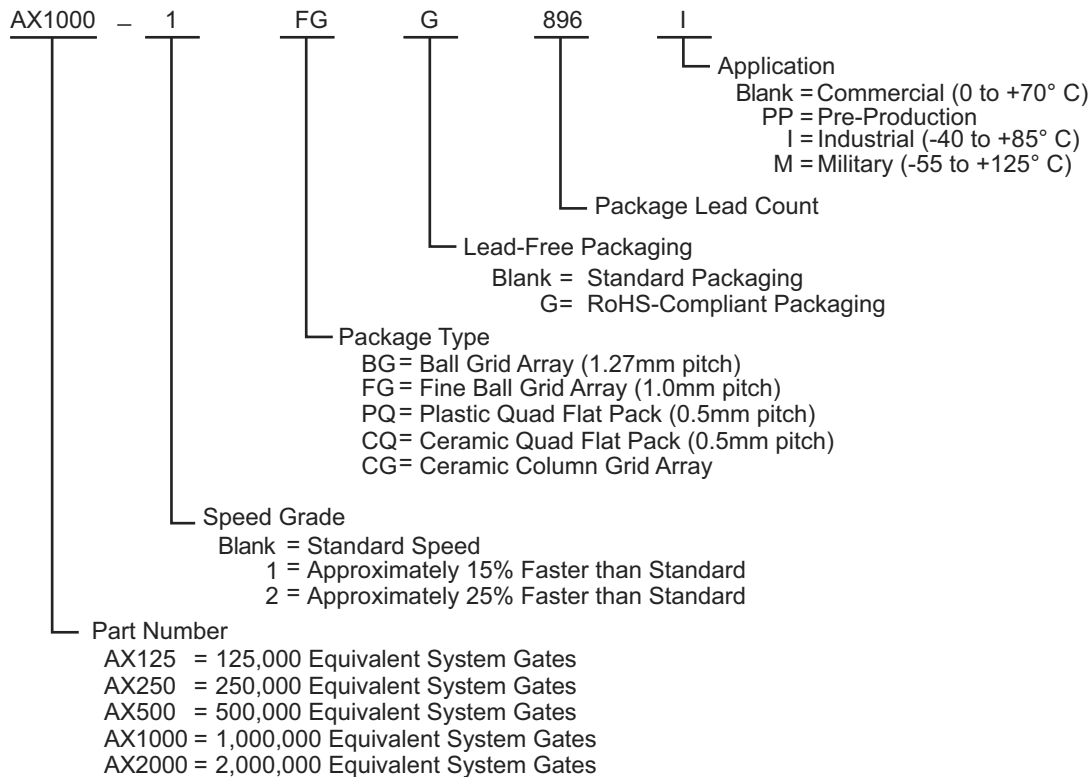
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	729-BBGA
Supplier Device Package	729-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-bg729i

Ordering Information



Device Resources

User I/Os (Including Clock Buffers)					
Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	115	115	–	–
CQ208	–	115	115	–	–
CQ256	–	–	–	–	136
FG256	138	138	–	–	–
FG324	168	–	–	–	–
CQ352	–	198	198	198	198
FG484	–	248	317	317	–
CG624	–	–	–	418	418
FG676	–	–	336	418	–
BG729	–	–	–	516	–
FG896	–	–	–	516	586
FG1152	–	–	–	–	684

Note: The FG256, FG324, and FG484 are footprint compatible with one another. The FG676, FG896, and FG1152 are also footprint compatible with one another.

Table 2-4 • Default CLOAD/VCCI

	C _{LOAD} (pF)	VCCI (V)	PLOAD (mw/MHz)	P10 (mw/MHz)	PI/O (mW/MHz)*
Single-Ended without VREF					
LVTTTL 24 mA High Slew	35	3.3	381.2	267.5	648.7
LVTTTL 16 mA High Slew	35	3.3	381.2	225.1	606.3
LVTTTL 12 mA High Slew	35	3.3	381.2	165.9	547.1
LVTTTL 8 mA High Slew	35	3.3	381.2	130.3	511.5
LVTTTL 24 mA Low Slew	35	3.3	381.2	169.2	550.4
LVTTTL 16 mA Low Slew	35	3.3	381.2	150.8	532.0
LVTTTL 12 mA Low Slew	35	3.3	381.2	138.6	519.8
LVTTTL 8 mA Low Slew	35	3.3	381.2	118.7	499.9
LVC MOS – 25	35	2.5	218.8	148.0	366.8
LVC MOS – 18	35	1.8	113.4	73.4	186.8
LVC MOS – 15 (JESD8-11)	35	1.5	78.8	49.5	128.3
PCI	10	3.3	108.9	218.5	327.4
PCI-X	10	3.3	108.9	162.9	271.8
Single-Ended with VREF					
HSTL-I	20	1.5	–	40.9	40.9
SSTL2-I	30	2.5	–	171.2	171.2
SSTL2-II	30	2.5	–	147.8	147.8
SSTL3-I	30	3.3	–	327.2	327.2
SSTL3-II	30	3.3	–	288.4	288.4
GTLP – 25	10	2.5	–	61.5	61.5
GTLP – 33	10	3.3	–	68.5	68.5
Differential					
LVPECL – 33	N/A	3.3	–	260.6	260.6
LVDS – 25	N/A	2.5	–	145.8	145.8

Note: $*P_{I/O} = P10 + C_{LOAD} * VCC_I^2$

User I/O Naming Conventions

Due to the complex and flexible nature of the Axcelerator family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (Figure 2-7).

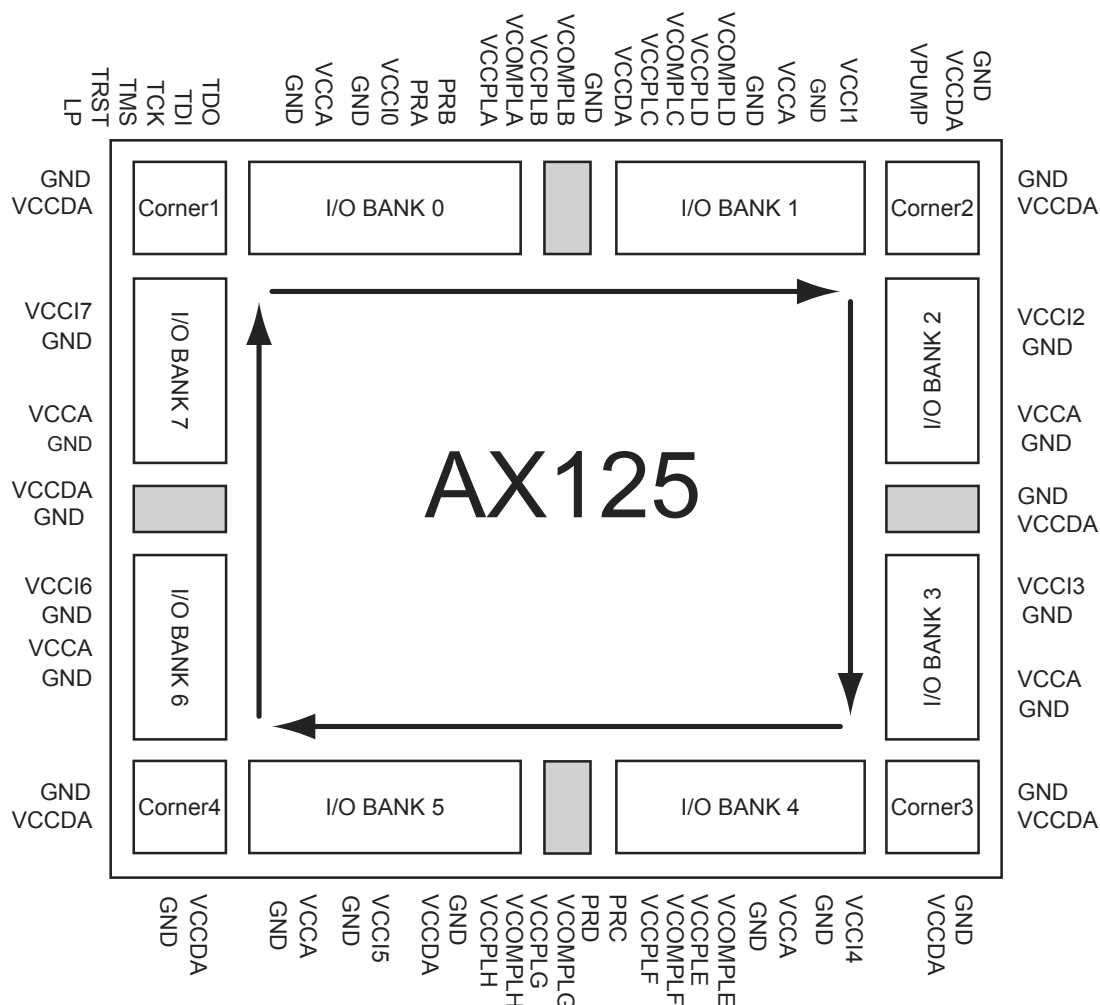
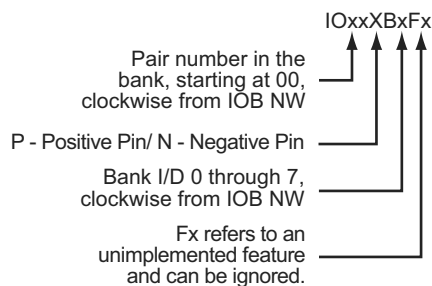


Figure 2-7 • I/O Bank and Dedicated Pin Layout



Examples:

IO12PB1F1 is the positive pin of the thirteenth pair of the first I/O bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair.

For those I/Os that can be employed either as a user I/O or as a special function, the following nomenclature is used:

IOxxXBxFx/special_function_name

IOxxPB1Fx/xCLKx this pin can be configured as a clock input or as a user I/O.

Figure 2-8 • General Naming Schemes

3.3 V LVTTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-20 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
−0.3	0.8	2.0	3.6	0.4	2.4	24	−24

AC Loadings

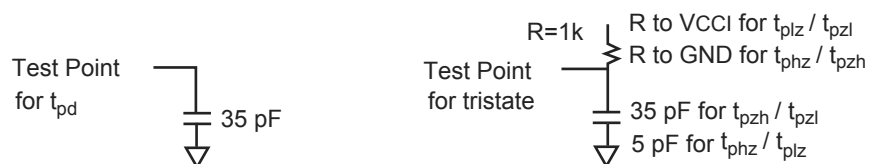


Figure 2-15 • AC Test Loads

Table 2-21 • AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	3.0	1.40	N/A	35

Note: * Measuring Point = VTRIP

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

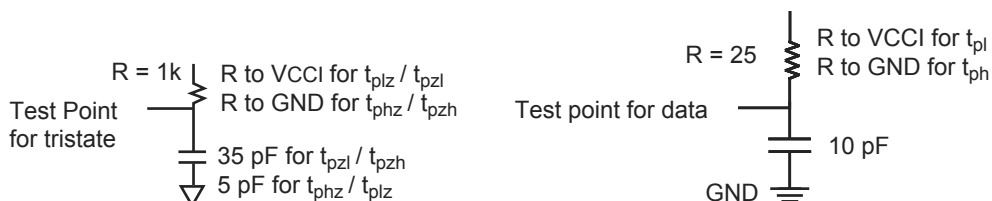


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

Table 2-36 • 3.3 V PCI-X I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI-X Output Module Timing								
t _{DP}	Input Buffer	1.57		1.79		2.10		ns
t _{PY}	Output Buffer	2.10		2.40		2.82		ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low	1.61		1.62		1.63		ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High	1.59		1.60		1.61		ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z	2.65		3.02		3.55		ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z	3.11		3.55		4.17		ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register	0.67		0.77		0.90		ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-37 on page 2-62). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 2-37). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

Figure 2-36 • FastConnect Routing

Figure 2-37 • Horizontal and Vertical Tracks

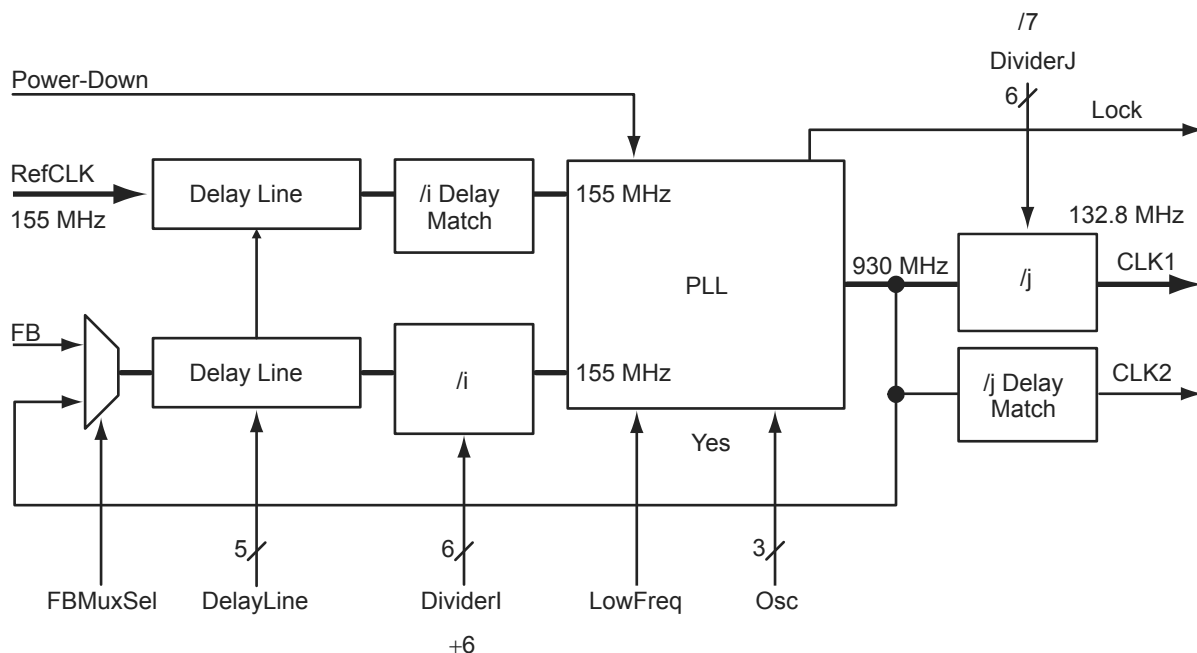


Figure 2-54 • Using the PLL 155 MHz In, 133 MHz Out

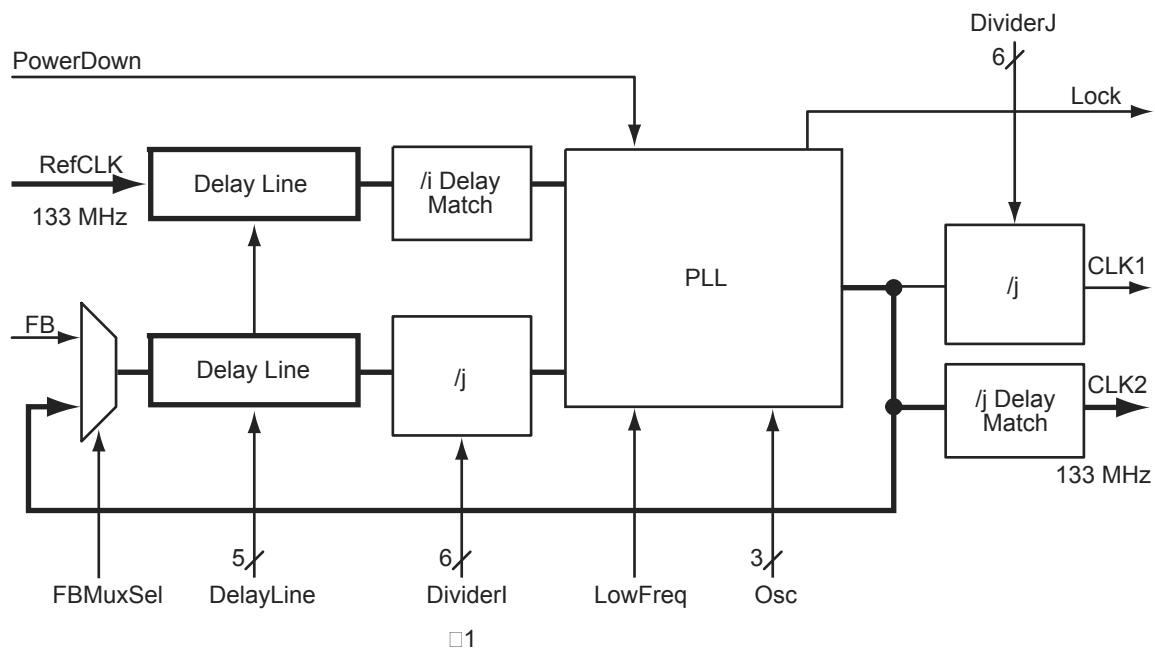
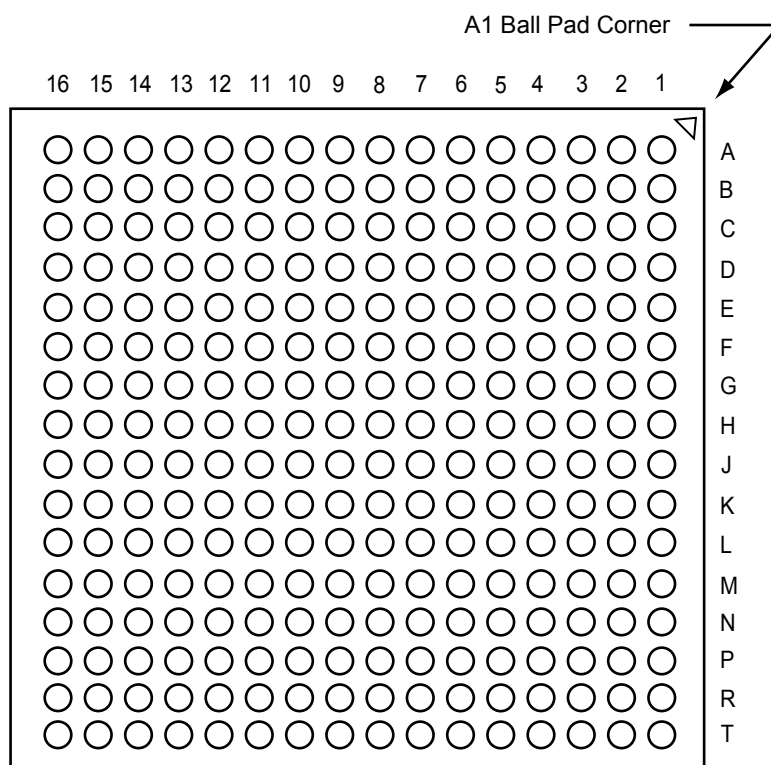


Figure 2-55 • Using the PLL Delaying the Reference Clock

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO218PB6F20	V2	IO236PB7F22	L1	IO255NB7F23	F5
IO219NB6F20	T1	IO237NB7F22	L4	IO255PB7F23	G5
IO219PB6F20	U1	IO237PB7F22	L3	IO256NB7F23	F3
IO220NB6F20	R5	IO238NB7F22	L6	IO256PB7F23	F4
IO220PB6F20	R6	IO238PB7F22	M6	IO257NB7F23	H7
IO221NB6F20	T3	IO239NB7F22	M8	IO257PB7F23	J7
IO221PB6F20	T4	IO239PB7F22	M7	Dedicated I/O	
IO222NB6F20	R2	IO240NB7F22	K2	GND	A1
IO222PB6F20	T2	IO240PB7F22	K1	GND	A2
IO223NB6F20	P8	IO241NB7F22	K4	GND	A25
IO223PB6F20	P9	IO241PB7F22	K3	GND	A26
IO224NB6F20	R3	IO242NB7F22	K5	GND	A27
IO224PB6F20	R4	IO242PB7F22	L5	GND	A3
Bank 7		IO243NB7F22	J2	GND	AC24
IO225NB7F21	P1	IO243PB7F22	J1	GND	AE1
IO225PB7F21	R1	IO244NB7F22	J4	GND	AE2
IO226NB7F21	P3	IO244PB7F22	J3	GND	AE25
IO226PB7F21	P2	IO245NB7F22	H2	GND	AE26
IO227NB7F21	N7	IO245PB7F22	H1	GND	AE27
IO227PB7F21	P7	IO246NB7F22	H4	GND	AE3
IO228NB7F21	P5	IO246PB7F22	H3	GND	AE5
IO228PB7F21	P4	IO247NB7F23	L8	GND	AF1
IO229NB7F21	N2	IO247PB7F23	L7	GND	AF2
IO229PB7F21	N1	IO248NB7F23	J6	GND	AF25
IO230NB7F21	N6	IO248PB7F23	K6	GND	AF26
IO230PB7F21	P6	IO249NB7F23	H5	GND	AF27
IO231NB7F21	N9	IO249PB7F23	J5	GND	AF3
IO231PB7F21	N8	IO250NB7F23	G2	GND	AG1
IO232NB7F21	N4	IO250PB7F23	G1	GND	AG2
IO232PB7F21	N3	IO251NB7F23	K8	GND	AG25
IO233NB7F21	M2	IO251PB7F23	K7	GND	AG26
IO233PB7F21	M1	IO252NB7F23	G4	GND	AG27
IO234NB7F21	M4	IO252PB7F23	G3	GND	AG3
IO234PB7F21	M3	IO253NB7F23	F2	GND	B1
IO235NB7F21	M5	IO253PB7F23	F1	GND	B2
IO235PB7F21	N5	IO254NB7F23	G6	GND	B25
IO236NB7F22	L2	IO254PB7F23	H6	GND	B26

FG256



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
Bank 0		IO17NB1F1	B14	IO34PB2F2	D22
IO00NB0F0	D7	IO17PB1F1	B13	IO35NB2F2	J18
IO00PB0F0	D6	IO18NB1F1	A14	IO35PB2F2	H18
IO01NB0F0	E7	IO18PB1F1	A13	IO36NB2F2	G21
IO01PB0F0	E6	IO19NB1F1	A16	IO36PB2F2	F21
IO02NB0F0	C5	IO19PB1F1	A15	IO37NB2F2	K19
IO02PB0F0	C4	IO20NB1F1	B16	IO37PB2F2	J19
IO03NB0F0	C7	IO20PB1F1	B15	IO38NB2F2	J20
IO03PB0F0	C6	IO21NB1F1	C17	IO38PB2F2	H20
IO04NB0F0	E9	IO21PB1F1	C16	IO39NB2F2	L16
IO04PB0F0	E8	IO22NB1F1	F15	IO39PB2F2	K16
IO05NB0F0	D9	IO22PB1F1	F14	IO40NB2F2	J21
IO05PB0F0	D8	IO23NB1F1	D16	IO40PB2F2	H21
IO06NB0F0	B7	IO23PB1F1	D15	IO41NB2F2	L17
IO06PB0F0	B6	IO24NB1F1	E16	IO41PB2F2	K17
IO07NB0F0	C9	IO24PB1F1	E15	IO42NB2F2	J22
IO07PB0F0	C8	IO25NB1F1	F18	IO42PB2F2	H22
IO08NB0F0	A7	IO25PB1F1	F17	IO43NB2F2	L18
IO08PB0F0	A6	IO26NB1F1	D18	IO43PB2F2	K18
IO09NB0F0	B9	IO26PB1F1	E17	IO44NB2F2	L20
IO09PB0F0	B8	IO27NB1F1	G16	IO44PB2F2	K20
IO10NB0F0	A9	IO27PB1F1	G15	Bank 3	
IO10PB0F0	A8	Bank 2		IO45NB3F3	M19
IO11NB0F0	B10	IO28NB2F2	F19	IO45PB3F3	L19
IO11PB0F0	A10	IO28PB2F2	E19	IO46NB3F3	M21
IO12NB0F0/HCLKAN	E11	IO29NB2F2	J16	IO46PB3F3	L21
IO12PB0F0/HCLKAP	E10	IO29PB2F2	H16	IO47NB3F3	N17
IO13NB0F0/HCLKBN	D12	IO30NB2F2	E20	IO47PB3F3	M17
IO13PB0F0/HCLKBP	D11	IO30PB2F2	D20	IO48NB3F3	N18
Bank 1		IO31NB2F2	J17	IO48PB3F3	N19
IO14NB1F1/HCLKCN	F13	IO31PB2F2	H17	IO49NB3F3	N16
IO14PB1F1/HCLKCP	F12	IO32NB2F2	G20	IO49PB3F3	M16
IO15NB1F1/HCLKDN	E14	IO32PB2F2	F20	IO50NB3F3	N20
IO15PB1F1/HCLKDP	E13	IO33NB2F2	H19	IO50PB3F3	M20
IO16NB1F1	C13	IO33PB2F2	G19	IO51NB3F3	P21
IO16PB1F1	C12	IO34NB2F2	E22	IO51PB3F3	N21

FG676	
AX500 Function	Pin Number
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8

FG676	
AX500 Function	Pin Number
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO51PB1F4	E21	IO68PB2F6	K24	IO86NB2F8	N28
IO52NB1F4	F22	IO69NB2F6	F27	IO86PB2F8	N27
IO52PB1F4	E22	IO69PB2F6	E27	IO87NB2F8	P29
IO53NB1F4	B25	IO70NB2F6	J26	IO87PB2F8	P30
IO53PB1F4	B24	IO70PB2F6	J25	IO88NB2F8	P25
IO54NB1F5	D24	IO71NB2F6	H27	IO88PB2F8	P24
IO54PB1F5	D23	IO71PB2F6	G27	IO89NB2F8	P28
IO55NB1F5	F23	IO72NB2F6	J28	IO89PB2F8	P27
IO55PB1F5	E23	IO72PB2F6	H28	IO90NB2F8	P22
IO56NB1F5	H21	IO73NB2F6	G28	IO90PB2F8	P23
IO56PB1F5	G21	IO73PB2F6	F28	IO91NB2F8	R26
IO57NB1F5	D25	IO74NB2F7	L23	IO91PB2F8	P26
IO57PB1F5	C25	IO74PB2F7	L24	IO92NB2F8	R24
IO58NB1F5	F24	IO75NB2F7	L26	IO92PB2F8	R25
IO58PB1F5	E24	IO75PB2F7	K26	IO93NB2F8	R29
IO59NB1F5	D26	IO76NB2F7	M25	IO93PB2F8	R30
IO59PB1F5	C26	IO76PB2F7	L25	IO94NB2F8	R22
IO60NB1F5	G23	IO77NB2F7	K27	IO94PB2F8	R23
IO60PB1F5	G22	IO77PB2F7	J27	IO95NB2F8	T27
IO61NB1F5	B27	IO78NB2F7	M27	IO95PB2F8	R27
IO61PB1F5	A27	IO78PB2F7	L27	Bank 3	
IO62NB1F5	F25	IO79NB2F7	K30	IO96NB3F9	T29
IO62PB1F5	E25	IO79PB2F7	K29	IO96PB3F9	T30
IO63NB1F5	H23	IO80NB2F7	M23	IO97NB3F9	U29
IO63PB1F5	H22	IO80PB2F7	M24	IO97PB3F9	U30
Bank 2		IO81NB2F7	M28	IO98NB3F9	T22
IO64NB2F6	K23	IO81PB2F7	L28	IO98PB3F9	T23
IO64PB2F6	J23	IO82NB2F7	N26	IO99NB3F9	U26
IO65NB2F6	J24	IO82PB2F7	M26	IO99PB3F9	T26
IO65PB2F6	H24	IO83NB2F7	N25	IO100NB3F9	U24
IO66NB2F6	H26	IO83PB2F7	N24	IO100PB3F9	T24
IO66PB2F6	H25	IO84NB2F7	N22	IO101NB3F9	V28
IO67NB2F6	G26	IO84PB2F7	N23	IO101PB3F9	U28
IO67PB2F6	G25	IO85NB2F8	M29	IO102NB3F9	U23
IO68NB2F6	K25	IO85PB2F8	L29	IO102PB3F9	U22

FG896	
AX1000 Function	Pin Number
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3

FG896	
AX1000 Function	Pin Number
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
Bank 0					
IO00NB0F0	D6	IO17NB0F1	F12	IO34PB0F3	D14
IO00PB0F0	C6	IO17PB0F1	F11	IO35NB0F3	A15
IO01NB0F0	H10	IO18NB0F1	E11	IO35PB0F3	B15
IO01PB0F0	H9	IO18PB0F1	E10	IO36NB0F3	B16
IO02NB0F0	F8	IO19NB0F1	F13	IO36PB0F3	A16
IO02PB0F0	G8	IO19PB0F1	G13	IO37NB0F3	G16
IO03NB0F0	A6	IO20NB0F1	A10	IO37PB0F3	G15
IO03PB0F0	B6	IO20PB0F1	A9	IO38NB0F3	D16
IO04NB0F0	C7	IO21NB0F1	K14	IO38PB0F3	C16
IO04PB0F0	D7	IO21PB0F1	K13	IO39NB0F3	K16
IO05NB0F0	K10	IO22NB0F2	B11	IO39PB0F3	L16
IO05PB0F0	J10	IO22PB0F2	B10	IO40NB0F3	D17
IO06NB0F0	F9	IO23NB0F2	C12	IO40PB0F3	C17
IO06PB0F0	G9	IO23PB0F2	C11	IO41NB0F3/HCLKAN	E16
IO07NB0F0	F10	IO24NB0F2	A12	IO41PB0F3/HCLKAP	F16
IO07PB0F0	G10	IO24PB0F2	A11	IO42NB0F3/HCLKBN	G17
IO08NB0F0	E9	IO25NB0F2	H14	IO42PB0F3/HCLKBP	F17
IO08PB0F0	E8	IO25PB0F2	J14	Bank 1	
IO09NB0F0	J11	IO26NB0F2	D13	IO43NB1F4/HCLKCN	G19
IO09PB0F0	K11	IO26PB0F2	D12	IO43PB1F4/HCLKCP	G18
IO10NB0F0	C8	IO27NB0F2	F14	IO44NB1F4/HCLKDN	E19
IO10PB0F0	D8	IO27PB0F2	G14	IO44PB1F4/HCLKDP	F19
IO11NB0F0	K12	IO28NB0F2	E14	IO45NB1F4	C18
IO11PB0F0	J12	IO28PB0F2	E13	IO45PB1F4	D18
IO12NB0F1	G11	IO29NB0F2	B13	IO46NB1F4	A18
IO12PB0F1	H11	IO29PB0F2	B12	IO46PB1F4	B18
IO13NB0F1	G12	IO30NB0F2	C14	IO47NB1F4	K19
IO13PB0F1	H12	IO30PB0F2	C13	IO47PB1F4	L19
IO14NB0F1	A7	IO31NB0F2	H15	IO48NB1F4	C19
IO14PB0F1	B7	IO31PB0F2	J15	IO48PB1F4	D19
IO15NB0F1	H13	IO32NB0F2	A14	IO49NB1F4	K20
IO15PB0F1	J13	IO32PB0F2	B14	IO49PB1F4	L20
IO16NB0F1	C9	IO33NB0F2	K15	IO50NB1F4	A19
IO16PB0F1	D9	IO33PB0F2	L15	IO50PB1F4	B19
		IO34NB0F3	D15	IO51NB1F4	H20

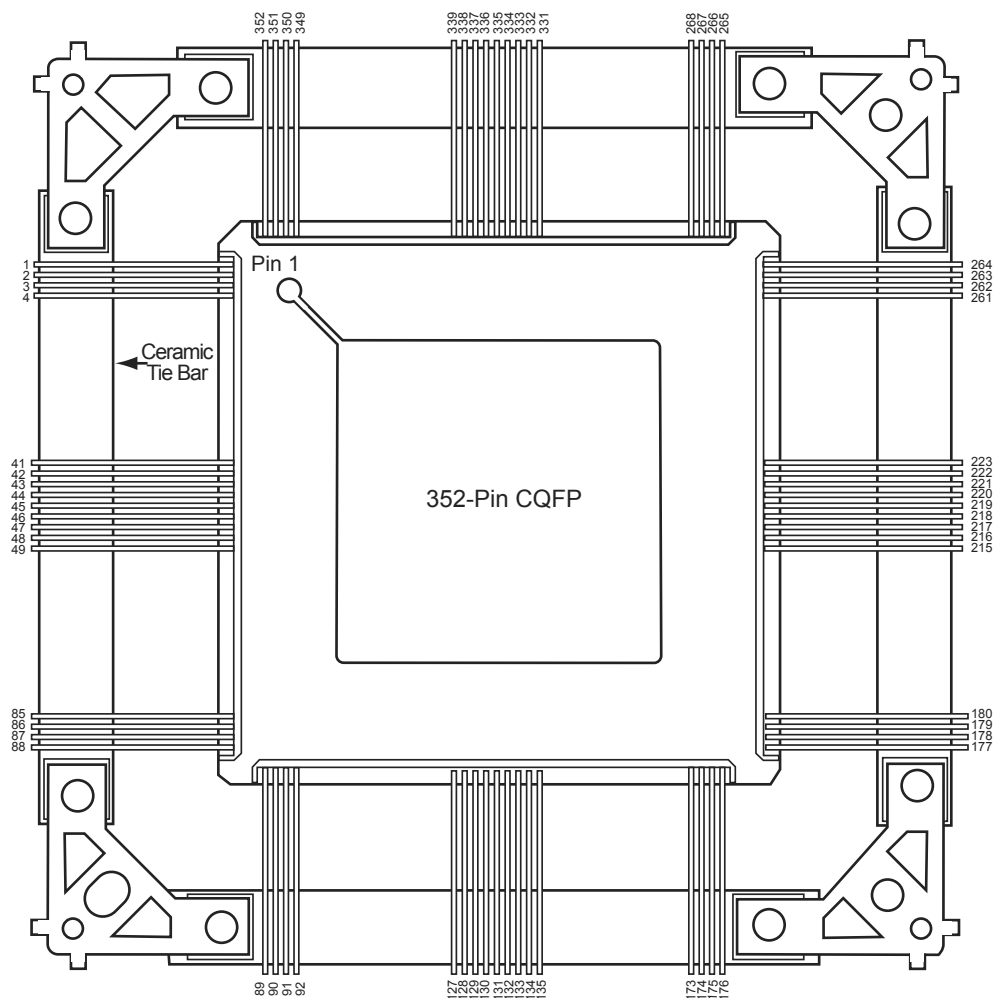
FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO207PB4F19	AL20	IO224PB5F21	AP14	IO242NB5F22	AG11
IO208NB4F19	AG19	IO225NB5F21	AK13	IO242PB5F22	AG12
IO208PB4F19	AF19	IO225PB5F21	AK14	IO243NB5F22	AL9
IO209NB4F19	AN18	IO226NB5F21	AE15	IO243PB5F22	AL10
IO209PB4F19	AP18	IO226PB5F21	AF15	IO244NB5F22	AM8
IO210NB4F19	AE19	IO227NB5F21	AG14	IO244PB5F22	AM9
IO210PB4F19	AD19	IO227PB5F21	AG15	IO245NB5F23	AH10
IO211NB4F19	AL18	IO228NB5F21	AJ13	IO245PB5F23	AJ10
IO211PB4F19	AM18	IO228PB5F21	AJ14	IO246NB5F23	AF10
IO212NB4F19/CLKEN	AJ20	IO229NB5F21	AM13	IO246PB5F23	AF11
IO212PB4F19/CLKEP	AK20	IO229PB5F21	AM14	IO247NB5F23	AJ9
IO213NB4F19/CLKFN	AJ18	IO230NB5F21	AE14	IO247PB5F23	AK9
IO213PB4F19/CLKFP	AJ19	IO230PB5F21	AF14	IO248NB5F23	AN7
Bank 5		IO231NB5F21	AN12	IO248PB5F23	AP7
IO214NB5F20/CLKGN	AJ16	IO231PB5F21	AP12	IO249NB5F23	AL7
IO214PB5F20/CLKGP	AJ17	IO232NB5F21	AG13	IO249PB5F23	AL8
IO215NB5F20/CLKHN	AJ15	IO232PB5F21	AH13	IO250NB5F23	AE10
IO215PB5F20/CLKHP	AK15	IO233NB5F21	AL12	IO250PB5F23	AE11
IO216NB5F20	AD16	IO233PB5F21	AL13	IO251NB5F23	AK8
IO216PB5F20	AE17	IO234NB5F21	AE13	IO251PB5F23	AJ8
IO217NB5F20	AM17	IO234PB5F21	AF13	IO252NB5F23	AH8
IO217PB5F20	AL17	IO235NB5F22	AN11	IO252PB5F23	AH9
IO218NB5F20	AG16	IO235PB5F22	AP11	IO253NB5F23	AN6
IO218PB5F20	AF16	IO236NB5F22	AM11	IO253PB5F23	AP6
IO219NB5F20	AM16	IO236PB5F22	AM12	IO254NB5F23	AG9
IO219PB5F20	AL16	IO237NB5F22	AJ11	IO254PB5F23	AG10
IO220NB5F20	AP16	IO237PB5F22	AJ12	IO255NB5F23	AJ7
IO220PB5F20	AN16	IO238NB5F22	AH11	IO255PB5F23	AK7
IO221NB5F20	AN15	IO238PB5F22	AH12	IO256NB5F23	AL6
IO221PB5F20	AP15	IO239NB5F22	AK10	IO256PB5F23	AM6
IO222NB5F20	AD15	IO239PB5F22	AK11	Bank 6	
IO222PB5F20	AE16	IO240NB5F22	AE12	IO257NB6F24	AG6
IO223NB5F21	AL14	IO240PB5F22	AF12	IO257PB6F24	AH6
IO223PB5F21	AL15	IO241NB5F22	AN10	IO258NB6F24	AD9
IO224NB5F21	AN14	IO241PB5F22	AP10	IO258PB6F24	AE9

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

Revision	Changes	Page
Revision 10 (continued)	The "TRST" section was updated.	2-107
	The "Global Set Fuse" section was added.	2-109
	A footnote was added to "FG896" for the AX2000 regarding pins AB1, AE2, G1, and K2.	3-52
	Pinouts for the AX250, AX500, and AX1000 were added for "CQ352".	3-98
	Pinout for the AX1000 was added for "CG624".	3-115
Revision 9 (v2.1)	Table 2-79 was updated.	2-69
	The "Low Power Mode" section was updated.	2-106
Revision 8 (v2.0)	Table 1 has been updated.	i
	The "Ordering Information" section has been updated.	ii
	The "Device Resources" section has been updated.	ii
	The "Temperature Grade Offerings" section is new.	iii
	The "Speed Grade and Temperature Grade Matrix" section has been updated.	iii
	Table 2-9 has been updated.	2-12
	Table 2-10 has been updated.	2-12
	Table 2-1 has been updated.	2-1
	Table 2-2 has been updated.	2-1
	Table 2-3 has been updated.	2-2
	Table 2-4 has been updated.	2-3
	Table 2-5 has been updated.	2-4
	The "Power Estimation Example" section has been updated.	2-5
	The "Thermal Characteristics" section has been updated.	2-6
	The "Package Thermal Characteristics" section has been updated.	2-6
	The "Timing Characteristics" section has been updated.	2-7
	The "Pin Descriptions" section has been updated.	2-9
	Timing numbers have been updated from the "3.3 V LVTTTL" section to the "Timing Characteristics" section. Many AC Loads were updated as well.	2-25 to 2-59
	Timing characteristics for the "Hardwired Clocks" and "Routed Clocks" sections were updated.	2-66, 2-68
	Table 2-89 to Table 2-92 and Table 2-98 to Table 2-99 were updated.	2-90 to 2-93, 2-102 to 2-103
	The following sections were updated: "Low Power Mode", "Interface", "Data Registers (DRs)", "Security", "Silicon Explorer II Probe Interface", and "Programming"	2-106 to 2-110
	In the "PQ208" (AX500) section, pins 2, 52, and 156 changed from V _{CCDA} to V _{CCA} . For pins 170 and 171, the I/O names refer to pair 23 instead of 24.	3-84



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