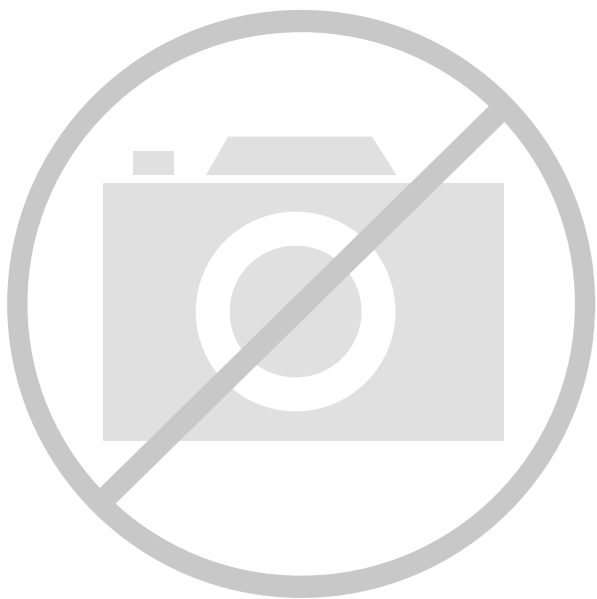




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	729-BBGA
Supplier Device Package	729-PBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-bg729m

I/O Standard Electrical Specifications

Table 2-18 • Input Capacitance

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF

Table 2-19 • I/O Input Rise Time and Fall Time*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTTL	No Requirement	50 ns
LVC MOS 2.5V	No Requirement	50 ns
LVC MOS 1.8V	No Requirement	50 ns
LVC MOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

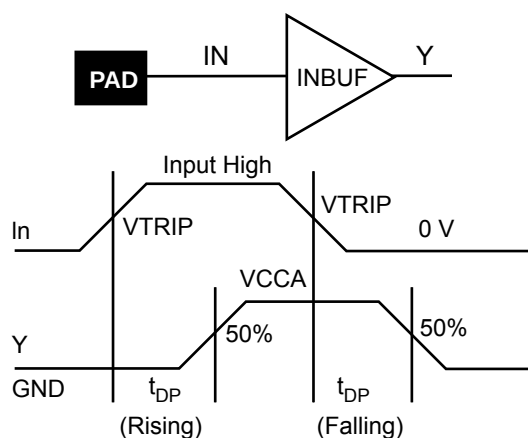


Figure 2-9 • Input Buffer Delays

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 1 (8 mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		4.23		4.81		5.66	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		4.64		5.28		6.21	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.23		4.81		5.66	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.01		2.02		2.03	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 4 (24mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		2.99		3.41		4.01	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.49		2.51		2.51	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.59		2.95		3.46	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.56		4.06		4.77	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Model and Waveforms

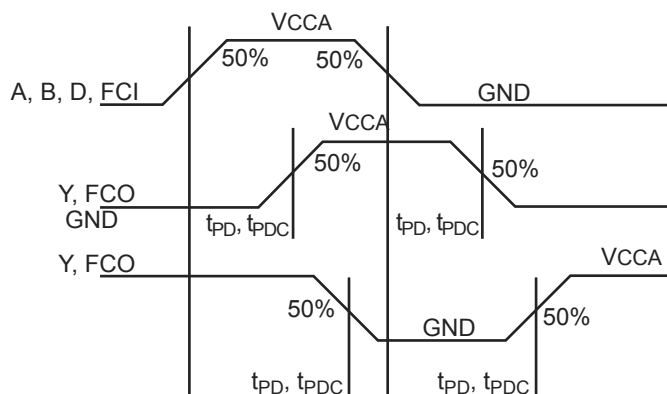


Figure 2-28 • C-Cell Timing Model and Waveforms

Timing Characteristics

Table 2-62 • C-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t _{PD}	Any input to output Y	0.74		0.84		0.99		ns
t _{PDC}	Any input to carry chain output (FCO)	0.57		0.64		0.76		ns
t _{PDB}	Any input through DB when one input is used	0.95		1.09		1.28		ns
t _{CCY}	Input to carry chain (FCI) to Y	0.61		0.69		0.82		ns
t _{CC}	Input to carry chain (FCI) to carry chain output (FCO)	0.08		0.09		0.11		ns

The ClockTileDist Cluster contains an HCLKMux (HM) module for each of the four HCLK trees and a CLKMux (CM) module for each of the CLK trees. The HCLK branches then propagate horizontally through the middle of the core tile to HCLKColDist (HD) modules in every SuperCluster column. The CLK branches propagate vertically through the center of the core tile to CLKRowDist (RD) modules in every SuperCluster row. Together, the HCLK and CLK branches provide for a low-skew global fanout within the core tile (Figure 2-40 and Figure 2-41).

Figure 2-40 • CTD, CD, and HD Module Layout

Figure 2-41 • HCLK and CLK Distribution within a Core Tile

Special PLL Macros

Table 2-84 shows the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

Table 2-84 • PLL Special Macros

Macro Name	Usage
PLLINT	Connects RefCLK to a regular routed net or a pad.
PLLCLK	Connects CLK1 or CLK2 to the CLK network.
PLHCLK	Connects CLK1 or CLK2 to the HCLK network.
PLLOUT	Connects CLK1 or CLK2 to a regular routed net.

Table 2-85 • Electrical Specifications

Parameter	Value	Notes
Frequency Ranges		
Reference Frequency (min.)	14 MHz	Lowest input frequency
Reference Frequency (max.)	200 MHz	Highest input frequency
OSC Frequency (min.)	20 MHz	Lowest output frequency
OSC Frequency (max.)	1 GHz	Highest output frequency
Jitter		
Long-Term Jitter (max.)	1%	Percentage of period, low reference clock frequencies
Long-Term Jitter (max.)	100ps	High reference clock frequencies
Short-Term Jitter (max.)	50ps+1%	Percentage of output frequency
Acquisition Time (lock) from Cold Start		
Acquisition Time (max.)*	400 cycles	Period of low reference clock frequencies
Acquisition Time (max.)*	1.5 μ s	High reference clock frequencies
Power Consumption		
Analog Supply Current (low freq.)	200 μ A	Current at minimum oscillator frequency
Analog Supply Current (high freq.)	200 μ A	Frequency-dependent current
Digital Supply Current (low freq.)	0.5 μ A/MHz	Current at maximum oscillator frequency, unloaded
Digital Supply Current (high freq.)	1 μ A/MHz	Frequency-dependent current
Duty Cycle		
Minimum Output Duty Cycle	45%	
Maximum Output Duty Cycle	55%	

Note: *The lock bit remains Low until RefCLK reaches the minimum input frequency.

Table 2-93 • Sixteen RAM Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t _{WDASU}	Write Data Setup vs. WCLK		16.54		18.84		22.15	ns
t _{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WADSU}	Write Address Setup vs. WCLK		16.54		18.84		22.15	ns
t _{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WENSU}	Write Enable Setup vs. WCLK		16.54		18.84		22.15	ns
t _{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t _{WCLK}	WCLK Minimum Low Pulse Width	13.40		13.40		13.40		ns
t _{WCKP}	WCLK Minimum Period	14.15		14.15		14.15		ns
Read Mode								
t _{RADSU}	Read Address Setup vs. RCLK		18.13		20.65		24.27	ns
t _{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RENSU}	Read Enable Setup vs. RCLK		18.13		20.65		24.27	ns
t _{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
t _{RCK2RD2}	RCLK-To-OUT (Non-Pipelined)		12.83		14.62		17.18	ns
t _{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t _{RCLKL}	RCLK Minimum Low Pulse Width	14.41		14.41		14.41		ns
t _{RCKP}	RCLK Minimum Period	15.14		15.14		15.14		ns

Note: Timing data for these sixteen cascaded RAM blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

Timing Characteristics

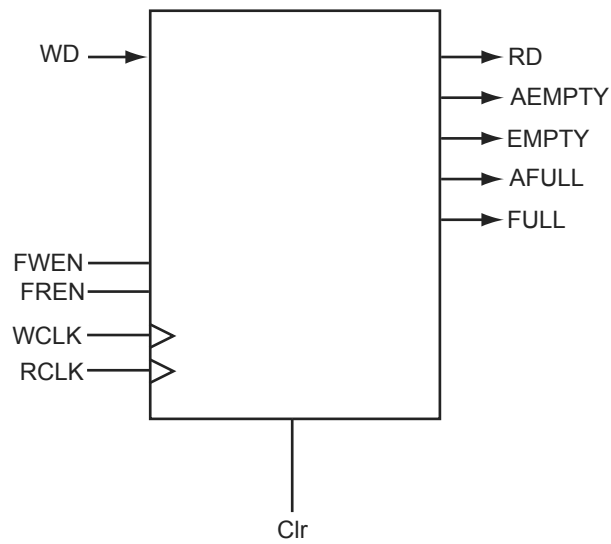


Figure 2-66 • FIFO Model

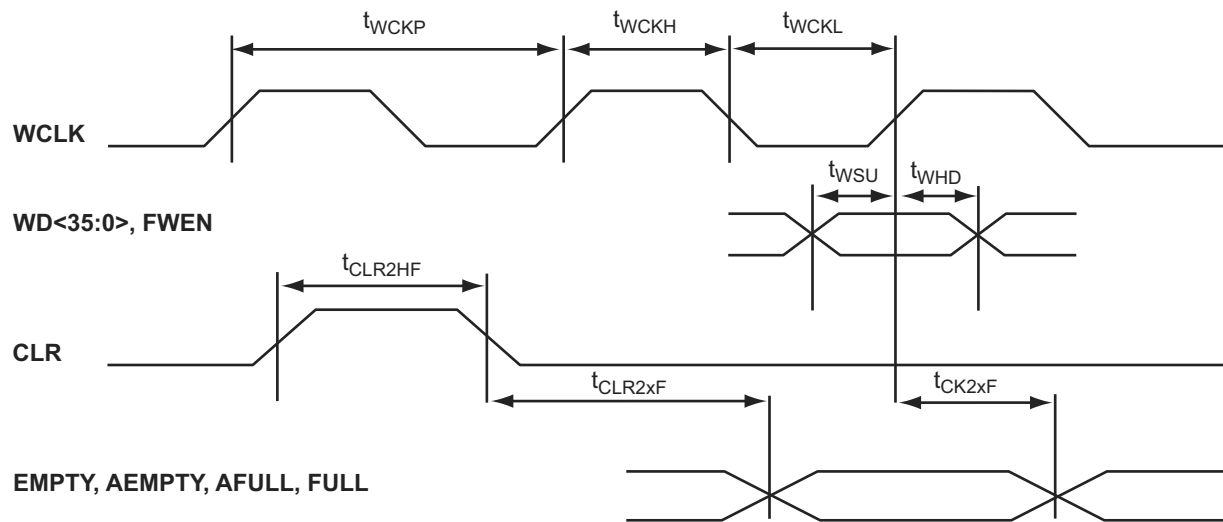


Figure 2-67 • FIFO Write Timing

Programming

Device programming is supported through the Silicon Sculptor II, a single-site, robust and compact device programmer for the PC. Up to four Silicon Sculptor IIs can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor II to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor II also provides a self-test to test its own hardware extensively.

Programming an Axcelerator device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

1. Load the *.AFM file.
2. Select the device to be programmed.
3. Begin programming.

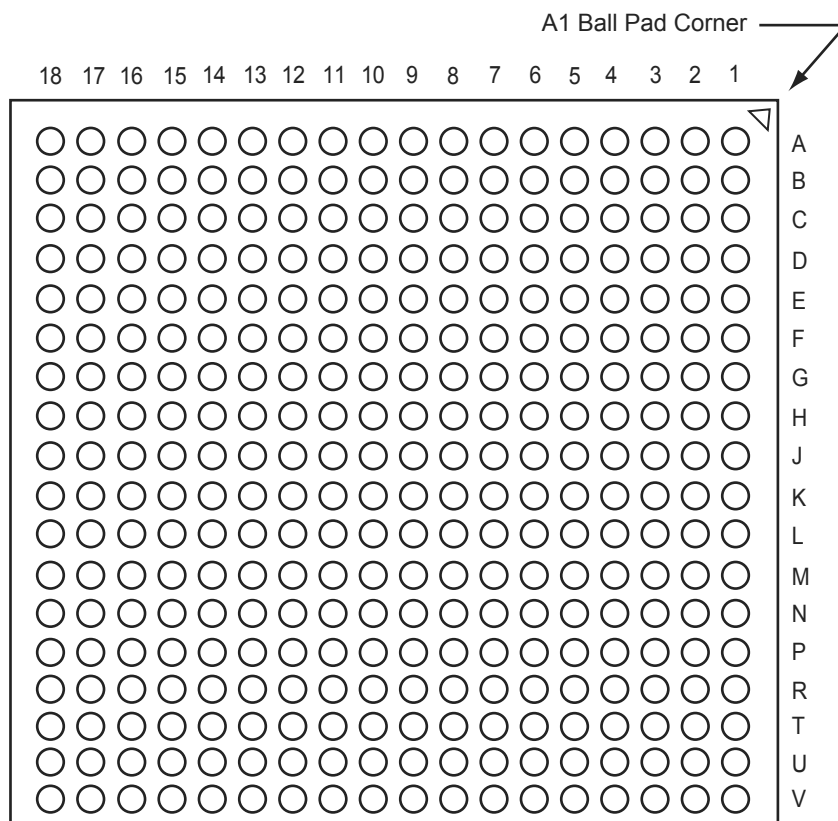
When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via our In-House Programming Center.

In addition, BP Microsystems offers multi-site programmers that provide qualified support for Axcelerator devices.

For more details on programming the Axcelerator devices, please refer to the *Silicon Sculptor II User's Guide*.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO54PB1F5	E20	IO72PB2F6	J23	IO91NB2F8	N25
IO55NB1F5	E21	IO73NB2F6	H24	IO91PB2F8	N24
IO55PB1F5	D21	IO73PB2F6	H23	IO92NB2F8	N27
IO56NB1F5	H19	IO74NB2F7	L21	IO92PB2F8	N26
IO56PB1F5	G19	IO74PB2F7	K21	IO93NB2F8	P26
IO57NB1F5	D22	IO75NB2F7	G27	IO93PB2F8	P27
IO57PB1F5	C22	IO75PB2F7	F27	IO94NB2F8	N19
IO58NB1F5	B23	IO76NB2F7	K23	IO94PB2F8	N20
IO58PB1F5	A23	IO76PB2F7	K22	IO95NB2F8	P23
IO59NB1F5	D23	IO77NB2F7	H26	IO95PB2F8	P22
IO59PB1F5	C23	IO77PB2F7	H25	Bank 3	
IO60NB1F5	G21	IO78NB2F7	K25	IO96NB3F9	P25
IO60PB1F5	G20	IO78PB2F7	K24	IO96PB3F9	P24
IO61NB1F5	E23	IO79NB2F7	J26	IO97NB3F9	R26
IO61PB1F5	E22	IO79PB2F7	J25	IO97PB3F9	R27
IO62NB1F5	F22	IO80NB2F7	M20	IO98NB3F9	P21
IO62PB1F5	F21	IO80PB2F7	L20	IO98PB3F9	P20
IO63NB1F5	H20	IO81NB2F7	J27	IO99NB3F9	R24
IO63PB1F5	J19	IO81PB2F7	H27	IO99PB3F9	R25
Bank 2		IO82NB2F7	L23	IO100NB3F9	T26
IO64NB2F6	J21	IO82PB2F7	L22	IO100PB3F9	T27
IO64PB2F6	H21	IO83NB2F7	L25	IO101NB3F9	T24
IO65NB2F6	F24	IO83PB2F7	L24	IO101PB3F9	T25
IO65PB2F6	F23	IO84NB2F7	N21	IO102NB3F9	R20
IO66NB2F6	F26	IO84PB2F7	M21	IO102PB3F9	R21
IO66PB2F6	F25	IO85NB2F8	K27	IO103NB3F9	R23
IO67NB2F6	E26	IO85PB2F8	K26	IO103PB3F9	R22
IO67PB2F6	E25	IO86NB2F8	M23	IO104NB3F9	U26
IO68NB2F6	J22	IO86PB2F8	M22	IO104PB3F9	U27
IO68PB2F6	H22	IO87NB2F8	M25	IO105NB3F9	U24
IO69NB2F6	G24	IO87PB2F8	M24	IO105PB3F9	U25
IO69PB2F6	G23	IO88NB2F8	L27	IO106NB3F9	R19
IO70NB2F6	K20	IO88PB2F8	L26	IO106PB3F9	P19
IO70PB2F6	J20	IO89NB2F8	M27	IO107NB3F10	V26
IO71NB2F6	G26	IO89PB2F8	M26	IO107PB3F10	V27
IO71PB2F6	G25	IO90NB2F8	N23	IO108NB3F10	T23
IO72NB2F6	J24	IO90PB2F8	N22	IO108PB3F10	T22

FG324



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG676	
AX500 Function	Pin Number
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A11
NC	A21

FG676	
AX500 Function	Pin Number
NC	A22
NC	A24
NC	A25
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
NC	AC25
NC	AD1
NC	AD11
NC	AD16
NC	AD25
NC	AE1
NC	AF2
NC	AF25
NC	B11
NC	B24
NC	B4
NC	C16

FG676	
AX500 Function	Pin Number
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
NC	G21
NC	G22
NC	H21
NC	H22
NC	H23
NC	H5
NC	H6

FG676	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10

FG676	
AX1000 Function	Pin Number
IO21PB0F1	C10
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
Bank 1	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20

FG676	
AX1000 Function	Pin Number
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20
IO52PB1F4	C20
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
Bank 2	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24

FG676	
AX1000 Function	Pin Number
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11

FG676	
AX1000 Function	Pin Number
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11

FG676	
AX1000 Function	Pin Number
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0		IO17NB0F1	B11	IO34NB1F3	A17
IO00NB0F0	D6	IO17PB0F1	B10	IO34PB1F3	B17
IO00PB0F0	E6	IO18NB0F1	D11	IO35NB1F3	D18
IO01NB0F0	A5	IO18PB0F1	E11	IO35PB1F3	C18
IO01PB0F0	B5	IO19NB0F1	C12	IO36NB1F3	H17
IO02NB0F0	G9	IO19PB0F1	C11	IO36PB1F3	J17
IO02PB0F0	G8	IO20NB0F1	F12	IO37NB1F3	B19
IO03NB0F0	F8	IO20PB0F1	G12	IO37PB1F3	A19
IO03PB0F0	F7	IO21NB0F1	D12	IO38NB1F3	H18
IO04NB0F0	D7	IO21PB0F1	E12	IO38PB1F3	J18
IO04PB0F0	E7	IO22NB0F2	H13	IO39NB1F3	B20
IO05NB0F0	C7	IO22PB0F2	J13	IO39PB1F3	A20
IO05PB0F0	C6	IO23NB0F2	A12	IO40NB1F3	C20
IO06NB0F0	H9	IO23PB0F2	A11	IO40PB1F3	C19
IO06PB0F0	H8	IO24NB0F2	F13	IO41NB1F4	E20
IO07NB0F0	D8	IO24PB0F2	G13	IO41PB1F4	E19
IO07PB0F0	E8	IO25NB0F2	B13	IO42NB1F4	F18
IO08NB0F0	E9	IO25PB0F2	B12	IO42PB1F4	G18
IO08PB0F0	F9	IO26NB0F2	E14	IO43NB1F4	A22
IO09NB0F0	A7	IO26PB0F2	E13	IO43PB1F4	A21
IO09PB0F0	B7	IO27NB0F2	B14	IO44NB1F4	F20
IO10NB0F0	H10	IO27PB0F2	A14	IO44PB1F4	F19
IO10PB0F0	G10	IO28NB0F2	H14	IO45NB1F4	D21
IO11NB0F0	C9	IO28PB0F2	J14	IO45PB1F4	D20
IO11PB0F0	C8	IO29NB0F2	B15	IO46NB1F4	D22
IO12NB0F1	E10	IO29PB0F2	A15	IO46PB1F4	C22
IO12PB0F1	F10	IO30NB0F2/HCLKAN	C14	IO47NB1F4	A25
IO13NB0F1	D10	IO30PB0F2/HCLKAP	D14	IO47PB1F4	A24
IO13PB0F1	D9	IO31NB0F2/HCLKBN	E15	IO48NB1F4	H19
IO14NB0F1	F11	IO31PB0F2/HCLKBP	D15	IO48PB1F4	G19
IO14PB0F1	G11	Bank 1		IO49NB1F4	C24
IO15NB0F1	A10	IO32NB1F3/HCLKCN	E17	IO49PB1F4	C23
IO15PB0F1	A9	IO32PB1F3/HCLKCP	E16	IO50NB1F4	G20
IO16NB0F1	H12	IO33NB1F3/HCLKDN	C17	IO50PB1F4	H20
IO16PB0F1	H11	IO33PB1F3/HCLKDP	D17	IO51NB1F4	F21

FG896	
AX2000 Function	Pin Number
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	Pin Number
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

PQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132

PQ208	
AX500 Function	Pin Number
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
Bank 4	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76

PQ208	
AX500 Function	Pin Number
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18

CQ352	
AX250 Function	Pin Number
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282

CQ352	
AX250 Function	Pin Number
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224

CQ352	
AX250 Function	Pin Number
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0					
IO00NB0F0	F8	IO23NB0F2	E11	IO42NB1F4	G21
IO00PB0F0	F7	IO23PB0F2	F11	IO42PB1F4	G20
IO02NB0F0	G7	IO24NB0F2	D7	IO43NB1F4	A16
IO02PB0F0	G6	IO24PB0F2	E7	IO43PB1F4	A15
IO04NB0F0	E9	IO25PB0F2	B12	IO44NB1F4	A20
IO04PB0F0	D8	IO26NB0F2	H11	IO44PB1F4	A19
IO06NB0F0	G9	IO26PB0F2	G11	IO45NB1F4	B17
IO06PB0F0	G8	IO27NB0F2	C11	IO45PB1F4	B16
IO07PB0F0	B6	IO27PB0F2	B8	IO46NB1F4	G17
IO08NB0F0	F10	IO28NB0F2	J13	IO46PB1F4	H17
IO08PB0F0	F9	IO28PB0F2	K13	IO47NB1F4	A17
IO09PB0F0	C7	IO29NB0F2	J8	IO48NB1F4	C19
IO10NB0F0	H8	IO29PB0F2	J7	IO48PB1F4	C18
IO10PB0F0	H7	IO30NB0F2/HCLKAN	G13	IO49NB1F4	B20
IO11NB0F0	D10	IO30PB0F2/HCLKAP	G12	IO49PB1F4	B19
IO11PB0F0	D9	IO31NB0F2/HCLKBN	C13	IO50NB1F4	H20
IO12NB0F1	B5	IO31PB0F2/HCLKBP	C12	IO50PB1F4	H19
IO12PB0F1	B4	Bank 1		IO51NB1F4	A22
IO13NB0F1	A7	IO32NB1F3/HCLKCN	G15	IO51PB1F4	A21
IO13PB0F1	A6	IO32PB1F3/HCLKCP	G14	IO52NB1F4	C21
IO14NB0F1	C9	IO33NB1F3/HCLKDN	B14	IO52PB1F4	C20
IO14PB0F1	C8	IO33PB1F3/HCLKDP	B13	IO53NB1F4	B22
IO15PB0F1	B7	IO34NB1F3	G16	IO53PB1F4	B21
IO16NB0F1	A5	IO34PB1F3	H16	IO54NB1F5	J18
IO16PB0F1	A4	IO35NB1F3	C17	IO54PB1F5	J19
IO17NB0F1	A9	IO35PB1F3	B18	IO55NB1F5	D18
IO17PB0F1	B9	IO36NB1F3	H18	IO55PB1F5	D17
IO18NB0F1	D12	IO36PB1F3	H15	IO56NB1F5	F20
IO18PB0F1	D11	IO37NB1F3	H13	IO56PB1F5	F19
IO20NB0F1	B11	IO38NB1F3	E15	IO58NB1F5	E17
IO20PB0F1	B10	IO38PB1F3	F15	IO58PB1F5	F17
IO21NB0F1	A11	IO39NB1F3	D14	IO60NB1F5	D20
IO21PB0F1	A10	IO39PB1F3	C14	IO60PB1F5	D19
IO22NB0F2	H10	IO40NB1F3	D16	IO62NB1F5	E18
IO22PB0F2	H9	IO40PB1F3	D15	IO62PB1F5	F18
		IO41NB1F4	F16	IO63NB1F5	G19

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Axcelerator Family Device Status" table on page iii, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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