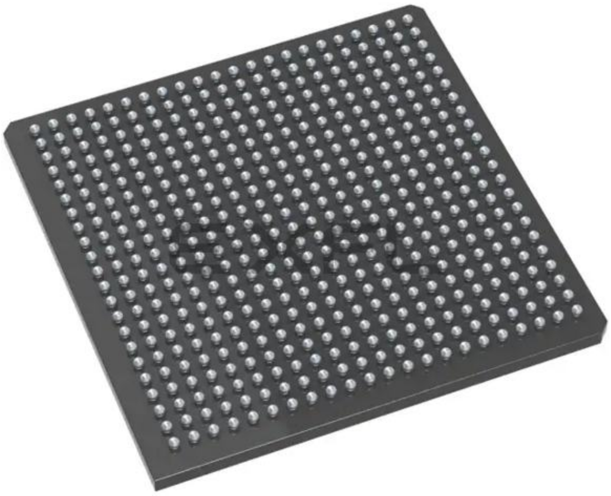
Microchip Technology - AX1000-FG484I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-fg484i

1 – General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microsemi AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

Device Architecture

AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

The very nature of Microsemi's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-108).

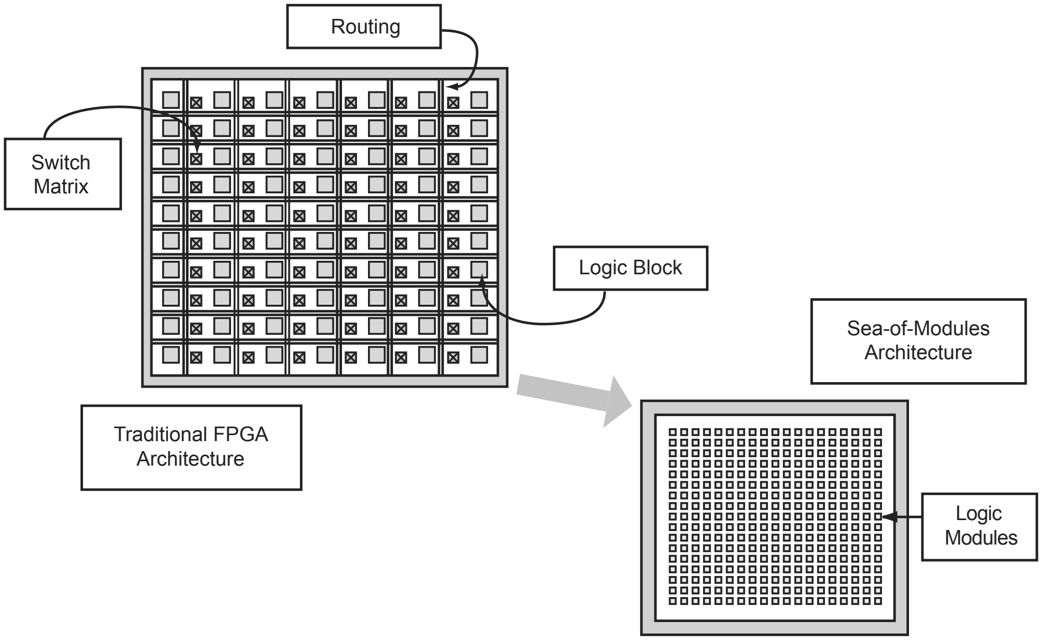


Figure 1-1 • **Sea-of-Modules Comparison**

Calculating Power Dissipation

Table 2-3 • **Standby Current**

Device	Temperature	ICCA	ICCDA	ICCBANK		ICCPLL	ICCCP[1]			
		Standby Current (Core)	Standby Current, Differential I/O	Standby Current per I/O Bank		Standby Current per PLL	Standby Current, Charge Pump		IIH, IIL, IOZ[2]	Units
				2.5 V VCCI	3.3 V VCCI		Active	Bypassed Mode		
AX125	Typical at 25°C	1.5	1.5	0.2	0.3	0.2	0.3	0.01	±0.01	mA
	70°C	15	6	0.5	0.75	1	0.4	0.01	±0.01	mA
	85°C	25	6	0.6	0.8	1	0.4	0.2	±0.01	mA
	125°C	50	8	1	1.5	2	0.4	0.5	±0.01	mA
AX250	Typical at 25°C	1.5	1.4	0.25	0.4	0.2	0.3	0.01	±0.01	mA
	70°C	30	7	0.8	0.9	1	0.4	0.01	±0.01	mA
	85°C	40	7	0.8	1	1	0.4	0.2	±0.01	mA
	125°C	70	9	1.3	1.8	2	0.4	0.5	±0.01	mA
AX500	Typical at 25°C	5	1.4	0.4	0.75	0.2	0.3	0.01	±0.01	mA
	70°C	60	7	1	1.5	1	0.4	0.01	±0.01	mA
	85°C	80	7	1	1.9	1	0.4	0.2	±0.01	mA
	125°C	180	9	1.75	2.5	1.5	0.4	0.5	±0.01	mA
AX1000	Typical at 25°C	7.5	1.5	0.5	1.25	0.2	0.3	0.01	±0.01	mA
	70°C	80	8	1.5	3	1	0.4	0.01	±0.01	mA
	85°C	120	8	1.5	3.4	1	0.4	0.2	±0.01	mA
	125°C	200	10	3	4	1.5	0.4	0.5	±0.01	mA
AX2000	Typical at 25°C	20	1.6	0.7	1.5	0.2	0.3	0.01	±0.01	mA
	70°C	160	10	2	7	1	0.4	0.01	±0.01	mA
	85°C	200	10	3	8	1	0.4	0.2	±0.01	mA
	125°C	500	15	4	10	1.5	0.4	0.5	±0.01	mA

Notes:

1. *ICCCP Active is the ICCDA or the Internal Charge Pump current. ICCCP Bypassed mode is the External Charge Pump current IIH (VPUMP pin).*
2. *IIH, IIL, or IOZ values are measured with inputs at the same level* as VCCI *for IIH and GND for IIL and IOZ.*

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

***Table 2-11* • Compatible I/O Standards for Different VREF Values**

VREF	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5V and 3.3V Outputs)
0.75 V	HSTL (Class I)

***Table 2-12* • Compatible I/O Standards for Different VCCI Values**

VCCI[1]	Compatible Standards	VREF
3.3 V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVCMOS 2.5 V, GTL+ 2.5 V, LVDS[2]	1.0
2.5 V	LVCMOS 2.5 V, SSTL 2 (Classes I and II), LVDS[2]	1.25
1.8 V	LVCMOS 1.8 V	N/A
1.5 V	LVCMOS 1.5 V, HSTL Class I	0.75

Notes:

1. *VCCI is used for both inputs and outputs*
2. *VCCI tolerance is ±5%*

Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Note that there are no tristated or bidirectional I/O buffers for differential standards.

Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users need to:

1. Instantiate an input buffer (with the required I/O standard)
2. Instantiate the DDR_REG macro (Figure 2-6)
3. Connect the output from the Input buffer to the input of the DDR macro

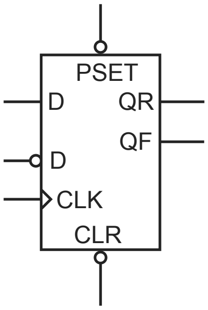


Figure 2-6 • **DDR Register**

Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required VCCI and VREF voltages for an I/O. The generic buffer macros require the LVTTL standard with slow slew rate and 24 mA-drive strength. LVTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (e.g. INBUF_LVDS) or a pair of differential outputs (e.g. OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (i.e. INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

Table 2-22 **• 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 4 (24 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		10.45		11.90		13.99	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		10.61		12.08		14.21	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		10.47		11.93		14.02	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.92		1.94		1.94	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.57		2.58		2.59	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

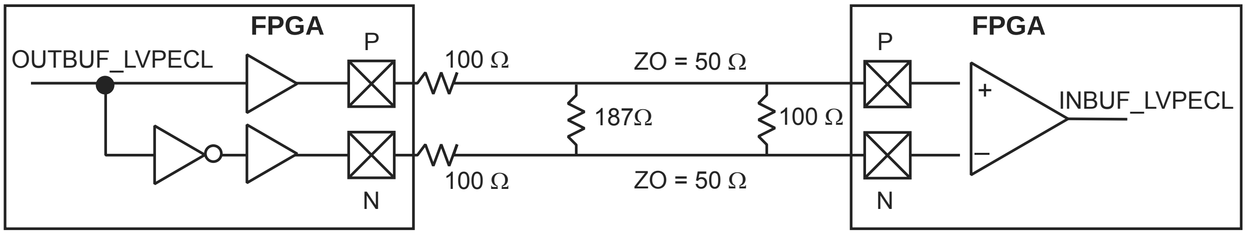


Figure 2-26 • **LVPECL Board-Level Implementation**

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS since the output voltage levels are different. Please note that the VOH levels are 200 mV below the standard LVPECL levels.

Table 2-59 • **DC Input and Output Levels**

	Min.		Typ.		Max.		
DC Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	3		3.3		3.6		V
VOH	1.8	2.11	1.92	2.28	2.13	2.41	V
VOL	0.96	1.27	1.06	1.43	1.3	1.57	V
VIH	1.49	2.72	1.49	2.72	1.49	2.72	V
VIL	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3		0.3		0.3		V

Table 2-60 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.6 – 0.3	1.6 + 0.3	1.6

*Note: * Measuring Point = VTRIP*

Timing Model and Waveforms

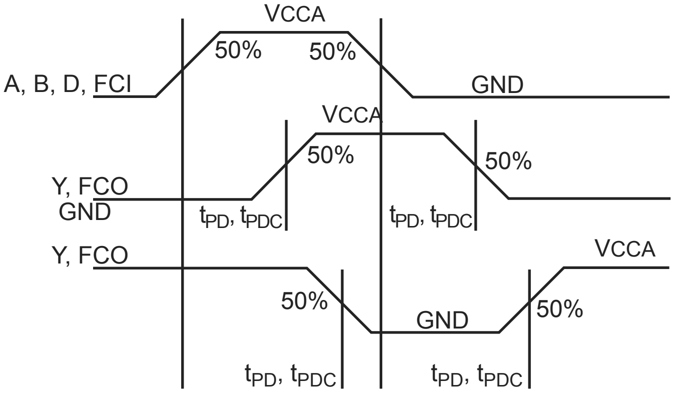


***Figure 2-28* • C-Cell Timing Model and Waveforms**

Timing Characteristics

***Table 2-62* • C-Cell**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays								
t_{PD}	Any input to output Y		0.74		0.84		0.99	ns
t_{PDC}	Any input to carry chain output (FCO)		0.57		0.64		0.76	ns
t_{PDB}	Any input through DB when one input is used		0.95		1.09		1.28	ns
t_{CCY}	Input to carry chain (FCI) to Y		0.61		0.69		0.82	ns
t_{CC}	Input to carry chain (FCI) to carry chain output (FCO)		0.08		0.09		0.11	ns

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

***Table 2-75* • AX125 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-76* • AX250 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t_{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is protected with highest level of security in the industry.

F™
FuseLock

Figure 2-69 • **FuseLock Logo**

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to the *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (Figure 2-31 on page 2-58). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer’s ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-108).

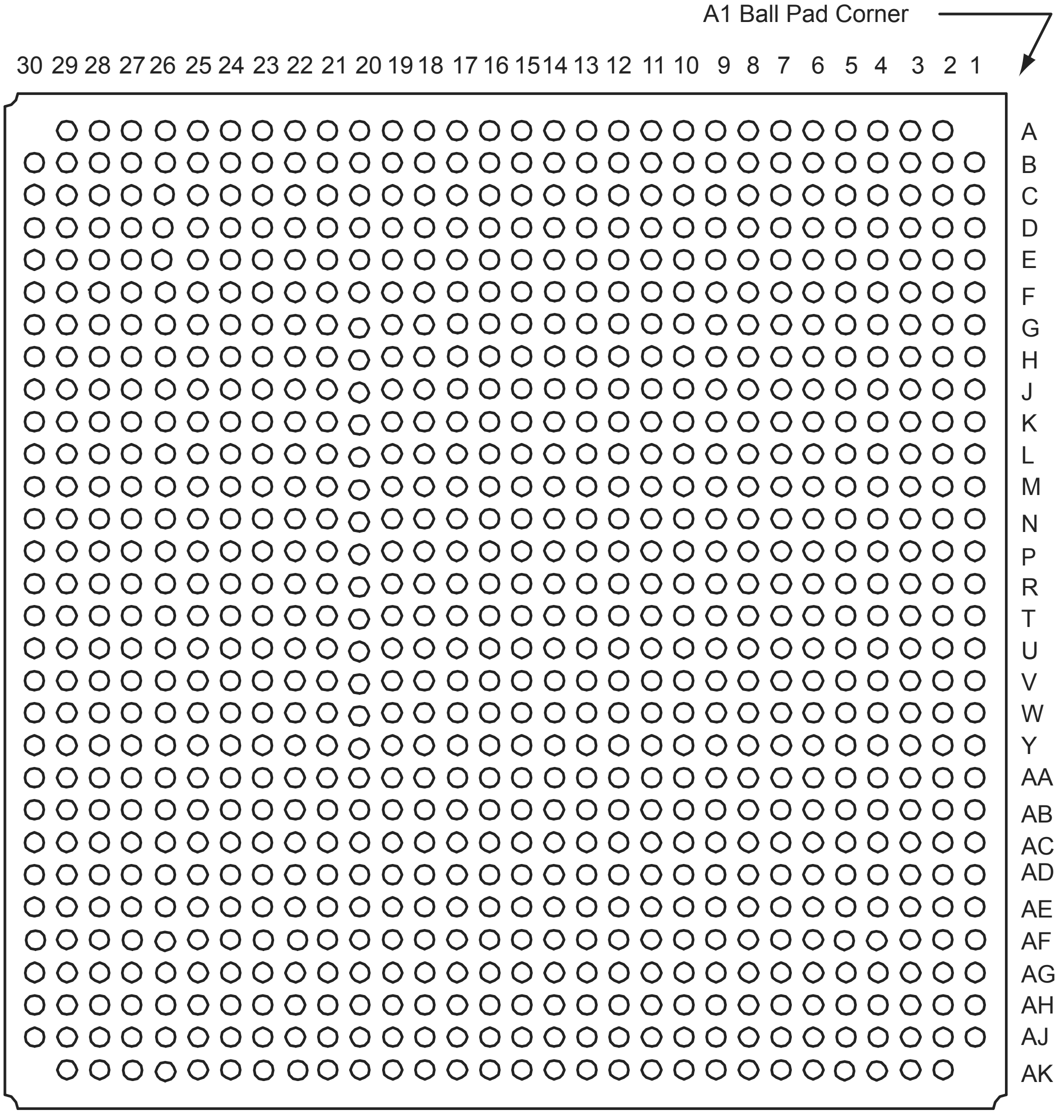
Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-7). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

FG324	
AX125 Function	**Pin Number**
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG676	
AX1000 Function	**Pin Number**
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

FG896



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG896	
AX1000 Function	**Pin Number**
IO51PB1F4	E21
IO52NB1F4	F22
IO52PB1F4	E22
IO53NB1F4	B25
IO53PB1F4	B24
IO54NB1F5	D24
IO54PB1F5	D23
IO55NB1F5	F23
IO55PB1F5	E23
IO56NB1F5	H21
IO56PB1F5	G21
IO57NB1F5	D25
IO57PB1F5	C25
IO58NB1F5	F24
IO58PB1F5	E24
IO59NB1F5	D26
IO59PB1F5	C26
IO60NB1F5	G23
IO60PB1F5	G22
IO61NB1F5	B27
IO61PB1F5	A27
IO62NB1F5	F25
IO62PB1F5	E25
IO63NB1F5	H23
IO63PB1F5	H22
Bank 2	
IO64NB2F6	K23
IO64PB2F6	J23
IO65NB2F6	J24
IO65PB2F6	H24
IO66NB2F6	H26
IO66PB2F6	H25
IO67NB2F6	G26
IO67PB2F6	G25
IO68NB2F6	K25
IO68PB2F6	K24
IO69NB2F6	F27
IO69PB2F6	E27
IO70NB2F6	J26
IO70PB2F6	J25
IO71NB2F6	H27
IO71PB2F6	G27
IO72NB2F6	J28
IO72PB2F6	H28
IO73NB2F6	G28
IO73PB2F6	F28
IO74NB2F7	L23
IO74PB2F7	L24
IO75NB2F7	L26
IO75PB2F7	K26
IO76NB2F7	M25
IO76PB2F7	L25
IO77NB2F7	K27
IO77PB2F7	J27
IO78NB2F7	M27
IO78PB2F7	L27
IO79NB2F7	K30
IO79PB2F7	K29
IO80NB2F7	M23
IO80PB2F7	M24
IO81NB2F7	M28
IO81PB2F7	L28
IO82NB2F7	N26
IO82PB2F7	M26
IO83NB2F7	N25
IO83PB2F7	N24
IO84NB2F7	N22
IO84PB2F7	N23
IO85NB2F8	M29
IO85PB2F8	L29
IO86NB2F8	N28
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IO89PB2F8	P27
IO90NB2F8	P22
IO90PB2F8	P23
IO91NB2F8	R26
IO91PB2F8	P26
IO92NB2F8	R24
IO92PB2F8	R25
IO93NB2F8	R29
IO93PB2F8	R30
IO94NB2F8	R22
IO94PB2F8	R23
IO95NB2F8	T27
IO95PB2F8	R27
Bank 3	
IO96NB3F9	T29
IO96PB3F9	T30
IO97NB3F9	U29
IO97PB3F9	U30
IO98NB3F9	T22
IO98PB3F9	T23
IO99NB3F9	U26
IO99PB3F9	T26
IO100NB3F9	U24
IO100PB3F9	T24
IO101NB3F9	V28
IO101PB3F9	U28
IO102NB3F9	U23
IO102PB3F9	U22

FG896	
AX2000 Function	**Pin Number**
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8

FG896	
AX2000 Function	**Pin Number**
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15

FG896	
AX2000 Function	**Pin Number**
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20

FG896	
AX2000 Function	**Pin Number**
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	**Pin Number**
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152	
AX2000 Function	Pin Number
GND	AK12
GND	AK17
GND	AK18
GND	AK23
GND	AK30
GND	AK5
GND	AL1
GND	AL11
GND	AL2
GND	AL24
GND	AL3
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL4
GND	AM1
GND	AM10
GND	AM15
GND	AM2
GND	AM20
GND	AM25
GND	AM3
GND	AM31
GND	AM32
GND	AM33
GND	AM34
GND	AM4
GND	AN1
GND	AN2
GND	AN26
GND	AN3
GND	AN31
GND	AN32
GND	AN33

FG1152	
AX2000 Function	Pin Number
GND	AN34
GND	AN4
GND	AN9
GND	AP13
GND	AP2
GND	AP22
GND	AP27
GND	AP3
GND	AP31
GND	AP32
GND	AP33
GND	AP4
GND	AP8
GND	B1
GND	B2
GND	B26
GND	B3
GND	B31
GND	B32
GND	B33
GND	B34
GND	B4
GND	B9
GND	C1
GND	C10
GND	C15
GND	C2
GND	C20
GND	C25
GND	C3
GND	C31
GND	C32
GND	C33
GND	C34
GND	C4

FG1152	
AX2000 Function	Pin Number
GND	D1
GND	D11
GND	D2
GND	D24
GND	D3
GND	D31
GND	D32
GND	D33
GND	D34
GND	D4
GND	E12
GND	E17
GND	E18
GND	E23
GND	E30
GND	E5
GND	F29
GND	F30
GND	F6
GND	G28
GND	G7
GND	H1
GND	H34
GND	J2
GND	J33
GND	K3
GND	K32
GND	L11
GND	L24
GND	L31
GND	L4
GND	M12
GND	M23
GND	M30
GND	M5

CQ352	
AX250 Function	Pin Number
IO64PB4F4	167
IO65NB4F4	170
IO65PB4F4	171
IO66NB4F4	164
IO66PB4F4	165
IO67NB4F4	160
IO67PB4F4	161
IO68NB4F4	158
IO68PB4F4	159
IO70NB4F4	154
IO70PB4F4	155
IO72NB4F4	152
IO72PB4F4	153
IO73NB4F4	146
IO73PB4F4	147
IO74NB4F4/CLKEN	142
IO74PB4F4/CLKEP	143
IO75NB4F4/CLKFN	136
IO75PB4F4/CLKFP	137
Bank 5	
IO76NB5F5/CLKGN	128
IO76PB5F5/CLKGP	129
IO77NB5F5/CLKHN	122
IO77PB5F5/CLKHP	123
IO78NB5F5	112
IO78PB5F5	113
IO79NB5F5	118
IO79PB5F5	119
IO80NB5F5	110
IO80PB5F5	111
IO82NB5F5	106
IO82PB5F5	107
IO84NB5F5	100
IO84PB5F5	101
IO85NB5F5	104

CQ352	
AX250 Function	Pin Number
IO85PB5F5	105
IO86NB5F5	98
IO86PB5F5	99
IO87NB5F5	94
IO87PB5F5	95
IO89NB5F5	92
IO89PB5F5	93
Bank 6	
IO90PB6F6	86
IO91NB6F6	84
IO91PB6F6	85
IO92NB6F6	78
IO92PB6F6	79
IO93NB6F6	82
IO93PB6F6	83
IO95NB6F6	76
IO95PB6F6	77
IO96NB6F6	72
IO96PB6F6	73
IO97NB6F6	70
IO97PB6F6	71
IO98NB6F6	66
IO98PB6F6	67
IO99NB6F6	64
IO99PB6F6	65
IO100NB6F6	60
IO100PB6F6	61
IO101NB6F6	58
IO101PB6F6	59
IO103NB6F6	54
IO103PB6F6	55
IO104NB6F6	52
IO104PB6F6	53
IO105NB6F6	48
IO105PB6F6	49

CQ352	
AX250 Function	Pin Number
IO106NB6F6	46
IO106PB6F6	47
Bank 7	
IO107NB7F7	40
IO107PB7F7	41
IO108NB7F7	42
IO108PB7F7	43
IO109NB7F7	36
IO109PB7F7	37
IO110NB7F7	34
IO110PB7F7	35
IO111NB7F7	30
IO111PB7F7	31
IO113NB7F7	28
IO113PB7F7	29
IO114NB7F7	24
IO114PB7F7	25
IO115NB7F7	22
IO115PB7F7	23
IO116NB7F7	18
IO116PB7F7	19
IO117NB7F7	16
IO117PB7F7	17
IO118NB7F7	12
IO118PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121NB7F7	6
IO121PB7F7	7
IO123NB7F7	4
IO123PB7F7	5
Dedicated I/O	
GND	1
GND	9
GND	15

CG624	
AX2000 Function	**Pin Number**
Bank 0	
IO00NB0F0	D7*
IO00PB0F0	E7*
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9*
IO13PB0F1	D8*
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11*
IO26PB0F2	B8*
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

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Revision	Changes	Page
Revision 8 (continued)	The following changes were made in the "FG676"(AX500) section: AE2, AE25 Change from NC to GND. AF2, AF25 Changed from GND to NC AB4, AF24, C1, C26 Changed from V_{CCDA} to V_{CCA} AD15 Change from V_{CCDA} to V_{COMPLE} AD17 Changed from V_{COMPLE} to V_{CCDA}	3-37
	In the "FG896" (AX2000) section, the AK28 changed from VCCIB5 to VCCIB4.	3-52
	The "CQ352" and "CG624" sections are new.	3-98, 3-115
Revision 7 (Advance v1.6)	All I/O FIFO capability was removed.	n/a
	Table 1 was updated.	i
	Figure 1-9 was updated.	1-7
	Figure 2-5 was updated.	2-16
	The "Using an I/O Register" section was updated.	2-16
	The AX250 and AX1000 descriptions were added to the "FG484"section.	3-21
Revision 6 (Advance v1.5)	Table 2-3 was updated.	2-2
	Figure 2-1 was updated.	2-8
	Figure 2-48 was updated.	2-75
	Figure 2-52 was updated.	2-82
Revision 5 (Advance v1.4)	In the "PQ208" table, pin 196 was missing, but it has been added in this version with a function of GND.	3-84
	The following pins in the "FG484" table for AX500 were changed: Pin G7 is GND/LP Pins AB8, C10, C11, C14, AB16 are NC.	3-21
	The "FG676" table was updated.	3-37
Revision 4 (Advance v1.3)	The "Device Resources" section was updated for the CS180.	ii
	The "Programmable Interconnect Element" and Figure 1-2 are new.	1-1 and 1-2
	The "CS180" table is new.	3-1
	The "PQ208" tables for the AX500 were updated. The following pins were not defined in the previous version: GND 21 IO106PB5F10/CLKHP 71 GND 136	3-84
Revision 3 (Advance v1.2)	Table 1, "Ordering Information", "Device Resources", and the Product Plan table were updated.	i, ii
	The following figures and tables were updated: Figure 1-3 Figure 1-8 (new) Table 2-3 Figure 2-2 Table 2-8 Figure 2-11	 1-2 1-6 2-2 2-9 2-12 2-23
	The "Design Environment" section was updated.	1-7
	The "Package Thermal Characteristics" was updated.	2-6