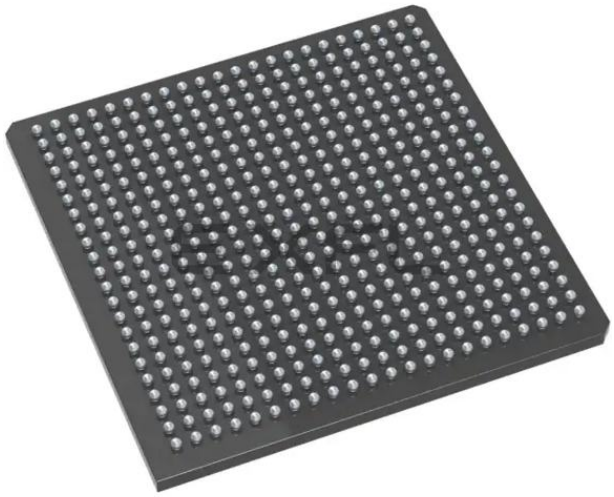


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

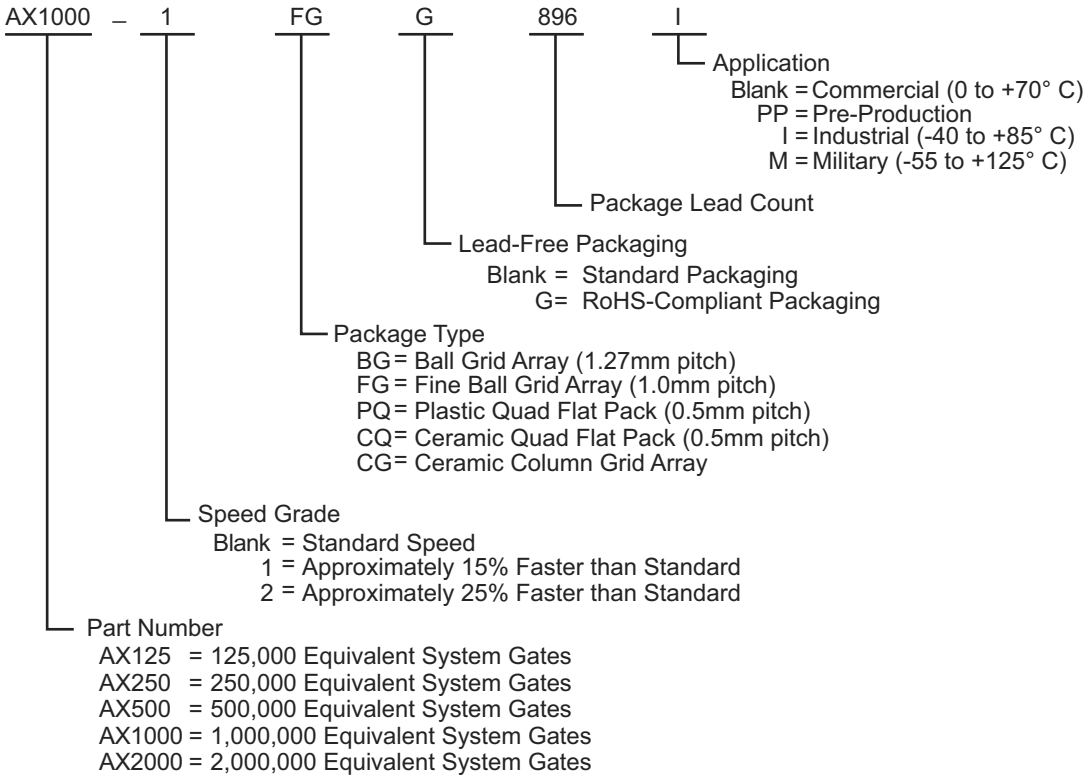
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	317
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-fg484m

Ordering Information



Device Resources

	User I/Os (Including Clock Buffers)				
Package	**AX125**	**AX250**	**AX500**	**AX1000**	**AX2000**
PQ208	–	115	115	–	–
CQ208	–	115	115	–	–
CQ256	–	–	–	–	136
FG256	138	138	–	–	–
FG324	168	–	–	–	–
CQ352	–	198	198	198	198
FG484	–	248	317	317	–
CG624	–	–	–	418	418
FG676	–	–	336	418	–
BG729	–	–	–	516	–
FG896	–	–	–	516	586
FG1152	–	–	–	–	684

Note: The FG256, FG324, and FG484 are footprint compatible with one another. The FG676, FG896, and FG1152 are also footprint compatible with one another.

The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).

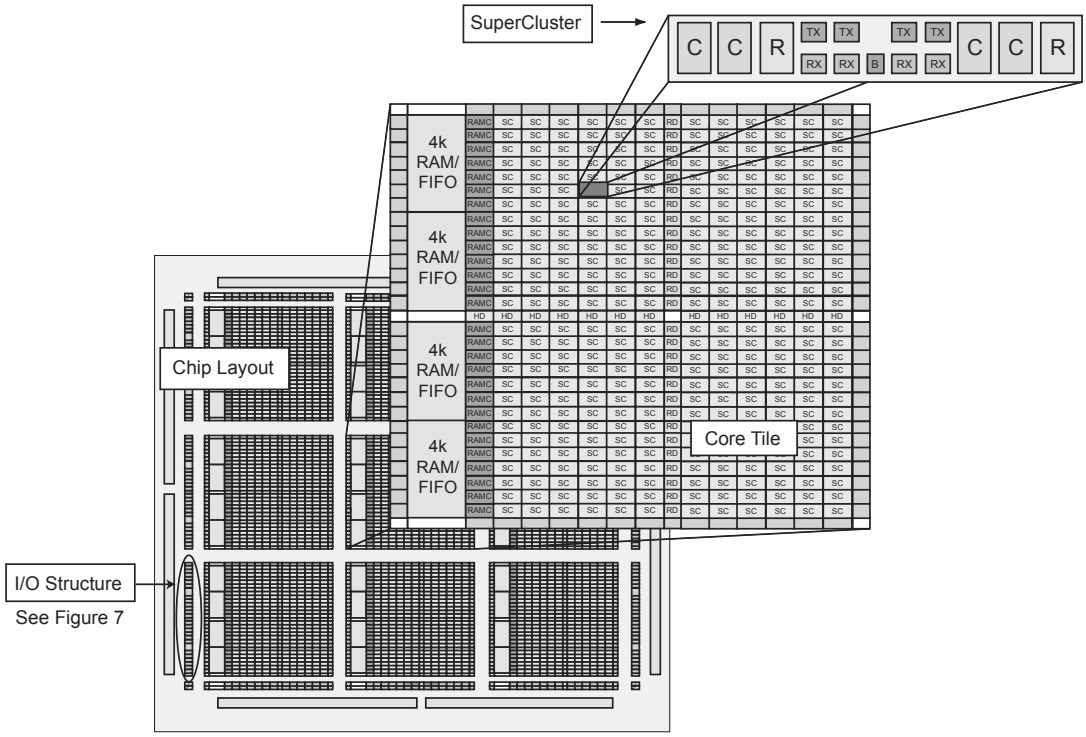


Figure 1-6 • **AX Device Architecture (AX1000 shown)**

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 4 (24 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		10.45		11.90		13.99	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		10.61		12.08		14.21	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		10.47		11.93		14.02	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.92		1.94		1.94	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.57		2.58		2.59	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength =3 (16 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		3.12		3.56		4.18	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.54		4.04		4.75	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.78		3.17		3.72	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.58		2.59		2.60	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

***Table 2-28* • 1.8V LVCMOS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.7 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVCMOS18 Output Module Timing								
t_{DP}	Input Buffer		3.26		3.71		4.37	ns
t_{PY}	Output Buffer		4.55		5.18		6.09	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.82		2.83		2.84	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.43		3.45		3.46	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.01		6.85		8.05	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.73		7.67		9.01	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Voltage-Referenced I/O Standards

GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It requires a differential amplifier input buffer and an Open Drain output buffer. The VCCI pin should be connected to 2.5 V or 3.3 V. Note that 2.5 V GTL+ is not supported across the full military temperature range.

***Table 2-37* • DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
N/A	VREF – 0.1	VREF + 0.1	N/A	0.6	NA	NA	NA

AC Loadings

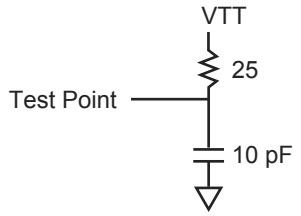


***Figure 2-19* • AC Test Loads**

***Table 2-38* • AC Waveforms, Measuring Points, and Capacitive Loads**

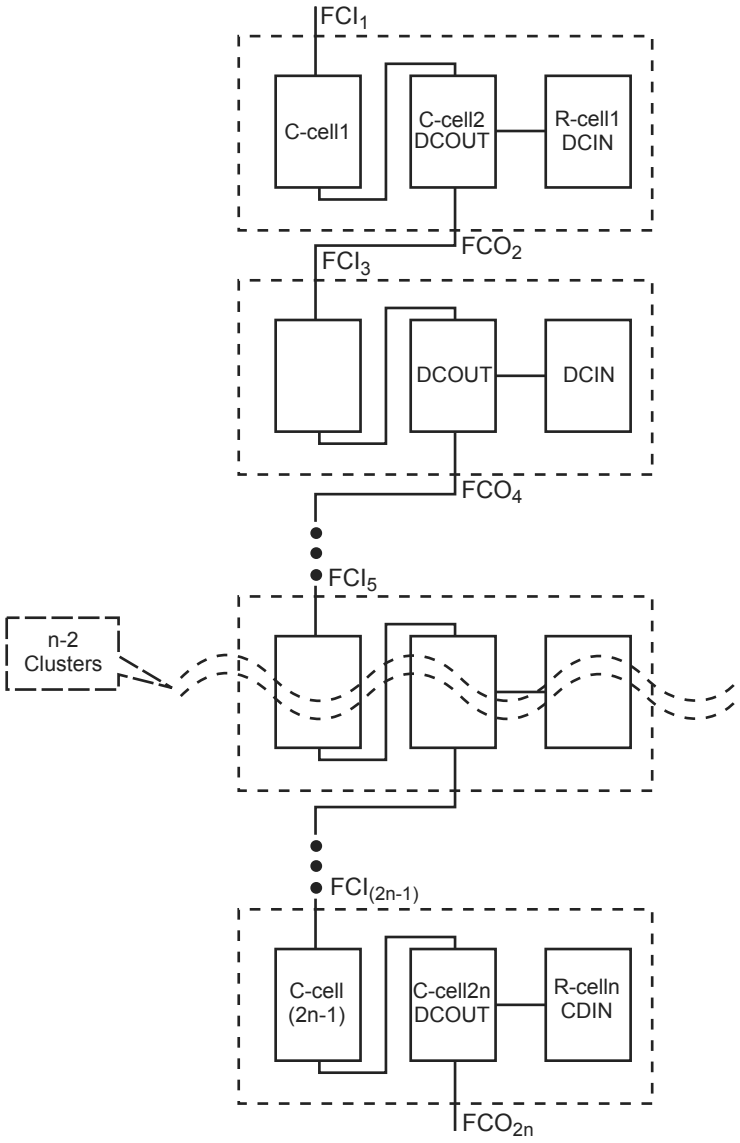
Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
VREF – 0.2	VREF + 0.2	VREF	1.0	10

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-39* • 2.5 V GTL+ I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5 V GTL+ I/O Module Timing								
t_{DP}	Input Buffer		1.71		1.95		2.29	ns
t_{PY}	Output Buffer		1.13		1.29		1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns



Note: The carry-chain sequence can end on either C-cell.

Figure 2-30 • **Carry-Chain Sequencing of C-Cells**

Timing Characteristics

Refer to Table 2-62 on page 2-55 for more information on carry-chain timing.

***Table 2-77* • AX500 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.31		2.63		3.09	ns
t_{RCKH}	Input High to Low		2.44		2.78		3.27	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-78* • AX1000 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-79* • AX2000 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-38).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-39).

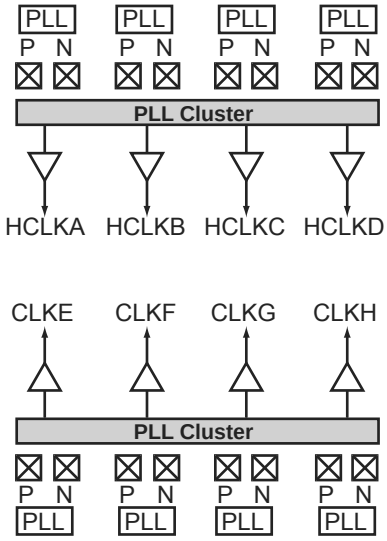


Figure 2-38 • **PLL Group**

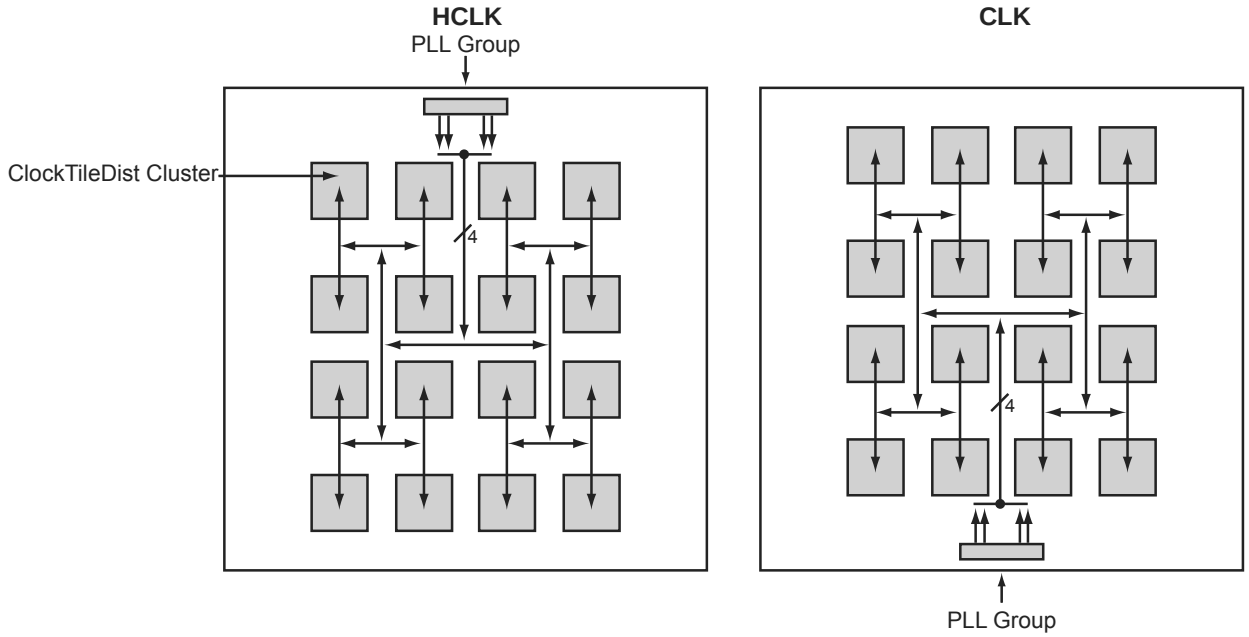


Figure 2-39 • **Example of HCLK and CLK Distributions on the AX2000**

CLK1 and CLK2

Both PLL outputs, CLK1 and CLK2, can be used to drive a global resource, an adjacent PLL RefCLK input, or a net in the FPGA core. Not all drive combinations are possible (Table 2-81).

***Table 2-81* • PLL General Connections Rules**

CLK1	CLK2
HCLK	HCLK
CLK	CLK
HCLK	Routed net output
Routed net output	HCLK
HCLK	NONE
NONE	HCLK
CLK	NONE
NONE	CLK

Note: The PLL outputs remain Low when REFCLK is constant (either Low or High).

Restrictions on CLK1 and CLK2

- When both are driving global resources, they must be driving the same *type* of global resource (i.e. either HCLK or CLK).
- Only one can drive a routed net at any given time.

Table 2-82 and Table 2-83 specify all the possible CLK1 and CLK2 connections for the north and south PLLs. HCLK1 and HCLK2 are used to denote the different HCLK networks when two are being driven at the same time by a single PLL (Note that HCLK1 is the primary clock resource associated with the PLL, and HCLK2 is the clock resource associated with the adjacent PLL). Likewise, CLK1 and CLK2 are used to denote the different CLK networks when two are being driven at the same time by a single PLL (Figure 2-48 on page 2-75).

***Table 2-82* • North PLL Connections**

CLK1	CLK2
HCLK1	Routed net
HCLK1	Unused
HCLK2	HCLK1
HCLK2	Routed net
HCLK2	Both HCLK1 and routed net
HCLK2	Unused
Unused	HCLK1
Unused	Routed net
Unused	Both HCLK1 and routed net
Unused	Unused
Routed net	HCLK1
Routed net	Unused
Both HCLK1 and HCLK2	Routed net
Both HCLK1 and HCLK2	Unused
Both HCLK1 and routed net	Unusable
Both HCLK2 and routed net	HCLK1
Both HCLK2 and routed net	Unused
HCLK1, HCLK2, and routed net	Unusable

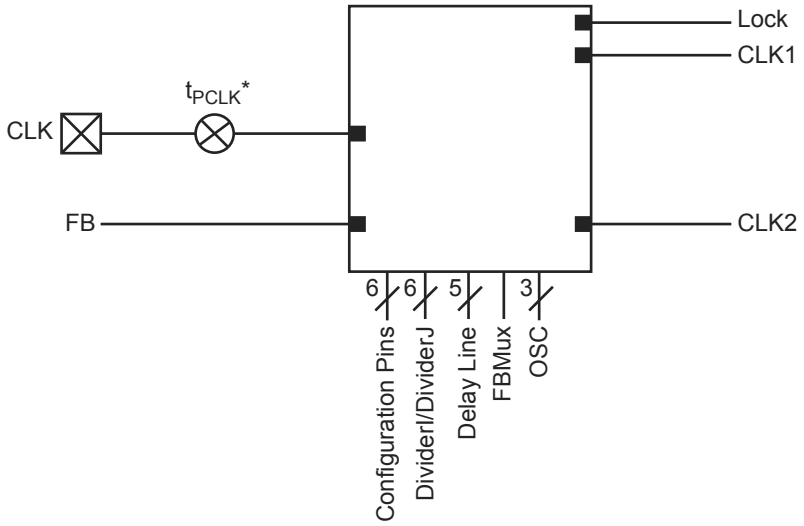
Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g.CLK1 driving HCLK1, and HCLK2 is not supported).

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model



Note: t_{PCLK} is the delay in the clock signal

Figure 2-52 • **PLL Model**

mode if desired. Please note, if the I/O bank is not disabled, differential I/Os belonging to the I/O bank will still consume normal power, even when operating in the low power mode.

The Axcelerator device will resume normal operation 10µs after the LP pin is pulled Low.

To further reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e. high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

In addition, any PLL in use can be powered down to further reduce power consumption. This can be done with the PowerDown pin driven Low. Driving this pin High restarts the PLL with the output clock(s) being stable once lock is restored.

JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the Table 2-103.

***Table 2-103* • JTAG Instruction Code**

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload / Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
Reserved	All others
Bypass	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low, asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1 kΩ resistor.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a VCCA and/or VCCDA voltage drop.

throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is protected with highest level of security in the industry.

Figure 2-69 • **FuseLock Logo**

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to the *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (Figure 2-31 on page 2-58). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-108).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-7). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

FG484	
AX250 Function	**Pin Number**
IO104PB6F6	N4
IO105NB6F6	M5
IO105PB6F6	N5
IO106NB6F6	M3
IO106PB6F6	N3
Bank 7	
IO107NB7F7	M2
IO107PB7F7	N1
IO108NB7F7	L3
IO108PB7F7	L2
IO109NB7F7	K2
IO109PB7F7	K1
IO110NB7F7	K5
IO110PB7F7	L5
IO111NB7F7	K6
IO111PB7F7	L6
IO112NB7F7	K4
IO112PB7F7	K3
IO113NB7F7	K7
IO113PB7F7	L7
IO114NB7F7	H1
IO114PB7F7	J1
IO115NB7F7	H2
IO115PB7F7	J2
IO116NB7F7	H4
IO116PB7F7	J4
IO117NB7F7	H5
IO117PB7F7	J5
IO118NB7F7	F2
IO118PB7F7	G2
IO119NB7F7	H6
IO119PB7F7	J6
IO120NB7F7	F1
IO120PB7F7	G1
IO121NB7F7	F4
IO121PB7F7	G4

FG484	
AX250 Function	**Pin Number**
IO122NB7F7	G5
IO122PB7F7	G6
IO123NB7F7	F5
IO123PB7F7	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14

FG484	
AX250 Function	**Pin Number**
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	A17
NC	A18

FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9

FG676	
AX500 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21

FG676	
AX500 Function	Pin Number
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

FG676	
AX1000 Function	**Pin Number**
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11

FG676	
AX1000 Function	**Pin Number**
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11

FG676	
AX1000 Function	**Pin Number**
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25

FG896	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8

FG896	
AX2000 Function	Pin Number
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15

FG896	
AX2000 Function	Pin Number
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20

PQ208	
AX250 Function	**Pin Number**
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	**Pin Number**
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX250 Function	**Pin Number**
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15