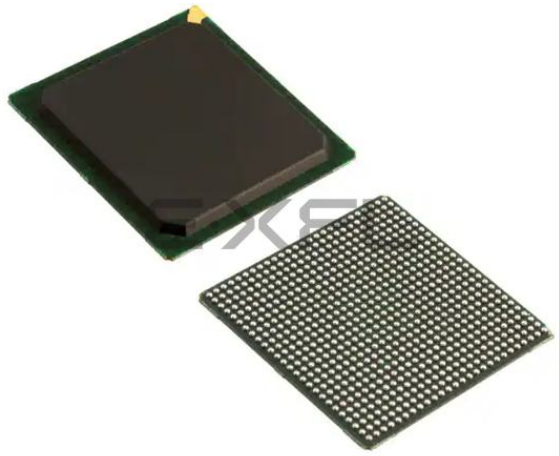

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	418
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax1000-fg676i

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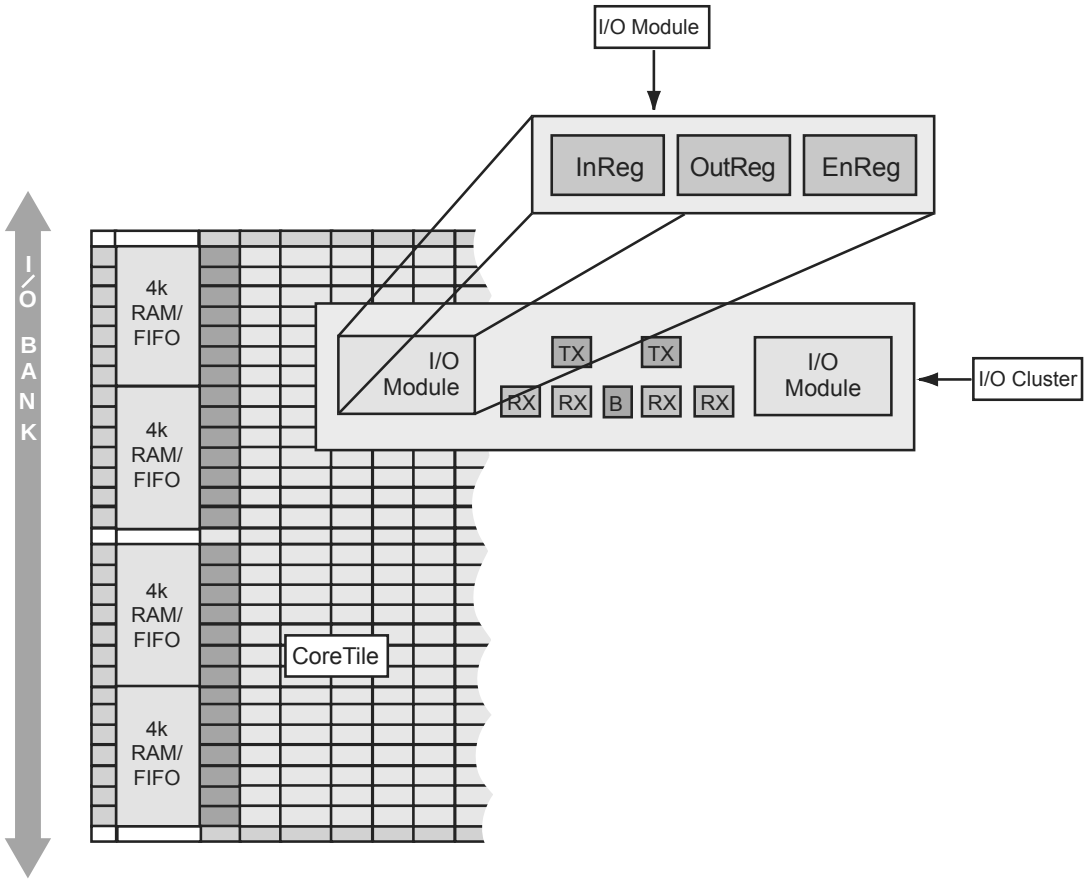


Figure 1-7 • **I/O Cluster Arrangement**

Routing

The AX hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together (Figure 1-8 on page 1-6). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

FastConnects provide high-performance, horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the FCO output of one two-bit, C-cell carry logic to the FCI input of the two-bit, C-cell carry logic of the SuperCluster below it. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. Over the SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns, respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north-to-south and east-to-west. These tracks are composed of highway routing that extend the entire length of the device (segmented at core tile boundaries) as well as segmented routing of varying lengths.

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 4 (24mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		2.99		3.41		4.01	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.49		2.51		2.51	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.59		2.95		3.46	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.56		4.06		4.77	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

***Table 2-25* • 2.5V LVCMOS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVCMOS25 I/O Module Timing								
t_{DP}	Input Buffer		1.95		2.22		2.61	ns
t_{PY}	Output Buffer		3.29		3.74		4.40	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.48		2.50		2.51	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.48		2.50		2.51	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		5.74		6.54		7.69	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.60		7.51		8.83	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

PLLRCLK and PLLHCLK

PLLRCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 2-44).

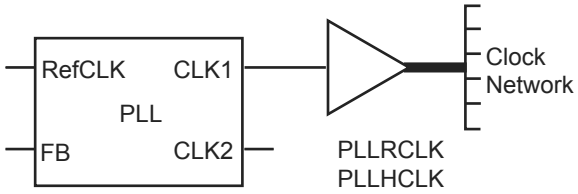


Figure 2-44 • **PLLRCLK and PLLHCLK**

Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc. (Figure 2-45).

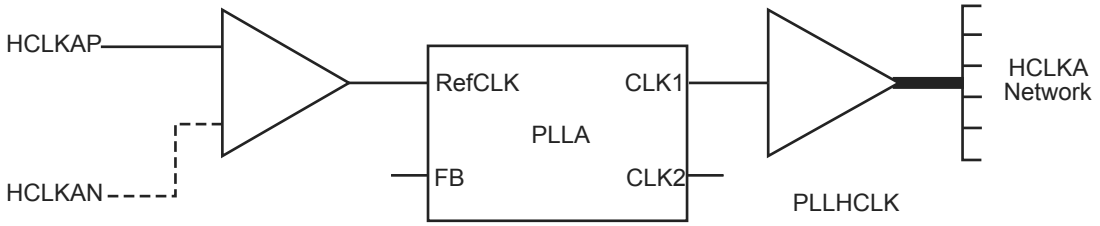


Figure 2-45 • **Example of HCLKA Driven from a PLL with External Clock Source**

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 2-46).

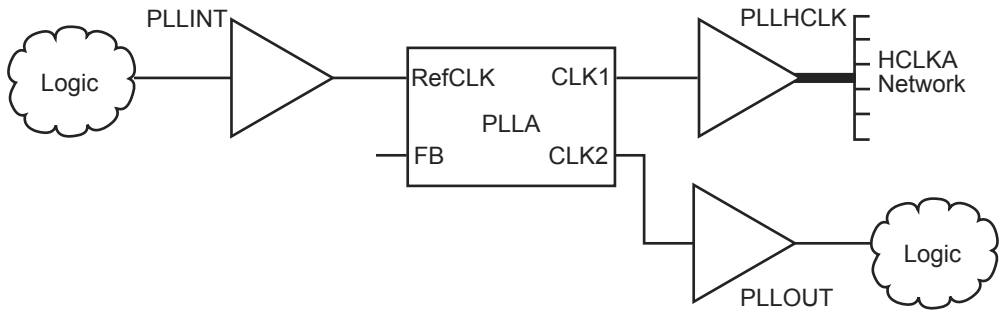


Figure 2-46 • **Example of PLLINT and PLLOUT Usage**

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

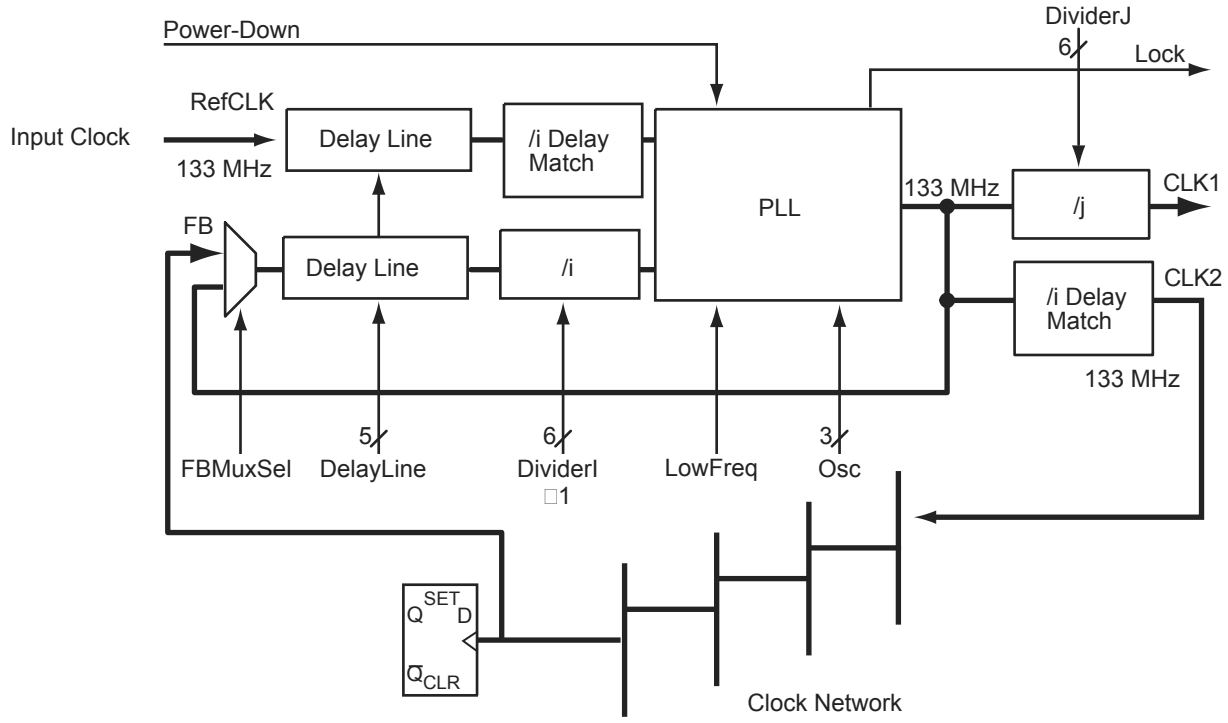


Figure 2-56 • **Using the PLL for Clock Deskewing**

Timing Characteristics

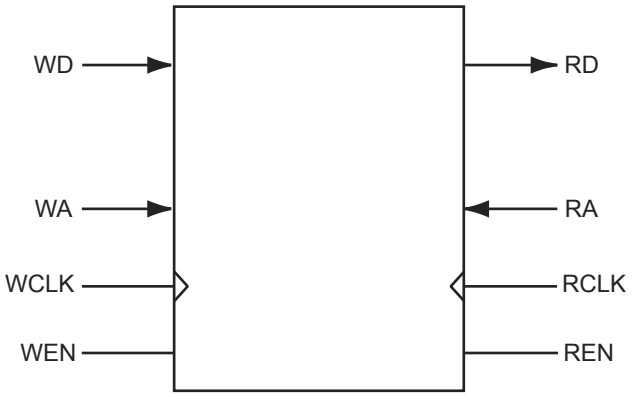


Figure 2-58 • **SRAM Model**

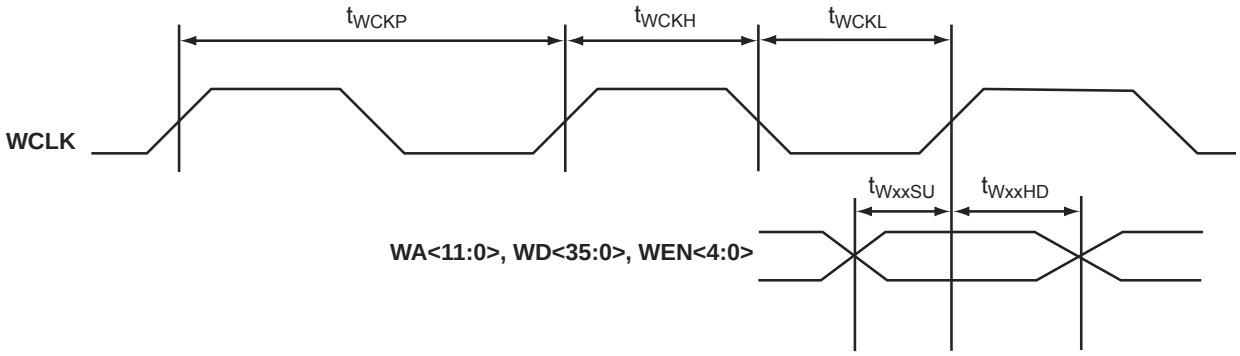


Figure 2-59 • **RAM Write Timing Waveforms**

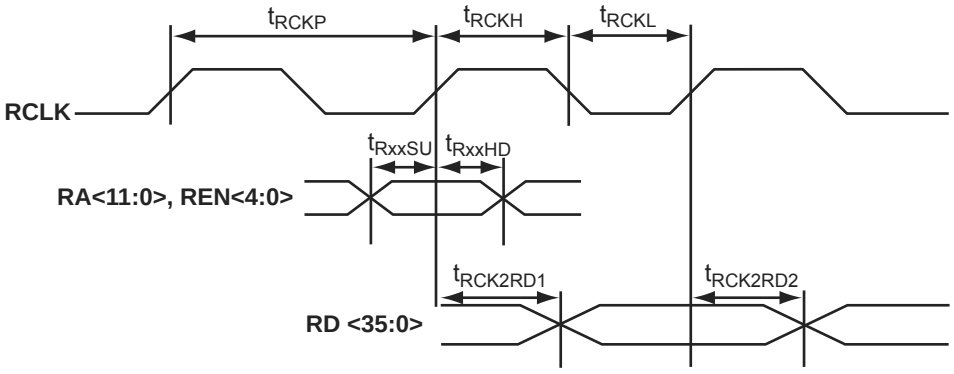


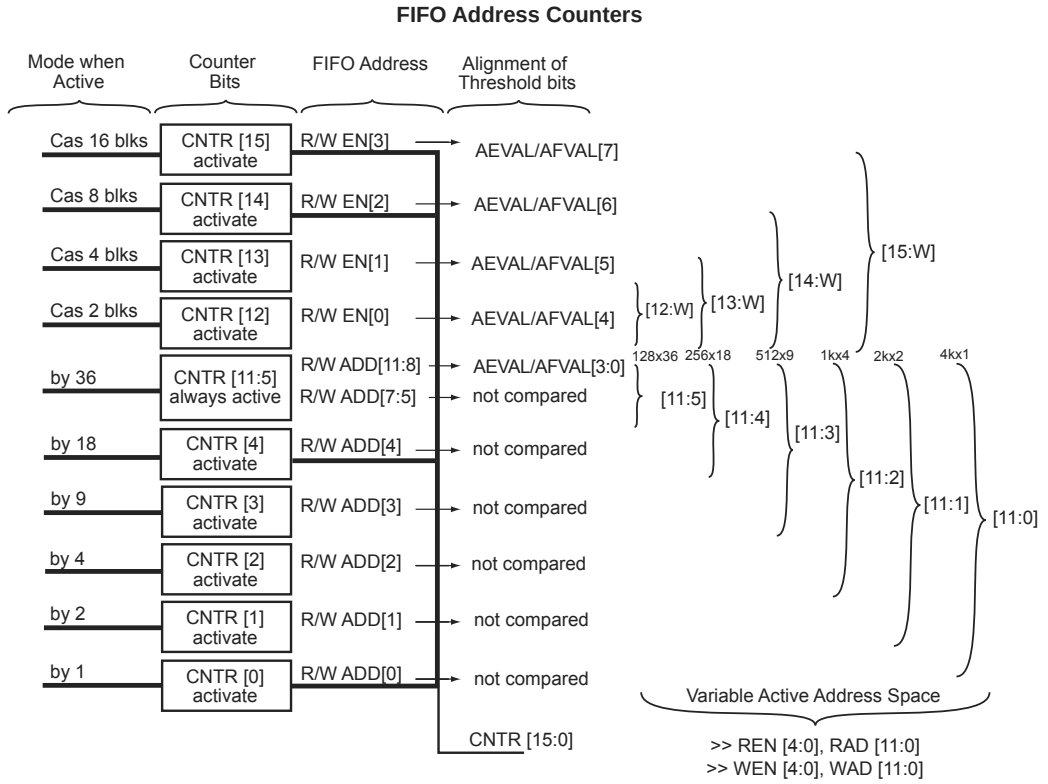
Figure 2-60 • **RAM Read Timing Waveforms**

FIFO Flag Logic

The FIFO is user configurable into various DEPTHs and WIDTHs. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.



Note: Inactive counter bits are set to zero.

Figure 2-62 • **FIFO Address Counters**

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

Table 2-94 • **FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

FG256	
AX250 Function	**Pin Number**
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A11
VCCDA	A2
VCCDA	C13
VCCDA	D9
VCCDA	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCDA	R11
VCCDA	R5
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10

FG256	
AX250 Function	**Pin Number**
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

FG484	
AX250 Function	**Pin Number**
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13

FG484	
AX250 Function	**Pin Number**
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG484	
AX1000 Function	Pin Number
IO167PB5F15	AA12
IO169NB5F15	AA9
IO169PB5F15	AA10
IO170NB5F15	AB9
IO170PB5F15	AB10
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	Y8
IO172PB5F16	Y9
IO173NB5F16	U8
IO173PB5F16	U9
IO174NB5F16	AA7
IO174PB5F16	AA8
IO175NB5F16	AB5
IO175PB5F16	AB6
IO176NB5F16	AA5
IO176PB5F16	AA6
IO177NB5F16	AA4
IO177PB5F16	AB4
IO178NB5F16	Y6
IO178PB5F16	Y7
IO179NB5F16	T7
IO179PB5F16	T8
IO180NB5F16	W6
IO180PB5F16	W7
IO181NB5F17	Y4
IO181PB5F17	Y5
IO184NB5F17	AB7
IO187NB5F17	V3
IO187PB5F17	W3
IO188NB5F17	V4
IO188PB5F17	W5
IO192NB5F17	V6
IO192PB5F17	V7
Bank 6	

FG484	
AX1000 Function	Pin Number
IO194NB6F18	V2
IO194PB6F18	W2
IO195NB6F18	U5
IO195PB6F18	T5
IO200NB6F18	T4
IO200PB6F18	U4
IO201NB6F18	P6
IO201PB6F18	R6
IO203NB6F19	U2
IO204NB6F19	T3
IO204PB6F19	U3
IO205NB6F19	P5
IO205PB6F19	R5
IO208NB6F19	V1
IO208PB6F19	W1
IO209NB6F19	P7
IO209PB6F19	R7
IO212NB6F19	P4
IO212PB6F19	R4
IO214NB6F20	P3
IO214PB6F20	R3
IO215NB6F20	M6
IO215PB6F20	N6
IO216NB6F20	R2
IO216PB6F20	T2
IO217NB6F20	T1
IO217PB6F20	U1
IO219NB6F20	M5
IO219PB6F20	N5
IO220NB6F20	P1
IO220PB6F20	R1
IO221NB6F20	N2
IO221PB6F20	P2
IO222NB6F20	M3
IO222PB6F20	N3

FG484	
AX1000 Function	Pin Number
IO223NB6F20	M7
IO223PB6F20	N7
IO224NB6F20	M4
IO224PB6F20	N4
Bank 7	
IO225NB7F21	M2
IO225PB7F21	N1
IO226NB7F21	K2
IO226PB7F21	K1
IO228NB7F21	L3
IO228PB7F21	L2
IO229NB7F21	K5
IO229PB7F21	L5
IO230NB7F21	H1
IO230PB7F21	J1
IO231NB7F21	H2
IO231PB7F21	J2
IO232NB7F21	K4
IO232PB7F21	K3
IO233NB7F21	K6
IO233PB7F21	L6
IO234NB7F21	F1
IO234PB7F21	G1
IO235NB7F21	F2
IO235PB7F21	G2
IO236NB7F22	H3
IO236PB7F22	J3
IO237NB7F22	K7
IO237PB7F22	L7
IO241NB7F22	H6
IO241PB7F22	J6
IO242NB7F22	H4
IO242PB7F22	J4
IO243NB7F22	H5
IO243PB7F22	J5

FG676	
AX1000 Function	**Pin Number**
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26
IO73PB2F6	D26
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23

FG676	
AX1000 Function	**Pin Number**
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
Bank 3	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24
IO100NB3F9	R22
IO100PB3F9	P22
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25

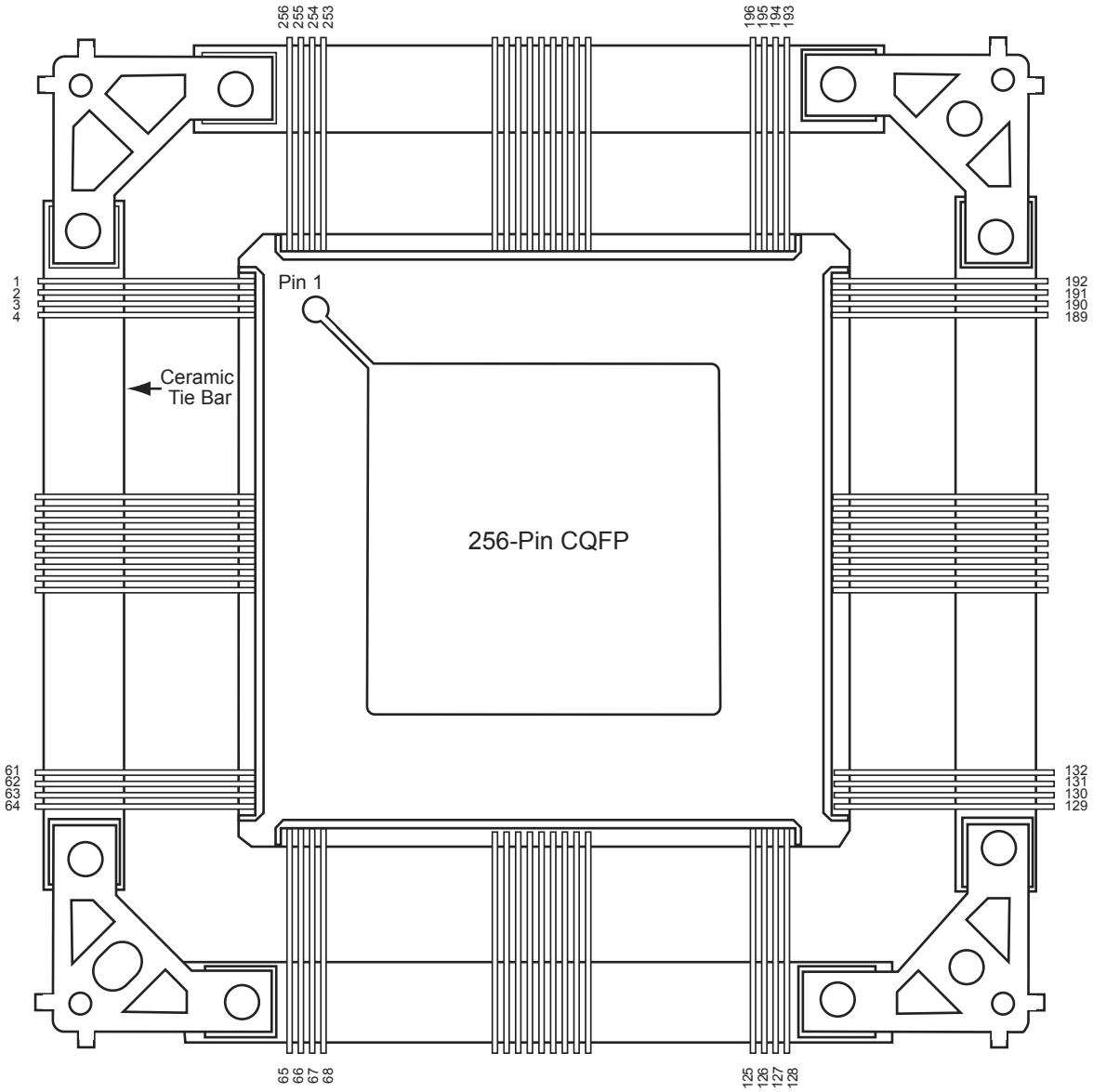
FG676	
AX1000 Function	**Pin Number**
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
Bank 4	
IO129NB4F12	AB21

FG896	
AX1000 Function	Pin Number
IO103NB3F9	V27
IO103PB3F9	U27
IO104NB3F9	W29
IO104PB3F9	V29
IO105NB3F9	Y28
IO105PB3F9	W28
IO106NB3F9	V25
IO106PB3F9	U25
IO107NB3F10	W26
IO107PB3F10	V26
IO108NB3F10	W24
IO108PB3F10	V24
IO109NB3F10	Y27
IO109PB3F10	W27
IO110NB3F10	V23
IO110PB3F10	V22
IO111NB3F10	AA29
IO111PB3F10	Y29
IO112NB3F10	Y25
IO112PB3F10	W25
IO113NB3F10	AB27
IO113PB3F10	AA27
IO114NB3F10	Y23
IO114PB3F10	W23
IO115NB3F10	AA26
IO115PB3F10	Y26
IO116NB3F10	AC28
IO116PB3F10	AB28
IO117NB3F10	AE29
IO117PB3F10	AD29
IO118NB3F11	AE28
IO118PB3F11	AD28
IO119NB3F11	AD27
IO119PB3F11	AC27
IO120NB3F11	AA24

FG896	
AX1000 Function	Pin Number
IO120PB3F11	Y24
IO121NB3F11	AB25
IO121PB3F11	AA25
IO122NB3F11	AC26
IO122PB3F11	AB26
IO123NB3F11	AG28
IO123PB3F11	AF28
IO124NB3F11	AB23
IO124PB3F11	AA23
IO125NB3F11	AF27
IO125PB3F11	AE27
IO126NB3F11	AD25
IO126PB3F11	AC25
IO127NB3F11	AE26
IO127PB3F11	AD26
IO128NB3F11	AC24
IO128PB3F11	AB24
Bank 4	
IO129NB4F12	AD23
IO129PB4F12	AC23
IO130NB4F12	AK26
IO130PB4F12	AK27
IO131NB4F12	AF24
IO131PB4F12	AF25
IO132NB4F12	AG25
IO132PB4F12	AG26
IO133NB4F12	AD22
IO133PB4F12	AC22
IO134NB4F12	AE23
IO134PB4F12	AE24
IO135NB4F12	AH24
IO135PB4F12	AH25
IO136NB4F12	AJ25
IO136PB4F12	AJ26
IO137NB4F12	AD21

FG896	
AX1000 Function	Pin Number
IO137PB4F12	AC21
IO138NB4F12	AK24
IO138PB4F12	AK25
IO139NB4F13	AE21
IO139PB4F13	AE22
IO140NB4F13	AG23
IO140PB4F13	AG24
IO141NB4F13	AF22
IO141PB4F13	AF23
IO142NB4F13	AJ23
IO142PB4F13	AJ24
IO143NB4F13	AD19
IO143PB4F13	AD20
IO144NB4F13	AG21
IO144PB4F13	AG22
IO145NB4F13	AE19
IO145PB4F13	AE20
IO146NB4F13	AF20
IO146PB4F13	AF21
IO147NB4F13	AC19
IO147PB4F13	AC20
IO148NB4F13	AH22
IO148PB4F13	AH23
IO149NB4F13	AC18
IO149PB4F13	AB18
IO150NB4F13	AK21
IO150PB4F13	AJ21
IO151NB4F13	AE18
IO151PB4F13	AD18
IO152NB4F14	AJ20
IO152PB4F14	AK20
IO153NB4F14	AG19
IO153PB4F14	AG20
IO154NB4F14	AH19
IO154PB4F14	AH20

CQ256



Note

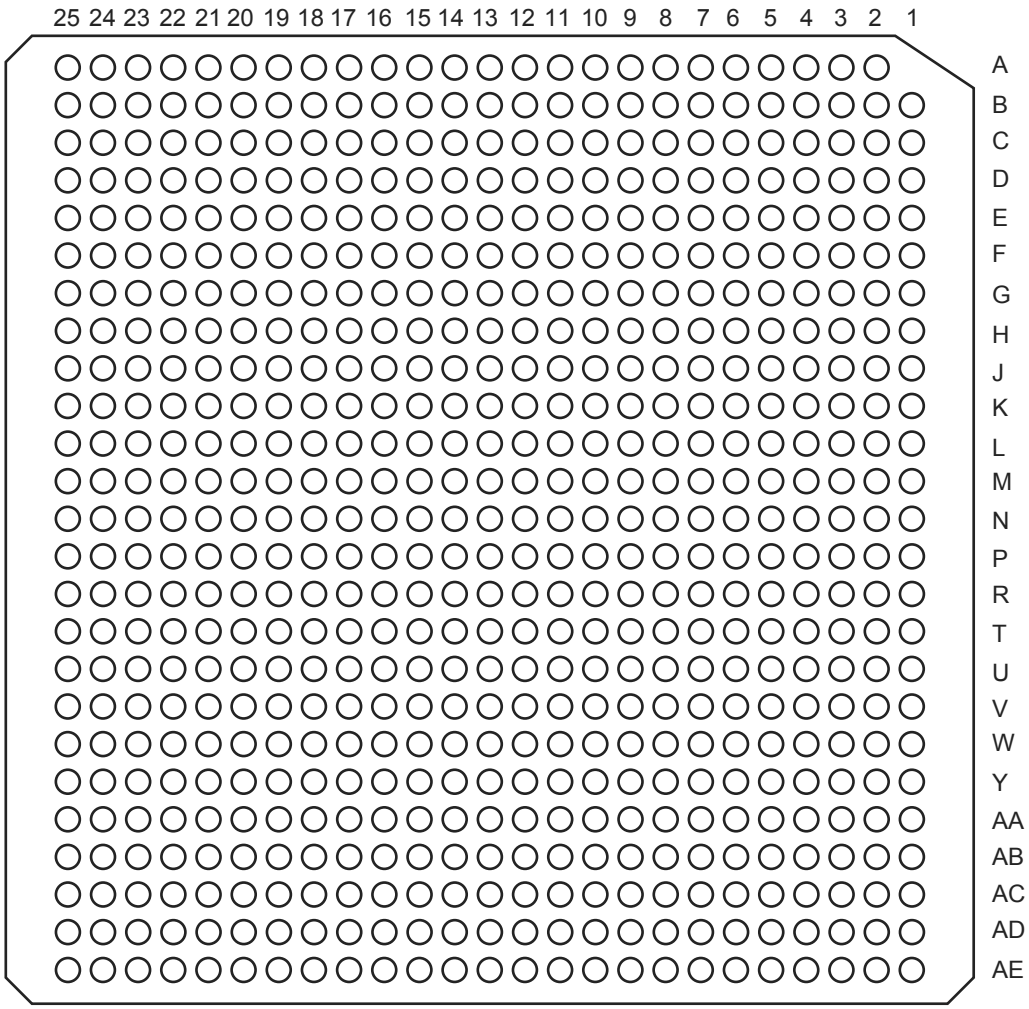
For Package Manufacturing and Environmental information, visit the Resource center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CQ352	
AX2000 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX2000 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114

CQ352	
AX2000 Function	Pin Number
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	91
VCCDA	116
VCCDA	117
VCCDA	130
VCCDA	131
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	174
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	268
VCCDA	293
VCCDA	294
VCCDA	307
VCCDA	308
VCCDA	309
VCCDA	327
VCCDA	328

CG624



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

CG624	
AX1000 Function	**Pin Number**
VCCA	U17
VCCA	U9
VCCA	Y4
VCCDA	A12
VCCDA	AA13
VCCDA	AA15
VCCDA	AA7
VCCDA	AC11
VCCDA	AD11
VCCDA	AE17
VCCDA	B15
VCCDA	C15
VCCDA	C6
VCCDA	D13
VCCDA	E13
VCCDA	E19
VCCDA	G5
VCCDA	N21
VCCDA	N5
VCCDA	W21
VCCIB0	A3
VCCIB0	B3
VCCIB0	C4
VCCIB0	D5
VCCIB0	J10
VCCIB0	J11
VCCIB0	K12
VCCIB1	A23
VCCIB1	B23
VCCIB1	C22
VCCIB1	D21
VCCIB1	J15
VCCIB1	J16
VCCIB1	K14
VCCIB2	C24
VCCIB2	C25

CG624	
AX1000 Function	**Pin Number**
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3

CG624	
AX1000 Function	**Pin Number**
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

CG624	
AX2000 Function	**Pin Number**
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*