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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	18144
Number of Logic Elements/Cells	-
Total RAM Bits	165888
Number of I/O	516
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax1000-fg896i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 kΩ). These are weak transistors with the gates tied on, so the on resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors; they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8 mA, 12 mA, 16 mA, or 24 mA – that can be specified in Designer.[5]

Table 2-14 **• Bank-Wide Delay Values**

Bits Setting	Delay (ns)	Bits Setting	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

5. *These values are minimum drive strengths.*

I/O Standard Electrical Specifications

Table 2-18 **• Input Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	VIN = 0, f = 1.0 MHz		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	VIN = 0, f = 1.0 MHz		10	pF

Table 2-19 **• I/O Input Rise Time and Fall Time***

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTL	No Requirement	50 ns
LVCMOS 2.5V	No Requirement	50 ns
LVCMOS 1.8V	No Requirement	50 ns
LVCMOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

Note: **Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

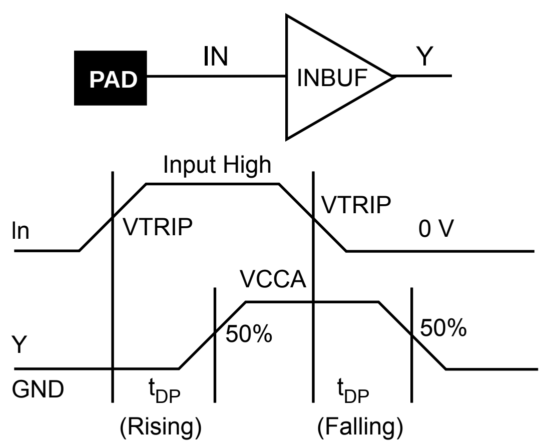


Figure 2-9 **• Input Buffer Delays**

Table 2-72 **• AX500 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		2.35		2.68		3.15	ns
t_{HCKH}	Input High to Low		2.44		2.79		3.27	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-73 **• AX1000 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-74 **• AX2000 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-75 **• AX125 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-76 **• AX250 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t_{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-77 • **AX500 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.31		2.63		3.09	ns
t_{RCKH}	Input High to Low		2.44		2.78		3.27	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-78 • **AX1000 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-79 • **AX2000 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Note that the RAM blocks employ little-endian byte order for read and write operations.

Table 2-88 • **RAM Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 2-64). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 2-64).

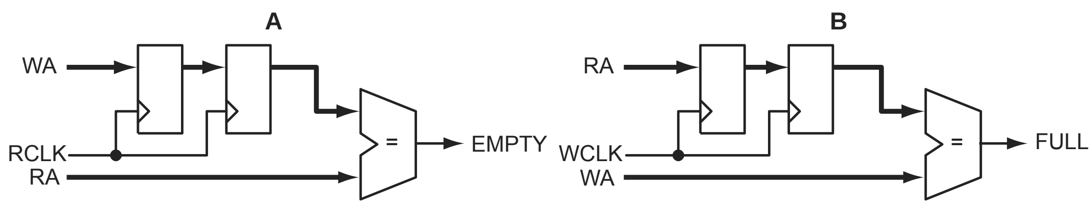


Figure 2-64 • **Overflow and Underflow Control**

FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 2-96.

Table 2-96 • **FIFO Width Configurations**

WIDTH(2:0)	W x D
000	1 x 4k
001	2 x 2k
010	4 x 1k
011	9 x 512
100	18 x 256
101	36 x 128
11x	reserved

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-86 on page 2-87 describes the FIFO depth options for various data width and memory blocks.

Interface

Figure 2-65 on page 2-99 shows a logic block diagram of the Axcelerator FIFO module.

Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using SmartGen, the user only needs to specify the depth and width of the necessary FIFO blocks. SmartGen automatically configures these blocks to optimize performance.

FG256-Pin FBGA	
AX125 Function	Pin Number
Bank 6	
IO60NB6F6	L4
IO60PB6F6	M4
IO61NB6F6	L3
IO61PB6F6	M3
IO63NB6F6	P2
IO63PB6F6	N2
IO64NB6F6	J4
IO64PB6F6	K4
IO65NB6F6	N1
IO65PB6F6	P1
IO67NB6F6	L2
IO67PB6F6	M2
IO69NB6F6	L1
IO69PB6F6	M1
IO70NB6F6	J3
IO70PB6F6	K3
IO71NB6F6	J2
IO71PB6F6	K2
Bank 7	
IO72NB7F7	J1
IO72PB7F7	K1
IO73NB7F7	G2
IO73PB7F7	H2
IO74NB7F7	G3
IO74PB7F7	H3
IO75NB7F7	E1
IO75PB7F7	F1
IO76NB7F7	G1
IO77NB7F7	E2
IO77PB7F7	F2
IO78NB7F7	G4
IO78PB7F7	H4
IO79NB7F7	C1
IO79PB7F7	D1

FG256-Pin FBGA	
AX125 Function	Pin Number
IO81NB7F7	C2
IO81PB7F7	B1
IO82NB7F7	D2
IO82PB7F7	D3
IO83NB7F7	E3
IO83PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6

FG256-Pin FBGA	
AX125 Function	Pin Number
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
NC	A11
NC	R11
NC	R5
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6

FG484	
AX500 Function	Pin Number
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX500 Function	Pin Number
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

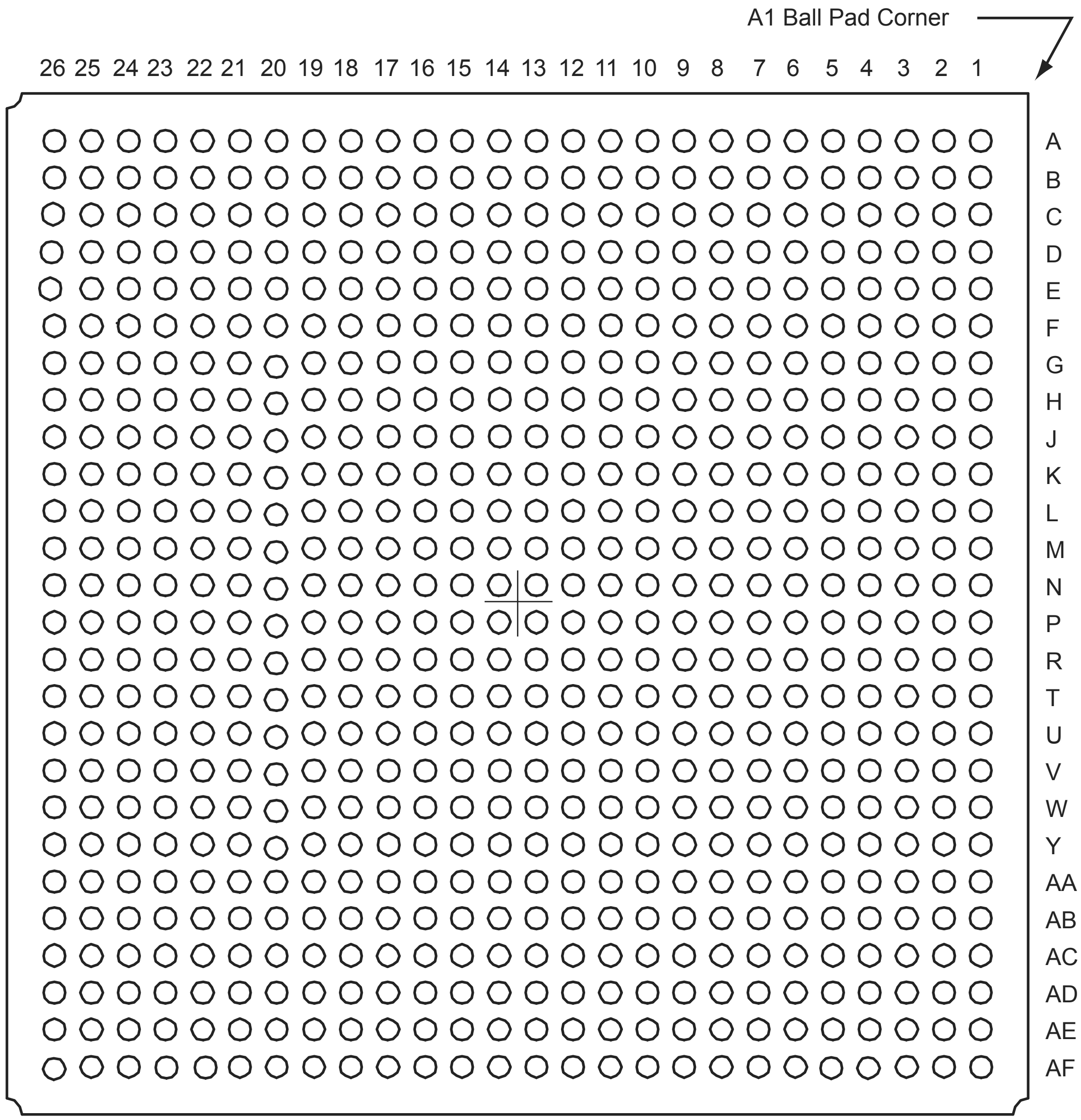
FG484	
AX500 Function	Pin Number
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG484	
AX1000 Function	Pin Number
IO87PB2F8	H20
IO88NB2F8	L18
IO88PB2F8	K18
IO89NB2F8	K19
IO89PB2F8	J19
IO90NB2F8	J21
IO90PB2F8	H21
IO91NB2F8	J22
IO91PB2F8	H22
IO93NB2F8	K21
IO93PB2F8	K22
IO94NB2F8	L20
IO94PB2F8	K20
IO95NB2F8	M21
IO95PB2F8	L21
Bank 3	
IO96NB3F9	N16
IO96PB3F9	M16
IO97NB3F9	M19
IO97PB3F9	L19
IO98NB3F9	P22
IO98PB3F9	N22
IO99NB3F9	N20
IO99PB3F9	M20
IO100NB3F9	N17
IO100PB3F9	M17
IO101NB3F9	P21
IO101PB3F9	N21
IO103NB3F9	R20
IO103PB3F9	P20
IO104NB3F9	N18
IO104PB3F9	N19
IO105NB3F9	T22
IO105PB3F9	R22
IO106NB3F9	R17

FG484	
AX1000 Function	Pin Number
IO106PB3F9	P17
IO107NB3F10	T21
IO107PB3F10	R21
IO110NB3F10	V22
IO110PB3F10	U22
IO113NB3F10	V21
IO113PB3F10	U21
IO114NB3F10	P18
IO114PB3F10	P19
IO116PB3F10	R19
IO117NB3F10	U20
IO117PB3F10	T20
IO118NB3F11	T18
IO118PB3F11	R18
IO121NB3F11	U19
IO121PB3F11	T19
IO124NB3F11	R16
IO124PB3F11	P16
IO127NB3F11	W21
IO127PB3F11	W22
Bank 4	
IO129PB4F12	AB17
IO132NB4F12	Y19
IO132PB4F12	W18
IO133NB4F12	W17
IO133PB4F12	V17
IO135NB4F12	T15
IO135PB4F12	T16
IO138NB4F12	Y17
IO138PB4F12	Y18
IO139NB4F13	V15
IO139PB4F13	V16
IO140NB4F13	U18
IO140PB4F13	V19
IO142NB4F13	W20

FG484	
AX1000 Function	Pin Number
IO142PB4F13	V20
IO143NB4F13	W15
IO143PB4F13	W16
IO144NB4F13	AA18
IO144PB4F13	AA19
IO145NB4F13	U14
IO145PB4F13	U15
IO146NB4F13	Y15
IO146PB4F13	Y16
IO147NB4F13	AB18
IO147PB4F13	AB19
IO149NB4F13	Y14
IO149PB4F13	W14
IO150NB4F13	AA16
IO150PB4F13	AA17
IO152NB4F14	AA14
IO152PB4F14	AA15
IO154NB4F14	AB14
IO154PB4F14	AB15
IO155NB4F14	AA13
IO155PB4F14	AB13
IO158NB4F14	Y12
IO158PB4F14	Y13
IO159NB4F14/CLKEN	V12
IO159PB4F14/CLKEP	V13
IO160NB4F14/CLKFN	W11
IO160PB4F14/CLKFP	W12
Bank 5	
IO161NB5F15/CLKGN	U10
IO161PB5F15/CLKGP	U11
IO162NB5F15/CLKHN	V9
IO162PB5F15/CLKHP	V10
IO163NB5F15	Y10
IO163PB5F15	Y11
IO167NB5F15	AA11

FG676



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG676	
AX500 Function	Pin Number
IO51NB2F4	L20
IO51PB2F4	L21
IO52NB2F5	K26
IO52PB2F5	J26
IO53NB2F5	L23
IO53PB2F5	L22
IO54NB2F5	L24
IO54PB2F5	K24
IO55NB2F5	M20
IO55PB2F5	M21
IO56NB2F5	L26
IO56PB2F5	L25
IO57NB2F5	M23
IO57PB2F5	M22
IO58NB2F5	M26
IO58PB2F5	M25
IO59NB2F5	N22
IO59PB2F5	N23
IO60NB2F5	N24
IO60PB2F5	M24
IO61NB2F5	N20
IO61PB2F5	N21
IO62NB2F5	P25
IO62PB2F5	N25
Bank 3	
IO63NB3F6	T26
IO63PB3F6	R26
IO64NB3F6	R24
IO64PB3F6	P24
IO65NB3F6	P20
IO65PB3F6	P21
IO66NB3F6	T25
IO66PB3F6	R25
IO67NB3F6	T23
IO67PB3F6	R23

FG676	
AX500 Function	Pin Number
IO68NB3F6	V26
IO68PB3F6	U26
IO69NB3F6	V25
IO69PB3F6	U25
IO70NB3F6	Y25
IO70PB3F6	W25
IO71NB3F6	W24
IO71PB3F6	V24
IO72NB3F6	V23
IO72PB3F6	U23
IO73NB3F6	T21
IO73PB3F6	T20
IO74NB3F7	AA26
IO74PB3F7	Y26
IO75NB3F7	AA24
IO75PB3F7	Y24
IO76NB3F7	Y23
IO76PB3F7	W23
IO77NB3F7	V21
IO77PB3F7	U21
IO78NB3F7	AB25
IO78PB3F7	AA25
IO79NB3F7	AC26
IO79PB3F7	AB26
IO80NB3F7	AC24
IO80PB3F7	AB24
IO81NB3F7	AB23
IO81PB3F7	AA23
IO82NB3F7	AA22
IO82PB3F7	Y22
IO83NB3F7	AE26
IO83PB3F7	AD26
Bank 4	
IO84NB4F8	AB21
IO84PB4F8	AA21

FG676	
AX500 Function	Pin Number
IO85NB4F8	AE23
IO85PB4F8	AE24
IO86NB4F8	AC21
IO86PB4F8	AC22
IO87NB4F8	AF22
IO87PB4F8	AF23
IO88NB4F8	AD22
IO88PB4F8	AD23
IO89NB4F8	AC19
IO89PB4F8	AC20
IO90NB4F8	AE21
IO90PB4F8	AE22
IO91NB4F8	AA17
IO91PB4F8	AA18
IO92NB4F8	AD20
IO92PB4F8	AD21
IO93NB4F8	AF20
IO93PB4F8	AF21
IO94NB4F9	AE19
IO94PB4F9	AE20
IO95NB4F9	AC17
IO95PB4F9	AC18
IO96NB4F9	AD18
IO96PB4F9	AD19
IO97NB4F9	AA16
IO97PB4F9	Y16
IO98NB4F9	AE17
IO98PB4F9	AE18
IO99NB4F9	AC16
IO99PB4F9	AB16
IO100NB4F9	AF17
IO100PB4F9	AF18
IO101NB4F9	AA15
IO101PB4F9	Y15
IO102NB4F9	AC15

FG676	
AX1000 Function	**Pin Number**
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26
IO73PB2F6	D26
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23

FG676	
AX1000 Function	**Pin Number**
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
Bank 3	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24
IO100NB3F9	R22
IO100PB3F9	P22
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25

FG676	
AX1000 Function	**Pin Number**
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
Bank 4	
IO129NB4F12	AB21

FG896	
AX1000 Function	Pin Number
IO103NB3F9	V27
IO103PB3F9	U27
IO104NB3F9	W29
IO104PB3F9	V29
IO105NB3F9	Y28
IO105PB3F9	W28
IO106NB3F9	V25
IO106PB3F9	U25
IO107NB3F10	W26
IO107PB3F10	V26
IO108NB3F10	W24
IO108PB3F10	V24
IO109NB3F10	Y27
IO109PB3F10	W27
IO110NB3F10	V23
IO110PB3F10	V22
IO111NB3F10	AA29
IO111PB3F10	Y29
IO112NB3F10	Y25
IO112PB3F10	W25
IO113NB3F10	AB27
IO113PB3F10	AA27
IO114NB3F10	Y23
IO114PB3F10	W23
IO115NB3F10	AA26
IO115PB3F10	Y26
IO116NB3F10	AC28
IO116PB3F10	AB28
IO117NB3F10	AE29
IO117PB3F10	AD29
IO118NB3F11	AE28
IO118PB3F11	AD28
IO119NB3F11	AD27
IO119PB3F11	AC27
IO120NB3F11	AA24

FG896	
AX1000 Function	Pin Number
IO120PB3F11	Y24
IO121NB3F11	AB25
IO121PB3F11	AA25
IO122NB3F11	AC26
IO122PB3F11	AB26
IO123NB3F11	AG28
IO123PB3F11	AF28
IO124NB3F11	AB23
IO124PB3F11	AA23
IO125NB3F11	AF27
IO125PB3F11	AE27
IO126NB3F11	AD25
IO126PB3F11	AC25
IO127NB3F11	AE26
IO127PB3F11	AD26
IO128NB3F11	AC24
IO128PB3F11	AB24
Bank 4	
IO129NB4F12	AD23
IO129PB4F12	AC23
IO130NB4F12	AK26
IO130PB4F12	AK27
IO131NB4F12	AF24
IO131PB4F12	AF25
IO132NB4F12	AG25
IO132PB4F12	AG26
IO133NB4F12	AD22
IO133PB4F12	AC22
IO134NB4F12	AE23
IO134PB4F12	AE24
IO135NB4F12	AH24
IO135PB4F12	AH25
IO136NB4F12	AJ25
IO136PB4F12	AJ26
IO137NB4F12	AD21

FG896	
AX1000 Function	Pin Number
IO137PB4F12	AC21
IO138NB4F12	AK24
IO138PB4F12	AK25
IO139NB4F13	AE21
IO139PB4F13	AE22
IO140NB4F13	AG23
IO140PB4F13	AG24
IO141NB4F13	AF22
IO141PB4F13	AF23
IO142NB4F13	AJ23
IO142PB4F13	AJ24
IO143NB4F13	AD19
IO143PB4F13	AD20
IO144NB4F13	AG21
IO144PB4F13	AG22
IO145NB4F13	AE19
IO145PB4F13	AE20
IO146NB4F13	AF20
IO146PB4F13	AF21
IO147NB4F13	AC19
IO147PB4F13	AC20
IO148NB4F13	AH22
IO148PB4F13	AH23
IO149NB4F13	AC18
IO149PB4F13	AB18
IO150NB4F13	AK21
IO150PB4F13	AJ21
IO151NB4F13	AE18
IO151PB4F13	AD18
IO152NB4F14	AJ20
IO152PB4F14	AK20
IO153NB4F14	AG19
IO153PB4F14	AG20
IO154NB4F14	AH19
IO154PB4F14	AH20

FG896	
AX1000 Function	**Pin Number**
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

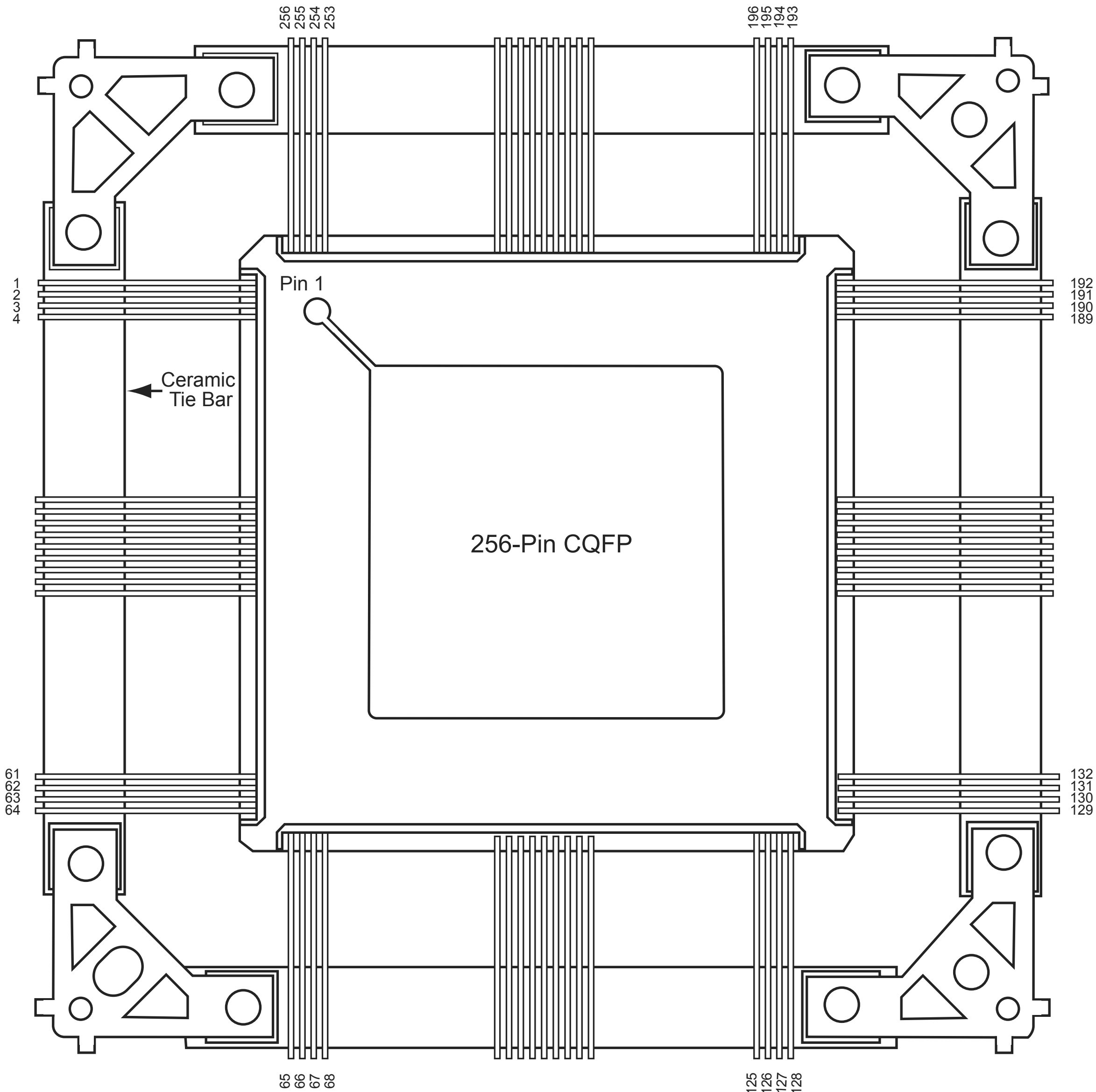
FG896	
AX1000 Function	**Pin Number**
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX1000 Function	**Pin Number**
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	**Pin Number**
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	**Pin Number**
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

CQ256



Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CQ352	
AX2000 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX2000 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114

CQ352	
AX2000 Function	Pin Number
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	91
VCCDA	116
VCCDA	117
VCCDA	130
VCCDA	131
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	174
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	268
VCCDA	293
VCCDA	294
VCCDA	307
VCCDA	308
VCCDA	309
VCCDA	327
VCCDA	328

CG624	
AX2000 Function	Pin Number
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20*
IO85PB1F7	D19*
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17*
IO89PB2F8	G22*
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23*
IO107PB2F10	N16*
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.