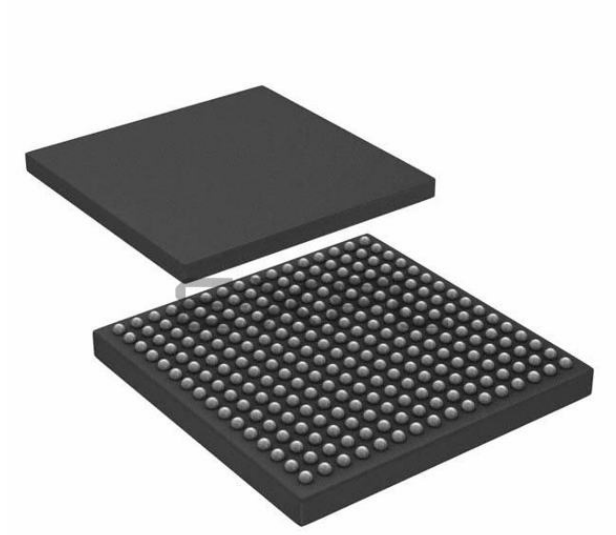

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2016 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 18432 |
| Number of I/O | 138 |
| Number of Gates | 125000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/ax125-1fg256 |

Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II, Microsemi's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-109).

# Summary

Microsemi's Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an Axcelerator design yet still achieve high performance and efficient device utilization.

# Related Documents

## Application Notes

*Simultaneous Switching Noise and Signal Integrity*
http://www.microsemi.com/soc/documents/SSN_AN.pdf
*Axcelerator Family PLL and Clock Management*
http://www.microsemi.com/soc/documents/AX_PLL_AN.pdf
*Implementation of Security in Actel Antifuse FPGAs*
http://www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

## User's Guides and Manuals

*Antifuse Macro Library Guide*
http://www.microsemi.com/soc/documents/libguide_UG.pdf
*SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder*
http://www.microsemi.com/soc/documents/genguide_ug.pdf
*Silicon Sculptor II User's Guide*
http://www.microsemi.com/soc/documents/silisculptII_sculpt3_ug.pdf

## White Paper

*Design Security in Nonvolatile Flash and Antifuse FPGAs*
http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf
*Understanding Actel Antifuse Device Security*
http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

## Miscellaneous

*Libero IDE flow diagram*
http://www.microsemi.com/soc/products/tools/libero/flow.html

***Table 2-5 •*** **Different Components Contributing to the Total Power Consumption in Axcelerator Devices**

| Component | Definition | Device Specific Value (in µW/MHz) | | | | |
|---|---|---|---|---|---|---|
| | | AX125 | AX250 | AX500 | AX1000 | AX2000 |
| P1 | Core tile HCLK power component | 33 | 49 | 71 | 130 | 216 |
| P2 | R-cell power component | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 |
| P3 | HCLK signal power dissipation | 4.5 | 4.5 | 9 | 13.5 | 18 |
| P4 | Core tile RCLK power component | 33 | 49 | 71 | 130 | 216 |
| P5 | R-cell power component | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| P6 | RCLK signal power dissipation | 6.5 | 6.5 | 13 | 19.5 | 26 |
| P7 | Power dissipation due to the switching activity on the R-cell | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 |
| P8 | Power dissipation due to the switching activity on the C-cell | 1.4 | 1.4 | 1.4 | 1.4 | 1.4 |
| P9 | Power component associated with the input voltage | 10 | 10 | 10 | 10 | 10 |
| P10 | Power component associated with the output voltage | See table Per pin contribution | | | | |
| P11 | Power component associated with the read operation in the RAM block | 25 | 25 | 25 | 25 | 25 |
| P12 | Power component associated with the write operation in the RAM block | 30 | 30 | 30 | 30 | 30 |
| P13 | Core PLL power component | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 |

***Ptotal = Pdc + Pac***

$P_{dc}$ = ICCA * VCCA

$P_{ac}$ = $P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$

***$P_{HCLK}$ = (P1 + P2 * s + P3 * sqrt[s]) * Fs***

s = the number of R-cells clocked by this clock

Fs = the clock frequency

***PCLK = (P4 + P5 * s + P6 * sqrt[s]) * Fs***

s = the number of R-cells clocked by this clock

Fs = the clock frequency

***PR-cells = P7 * ms * Fs***

ms = the number of R-cells switching at each Fs cycle

Fs = the clock frequency

***PC-cells = P8 * mc * Fs***

mc = the number of C-cells switching at each Fs cycle

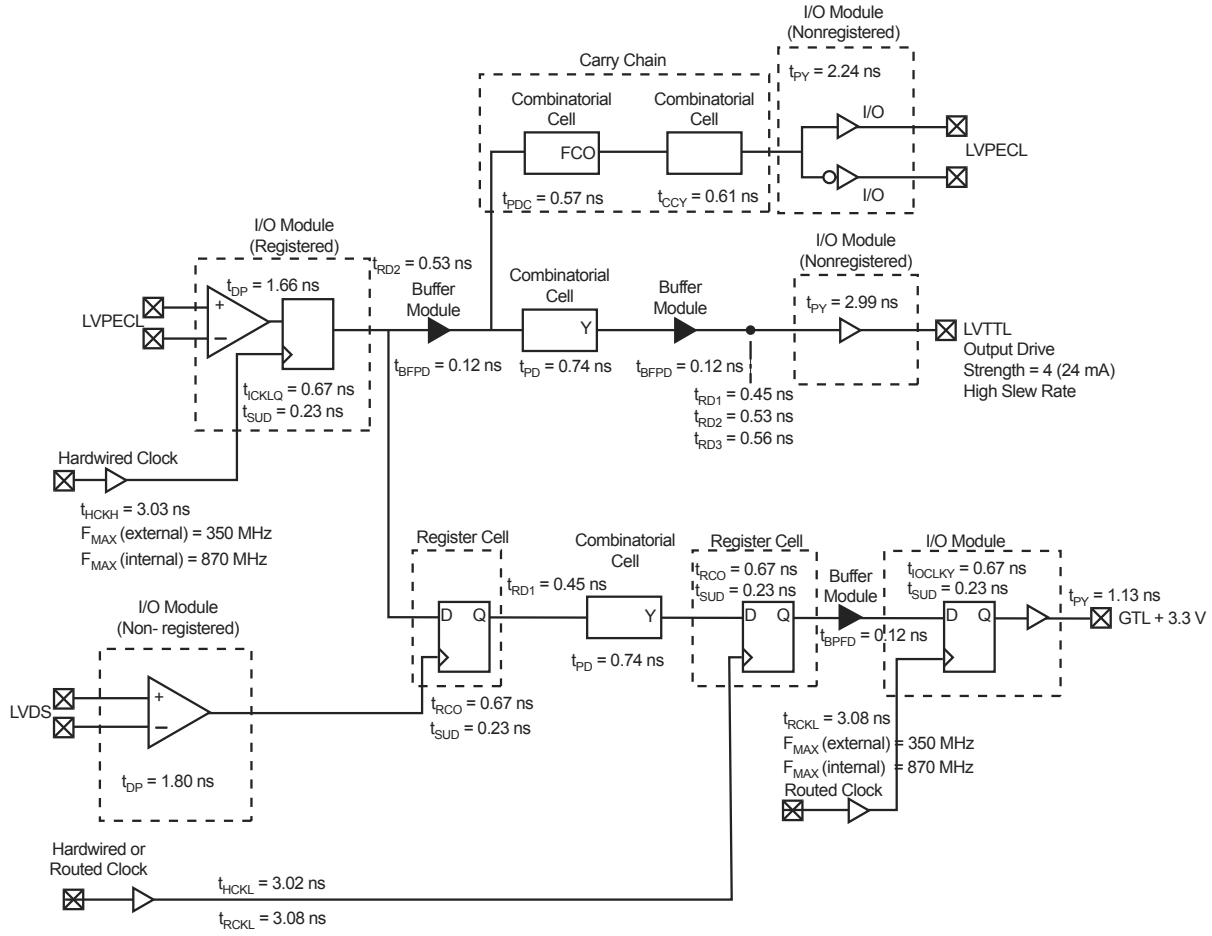
Fs = the clock frequency

***Pinputs = P9 * pi * Fpi***

pi = the number of inputs

$F_{pi}$ = the average input frequency

## Timing Model




*Note: Worst case timing data for the AX1000, –2 speed grade*

***Figure 2-1 •*** **Worst Case Timing Data**

### *Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O*

External Setup

$= (t_{DP} + t_{RD2} + t_{SUD}) – t_{HCKL}$

$= (1.72 + 0.53 + 0.23) – 3.02 = –0.54$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{HCKL} + t_{RCO} + t_{RD1} + t_{PY}$

$= 3.02 + 0.67 + 0.45 + 2.99 = 7.13$ ns

### *Routed Clock – Using LVTTL 24 mA High Slew Clock I/O*

External Setup

$= (t_{DP} + t_{RD2} + t_{SUD}) – t_{RCKH}$

$= (1.72 + 0.53 + 0.23) – 3.13 = –0.65$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$

$= 3.13 + 0.67 + 0.45 + 3.03 = 7.24$ ns

***Table 2-40* • 3.3 V GTL+ I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **3.3 V GTL+I/O Module Timing** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.71 | | 1.95 | | 2.29 | ns |
| $t_{PY}$ | Output Buffer | | 1.13 | | 1.29 | | 1.52 | ns |
| $t_{ICLKQ}$ | Clock-to-Q for the I/O input register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{OCLKQ}$ | Clock-to-Q for the I/O output register and the I/O enable register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |

## Carry-Chain Logic

The Axcelerator dedicated carry-chain logic offers a very compact solution for implementing arithmetic functions without sacrificing performance.

To implement the carry-chain logic, two C-cells in a Cluster are connected together so the FCO (i.e. carry out) for the two bits is generated in a carry look-ahead scheme to achieve minimum propagation delay from the FCI (i.e. carry in) into the two-bit Cluster. The two-bit carry logic is shown in Figure 2-29.

The FCI of one C-cell pair is driven by the FCO of the C-cell pair immediately above it. Similarly, the FCO of one C-cell pair, drives the FCI input of the C-cell pair immediately below it (Figure 1-4 on page 1-3 and Figure 2-30 on page 2-57).

The carry-chain logic is selected via the CFN input. When carry logic is not required, this signal is deasserted to save power. Again, this configuration is handled automatically for the user through Microsemi's macro library.

The signal propagation delay between two C-cells in the carry-chain sequence is 0.1 ns.

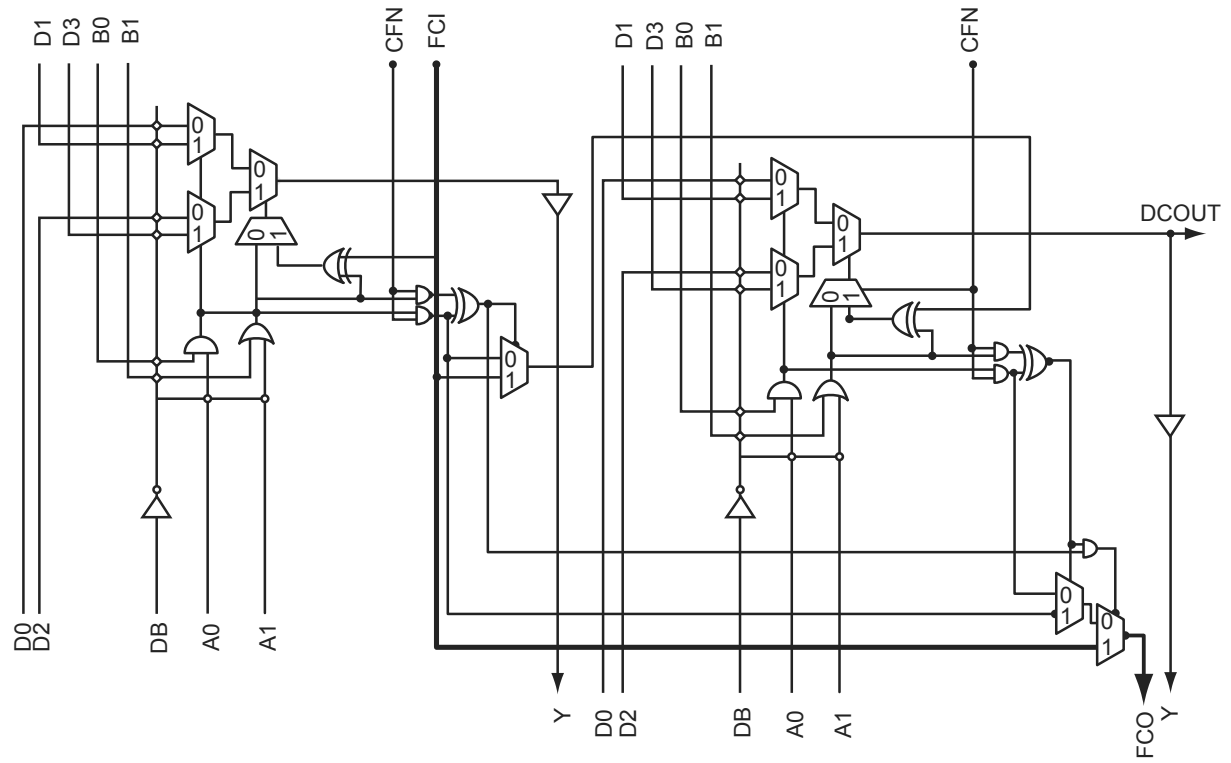



***Figure 2-29 •*** **Axcelerator's Two-Bit Carry Logic**

# Routing Specifications

## Routing Resources

The routing structure found in Axcelerator devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the AX architecture: DirectConnect, CarryConnect, FastConnect, and Vertical and Horizontal Routing.

### *DirectConnect*

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 2-35). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

***Figure 2-35 •*** **DirectConnect and CarryConnect**

### *CarryConnect*

CarryConnects are used to build carry chains for arithmetic functions (Figure 2-35). The FCO output of the right C-cell of a two-C-cell Cluster drives the FCI input of the left C-cell in the two-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two-C-cell cluster to the FCI of the two-C-cell cluster immediately below it (see the "Carry-Chain Logic" section on page 2-56 for more information).

### *FastConnect*

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 2-36 on page 2-62). FastConnects provide a maximum delay of 0.3 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

# Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

## Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

### *Timing Characteristics*

***Table 2-70* • AX125 Dedicated (Hardwired) Array Clock Networks**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | |
| $t_{HCKL}$ | Input Low to High | | 3.02 | | 3.44 | | 4.05 | ns |
| $t_{HCKH}$ | Input High to Low | | 3.03 | | 3.46 | | 4.06 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 0.58 | | 0.65 | | 0.77 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 0.52 | | 0.59 | | 0.69 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.06 | | 0.07 | | 0.08 | ns |
| $t_{HP}$ | Minimum Period | 1.15 | | 1.31 | | 1.54 | | ns |
| $t_{HMAX}$ | Maximum Frequency | | 870 | | 763 | | 649 | MHz |

***Table 2-71* • AX250 Dedicated (Hardwired) Array Clock Networks**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Networks** | | | | | | | | |
| $t_{HCKL}$ | Input Low to High | | 2.57 | | 2.93 | | 3.45 | ns |
| $t_{HCKH}$ | Input High to Low | | 2.61 | | 2.97 | | 3.50 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 0.58 | | 0.65 | | 0.77 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 0.52 | | 0.59 | | 0.69 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.06 | | 0.07 | | 0.08 | ns |
| $t_{HP}$ | Minimum Period | 1.15 | | 1.31 | | 1.54 | | ns |
| $t_{HMAX}$ | Maximum Frequency | | 870 | | 763 | | 649 | MHz |

The HM and CM modules can select between:

- The HCLK or CLK source respectively
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module respectively
- A local signal routed on generic routing resources

The AX architecture is capable of supporting a large number of local clocks—24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Microsemi's Designer software's place-and-route takes advantage of the segmented clock structure found in Axcelerator devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption.

## Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s), an internal net, or the output of a PLL. These connections can be made by using one of three types of macros: CLKBUF, CLKINT, and PLLCLK.

### *CLKBUF and HCLKBUF*

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF_LVCMOS25, HCLKBUF_LVDS, etc.) (Figure 2-42).

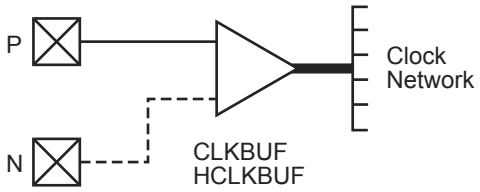



***Figure 2-42 •*** **CLKBUF and HCLKBUF**

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

### *CLKINT and HCLKINT*

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 2-43).

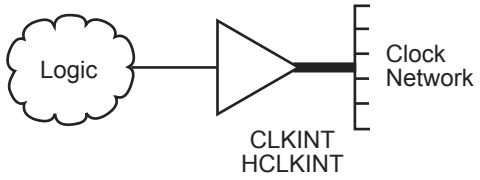



***Figure 2-43 •*** **CLKINT and HCLKINT**

Figure 2-63 illustrates flag generation.

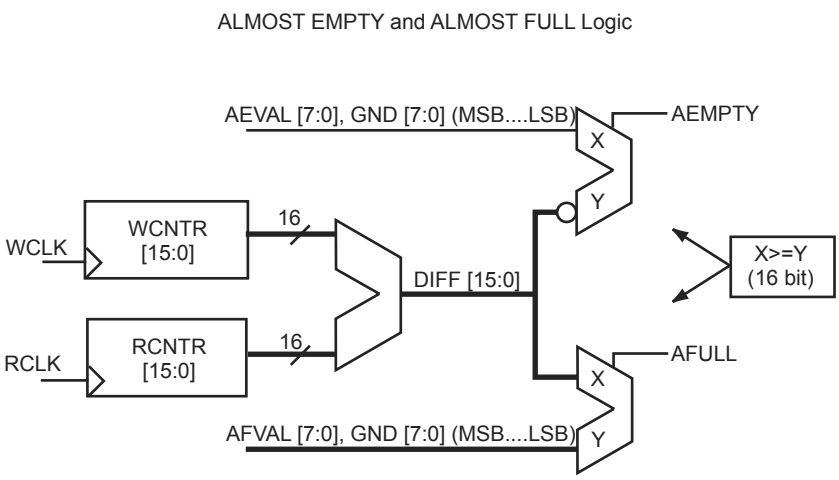



***Figure 2-63 •*** **ALMOST-EMPTY and ALMOST-FULL Logic**

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-95).

***Table 2-95 •*** **Number of Available Configuration Bits**

| Number of Blocks | Block DxW | Number of AEVAL/AFVAL Bits |
|---|---|---|
| 1 | 1x1 | 4 |
| 2 | 1x2 | 4 |
| 2 | 2x1 | 5 |
| 4 | 1x4 | 4 |
| 4 | 2x2 | 5 |
| 4 | 4x1 | 6 |
| 8 | 1x8 | 4 |
| 8 | 2x4 | 5 |
| 8 | 4x2 | 6 |
| 8 | 8x1 | 7 |
| 16 | 1x16 | 4 |
| 16 | 2x8 | 5 |
| 16 | 4x4 | 6 |
| 16 | 8x2 | 7 |
| 16 | 16x1 | 8 |

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-100.

## Clock

As with RAM configuration, the RCLK and WCLK pins have independent polarity selection.

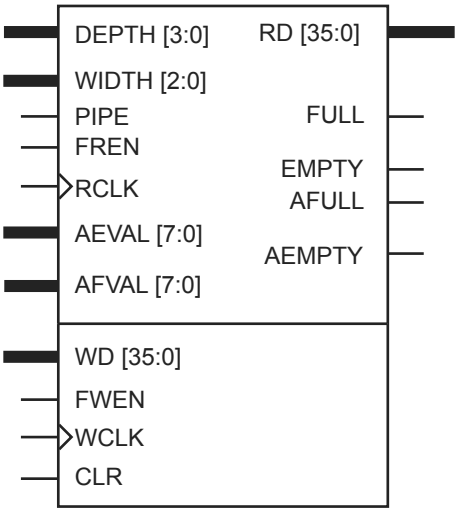



***Figure 2-65 •*** **FIFO Block Diagram**

***Table 2-97 •*** **FIFO Signal Description**

| Signal | Direction | Description |
|---|---|---|
| WCLK | Input | Write clock (active either edge). |
| FWEN | Input | FIFO write enable. When this signal is asserted, the WD bus data is latched into the FIFO, and the internal write counters are incremented. |
| WD[N-1:0] | Input | Write data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36. |
| FULL | Output | Active high signal indicating that the FIFO is FULL. When this signal is set, additional write requests are ignored. |
| AFULL | Output | Active high signal indicating that the FIFO is AFULL. |
| AFVAL | Input | 8-bit input defining the AFULL value of the FIFO. |
| RCLK | Input | Read clock (active either edge). |
| FREN | Input | FIFO read enable. |
| RD[N-1:0] | Output | Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36. |
| EMPTY | Output | Empty flag indicating that the FIFO is EMPTY. When this signal is asserted, attempts to read the FIFO will be ignored. |
| AEMPTY | Output | Active high signal indicating that the FIFO is AEMPTY. |
| AEVAL | Input | 8-bit input defining the almost-empty value of the FIFO. |
| PIPE | Input | Sets the pipe option on or off. |
| CLR | Input | Active high clear input. |
| DEPTH | Input | Determines the depth of the FIFO and the number of FIFOs to be cascaded. |
| WIDTH | Input | Determines the width of the dataword/FIFO, and the number of the FIFOs to be cascaded. |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| **Bank 0** | |
| IO00NB0F0 | E6 |
| IO00PB0F0 | F6 |
| IO01NB0F0 | G8 |
| IO01PB0F0 | G7 |
| IO02NB0F0 | D7 |
| IO02PB0F0 | E7 |
| IO03NB0F0 | D5 |
| IO03PB0F0 | E5 |
| IO04NB0F0 | G9 |
| IO04PB0F0 | H9 |
| IO05NB0F0 | E8 |
| IO05PB0F0 | F8 |
| IO06NB0F0 | C6 |
| IO06PB0F0 | D6 |
| IO07NB0F0 | B5 |
| IO07PB0F0 | C5 |
| IO08NB0F0 | A6 |
| IO08PB0F0 | A5 |
| IO09NB0F0 | E9 |
| IO09PB0F0 | F9 |
| IO10NB0F0 | G10 |
| IO10PB0F0 | H10 |
| IO11NB0F0 | B7 |
| IO11PB0F0 | B6 |
| IO12NB0F1 | C8 |
| IO12PB0F1 | C7 |
| IO13NB0F1 | E10 |
| IO13PB0F1 | F10 |
| IO14NB0F1 | G11 |
| IO14PB0F1 | H11 |
| IO15NB0F1 | D9 |
| IO15PB0F1 | D8 |
| IO16NB0F1 | A8 |
| IO16PB0F1 | A7 |
| IO17NB0F1 | B9 |
| IO17PB0F1 | B8 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO18NB0F1 | C10 |
| IO18PB0F1 | C9 |
| IO19NB0F1 | E11 |
| IO19PB0F1 | F11 |
| IO20NB0F1 | G12 |
| IO20PB0F1 | H12 |
| IO21NB0F1 | D11 |
| IO21PB0F1 | D10 |
| IO22NB0F2 | A10 |
| IO22PB0F2 | A9 |
| IO23NB0F2 | B11 |
| IO23PB0F2 | B10 |
| IO24NB0F2 | G13 |
| IO24PB0F2 | H13 |
| IO25NB0F2 | C12 |
| IO25PB0F2 | C11 |
| IO26NB0F2 | E12 |
| IO26PB0F2 | D12 |
| IO27NB0F2 | E13 |
| IO27PB0F2 | F13 |
| IO28NB0F2 | G14 |
| IO28PB0F2 | H14 |
| IO29NB0F2 | A12 |
| IO29PB0F2 | B12 |
| IO30NB0F2/HCLKAN | C13 |
| IO30PB0F2/HCLKAP | D13 |
| IO31NB0F2/HCLKBN | F14 |
| IO31PB0F2/HCLKBP | E14 |
| **Bank 1** | |
| IO32NB1F3/HCLKCN | C14 |
| IO32PB1F3/HCLKCP | B14 |
| IO33NB1F3/HCLKDN | D16 |
| IO33PB1F3/HCLKDP | D15 |
| IO34NB1F3 | B16 |
| IO34PB1F3 | A16 |
| IO35NB1F3 | E15 |
| IO35PB1F3 | F15 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO36NB1F3 | H15 |
| IO36PB1F3 | G15 |
| IO37NB1F3 | C17 |
| IO37PB1F3 | C16 |
| IO38NB1F3 | B18 |
| IO38PB1F3 | B17 |
| IO39NB1F3 | A18 |
| IO39PB1F3 | A17 |
| IO40NB1F3 | H16 |
| IO40PB1F3 | G16 |
| IO41NB1F4 | B19 |
| IO41PB1F4 | A19 |
| IO42NB1F4 | C19 |
| IO42PB1F4 | C18 |
| IO43NB1F4 | D18 |
| IO43PB1F4 | D17 |
| IO44NB1F4 | H17 |
| IO44PB1F4 | G17 |
| IO45NB1F4 | F17 |
| IO45PB1F4 | E17 |
| IO46NB1F4 | B20 |
| IO46PB1F4 | A20 |
| IO47NB1F4 | C21 |
| IO47PB1F4 | C20 |
| IO48NB1F4 | H18 |
| IO48PB1F4 | G18 |
| IO49NB1F4 | F18 |
| IO49PB1F4 | E18 |
| IO50NB1F4 | D20 |
| IO50PB1F4 | D19 |
| IO51NB1F4 | A22 |
| IO51PB1F4 | A21 |
| IO52NB1F4 | B22 |
| IO52PB1F4 | B21 |
| IO53NB1F4 | F19 |
| IO53PB1F4 | E19 |
| IO54NB1F5 | F20 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO54PB1F5 | E20 |
| IO55NB1F5 | E21 |
| IO55PB1F5 | D21 |
| IO56NB1F5 | H19 |
| IO56PB1F5 | G19 |
| IO57NB1F5 | D22 |
| IO57PB1F5 | C22 |
| IO58NB1F5 | B23 |
| IO58PB1F5 | A23 |
| IO59NB1F5 | D23 |
| IO59PB1F5 | C23 |
| IO60NB1F5 | G21 |
| IO60PB1F5 | G20 |
| IO61NB1F5 | E23 |
| IO61PB1F5 | E22 |
| IO62NB1F5 | F22 |
| IO62PB1F5 | F21 |
| IO63NB1F5 | H20 |
| IO63PB1F5 | J19 |
| **Bank 2** | |
| IO64NB2F6 | J21 |
| IO64PB2F6 | H21 |
| IO65NB2F6 | F24 |
| IO65PB2F6 | F23 |
| IO66NB2F6 | F26 |
| IO66PB2F6 | F25 |
| IO67NB2F6 | E26 |
| IO67PB2F6 | E25 |
| IO68NB2F6 | J22 |
| IO68PB2F6 | H22 |
| IO69NB2F6 | G24 |
| IO69PB2F6 | G23 |
| IO70NB2F6 | K20 |
| IO70PB2F6 | J20 |
| IO71NB2F6 | G26 |
| IO71PB2F6 | G25 |
| IO72NB2F6 | J24 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO72PB2F6 | J23 |
| IO73NB2F6 | H24 |
| IO73PB2F6 | H23 |
| IO74NB2F7 | L21 |
| IO74PB2F7 | K21 |
| IO75NB2F7 | G27 |
| IO75PB2F7 | F27 |
| IO76NB2F7 | K23 |
| IO76PB2F7 | K22 |
| IO77NB2F7 | H26 |
| IO77PB2F7 | H25 |
| IO78NB2F7 | K25 |
| IO78PB2F7 | K24 |
| IO79NB2F7 | J26 |
| IO79PB2F7 | J25 |
| IO80NB2F7 | M20 |
| IO80PB2F7 | L20 |
| IO81NB2F7 | J27 |
| IO81PB2F7 | H27 |
| IO82NB2F7 | L23 |
| IO82PB2F7 | L22 |
| IO83NB2F7 | L25 |
| IO83PB2F7 | L24 |
| IO84NB2F7 | N21 |
| IO84PB2F7 | M21 |
| IO85NB2F8 | K27 |
| IO85PB2F8 | K26 |
| IO86NB2F8 | M23 |
| IO86PB2F8 | M22 |
| IO87NB2F8 | M25 |
| IO87PB2F8 | M24 |
| IO88NB2F8 | L27 |
| IO88PB2F8 | L26 |
| IO89NB2F8 | M27 |
| IO89PB2F8 | M26 |
| IO90NB2F8 | N23 |
| IO90PB2F8 | N22 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO91NB2F8 | N25 |
| IO91PB2F8 | N24 |
| IO92NB2F8 | N27 |
| IO92PB2F8 | N26 |
| IO93NB2F8 | P26 |
| IO93PB2F8 | P27 |
| IO94NB2F8 | N19 |
| IO94PB2F8 | N20 |
| IO95NB2F8 | P23 |
| IO95PB2F8 | P22 |
| **Bank 3** | |
| IO96NB3F9 | P25 |
| IO96PB3F9 | P24 |
| IO97NB3F9 | R26 |
| IO97PB3F9 | R27 |
| IO98NB3F9 | P21 |
| IO98PB3F9 | P20 |
| IO99NB3F9 | R24 |
| IO99PB3F9 | R25 |
| IO100NB3F9 | T26 |
| IO100PB3F9 | T27 |
| IO101NB3F9 | T24 |
| IO101PB3F9 | T25 |
| IO102NB3F9 | R20 |
| IO102PB3F9 | R21 |
| IO103NB3F9 | R23 |
| IO103PB3F9 | R22 |
| IO104NB3F9 | U26 |
| IO104PB3F9 | U27 |
| IO105NB3F9 | U24 |
| IO105PB3F9 | U25 |
| IO106NB3F9 | R19 |
| IO106PB3F9 | P19 |
| IO107NB3F10 | V26 |
| IO107PB3F10 | V27 |
| IO108NB3F10 | T23 |
| IO108PB3F10 | T22 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO218PB6F20 | V2 |
| IO219NB6F20 | T1 |
| IO219PB6F20 | U1 |
| IO220NB6F20 | R5 |
| IO220PB6F20 | R6 |
| IO221NB6F20 | T3 |
| IO221PB6F20 | T4 |
| IO222NB6F20 | R2 |
| IO222PB6F20 | T2 |
| IO223NB6F20 | P8 |
| IO223PB6F20 | P9 |
| IO224NB6F20 | R3 |
| IO224PB6F20 | R4 |
| **Bank 7** | |
| IO225NB7F21 | P1 |
| IO225PB7F21 | R1 |
| IO226NB7F21 | P3 |
| IO226PB7F21 | P2 |
| IO227NB7F21 | N7 |
| IO227PB7F21 | P7 |
| IO228NB7F21 | P5 |
| IO228PB7F21 | P4 |
| IO229NB7F21 | N2 |
| IO229PB7F21 | N1 |
| IO230NB7F21 | N6 |
| IO230PB7F21 | P6 |
| IO231NB7F21 | N9 |
| IO231PB7F21 | N8 |
| IO232NB7F21 | N4 |
| IO232PB7F21 | N3 |
| IO233NB7F21 | M2 |
| IO233PB7F21 | M1 |
| IO234NB7F21 | M4 |
| IO234PB7F21 | M3 |
| IO235NB7F21 | M5 |
| IO235PB7F21 | N5 |
| IO236NB7F22 | L2 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO236PB7F22 | L1 |
| IO237NB7F22 | L4 |
| IO237PB7F22 | L3 |
| IO238NB7F22 | L6 |
| IO238PB7F22 | M6 |
| IO239NB7F22 | M8 |
| IO239PB7F22 | M7 |
| IO240NB7F22 | K2 |
| IO240PB7F22 | K1 |
| IO241NB7F22 | K4 |
| IO241PB7F22 | K3 |
| IO242NB7F22 | K5 |
| IO242PB7F22 | L5 |
| IO243NB7F22 | J2 |
| IO243PB7F22 | J1 |
| IO244NB7F22 | J4 |
| IO244PB7F22 | J3 |
| IO245NB7F22 | H2 |
| IO245PB7F22 | H1 |
| IO246NB7F22 | H4 |
| IO246PB7F22 | H3 |
| IO247NB7F23 | L8 |
| IO247PB7F23 | L7 |
| IO248NB7F23 | J6 |
| IO248PB7F23 | K6 |
| IO249NB7F23 | H5 |
| IO249PB7F23 | J5 |
| IO250NB7F23 | G2 |
| IO250PB7F23 | G1 |
| IO251NB7F23 | K8 |
| IO251PB7F23 | K7 |
| IO252NB7F23 | G4 |
| IO252PB7F23 | G3 |
| IO253NB7F23 | F2 |
| IO253PB7F23 | F1 |
| IO254NB7F23 | G6 |
| IO254PB7F23 | H6 |

| BG729 | |
|---|---|
| AX1000 Function | Pin Number |
| IO255NB7F23 | F5 |
| IO255PB7F23 | G5 |
| IO256NB7F23 | F3 |
| IO256PB7F23 | F4 |
| IO257NB7F23 | H7 |
| IO257PB7F23 | J7 |
| **Dedicated I/O** | |
| GND | A1 |
| GND | A2 |
| GND | A25 |
| GND | A26 |
| GND | A27 |
| GND | A3 |
| GND | AC24 |
| GND | AE1 |
| GND | AE2 |
| GND | AE25 |
| GND | AE26 |
| GND | AE27 |
| GND | AE3 |
| GND | AE5 |
| GND | AF1 |
| GND | AF2 |
| GND | AF25 |
| GND | AF26 |
| GND | AF27 |
| GND | AF3 |
| GND | AG1 |
| GND | AG2 |
| GND | AG25 |
| GND | AG26 |
| GND | AG27 |
| GND | AG3 |
| GND | B1 |
| GND | B2 |
| GND | B25 |
| GND | B26 |

| FG484 | |
|---|---|
| AX500 Function | Pin Number |
| IO54PB2F5 | H22 |
| IO55NB2F5 | L17 |
| IO55PB2F5 | K17 |
| IO56NB2F5 | K21 |
| IO56PB2F5 | K22 |
| IO58NB2F5 | L20 |
| IO58PB2F5 | K20 |
| IO59NB2F5 | L18 |
| IO59PB2F5 | K18 |
| IO60NB2F5 | M21 |
| IO60PB2F5 | L21 |
| IO61NB2F5 | L16 |
| IO61PB2F5 | K16 |
| IO62NB2F5 | M19 |
| IO62PB2F5 | L19 |
| **Bank 3** | |
| IO63NB3F6 | N16 |
| IO63PB3F6 | M16 |
| IO64NB3F6 | P22 |
| IO64PB3F6 | N22 |
| IO65NB3F6 | N20 |
| IO65PB3F6 | M20 |
| IO66NB3F6 | P21 |
| IO66PB3F6 | N21 |
| IO67NB3F6 | N18 |
| IO67PB3F6 | N19 |
| IO68NB3F6 | T22 |
| IO68PB3F6 | R22 |
| IO69NB3F6 | N17 |
| IO69PB3F6 | M17 |
| IO70NB3F6 | T21 |
| IO70PB3F6 | R21 |
| IO71NB3F6 | P18 |
| IO71PB3F6 | P19 |
| IO72NB3F6 | R20 |

| FG484 | |
|---|---|
| AX500 Function | Pin Number |
| IO72PB3F6 | P20 |
| IO73PB3F6 | R19 |
| IO74NB3F7 | V21 |
| IO74PB3F7 | U21 |
| IO75NB3F7 | V22 |
| IO75PB3F7 | U22 |
| IO76NB3F7 | U20 |
| IO76PB3F7 | T20 |
| IO77NB3F7 | R17 |
| IO77PB3F7 | P17 |
| IO78NB3F7 | W21 |
| IO78PB3F7 | W22 |
| IO79NB3F7 | T18 |
| IO79PB3F7 | R18 |
| IO80NB3F7 | W20 |
| IO80PB3F7 | V20 |
| IO81NB3F7 | U19 |
| IO81PB3F7 | T19 |
| IO82NB3F7 | U18 |
| IO82PB3F7 | V19 |
| IO83NB3F7 | R16 |
| IO83PB3F7 | P16 |
| **Bank 4** | |
| IO84NB4F8 | AB18 |
| IO84PB4F8 | AB19 |
| IO85NB4F8 | T15 |
| IO85PB4F8 | T16 |
| IO86NB4F8 | AA18 |
| IO86PB4F8 | AA19 |
| IO87NB4F8 | W17 |
| IO87PB4F8 | V17 |
| IO88NB4F8 | Y19 |
| IO88PB4F8 | W18 |
| IO89NB4F8 | U14 |
| IO89PB4F8 | U15 |

| FG484 | |
|---|---|
| AX500 Function | Pin Number |
| IO90NB4F8 | Y17 |
| IO90PB4F8 | Y18 |
| IO91NB4F8 | V15 |
| IO91PB4F8 | V16 |
| IO92PB4F8 | AB17 |
| IO93NB4F8 | Y15 |
| IO93PB4F8 | Y16 |
| IO94NB4F9 | AA16 |
| IO94PB4F9 | AA17 |
| IO95NB4F9 | AB14 |
| IO95PB4F9 | AB15 |
| IO96NB4F9 | W15 |
| IO96PB4F9 | W16 |
| IO97NB4F9 | AA13 |
| IO97PB4F9 | AB13 |
| IO98NB4F9 | AA14 |
| IO98PB4F9 | AA15 |
| IO100NB4F9 | Y14 |
| IO100PB4F9 | W14 |
| IO101NB4F9 | Y12 |
| IO101PB4F9 | Y13 |
| IO102NB4F9 | AA11 |
| IO102PB4F9 | AA12 |
| IO103NB4F9/CLKEN | V12 |
| IO103PB4F9/CLKEP | V13 |
| IO104NB4F9/CLKFN | W11 |
| IO104PB4F9/CLKFP | W12 |
| **Bank 5** | |
| IO105NB5F10/CLKGN | U10 |
| IO105PB5F10/CLKGP | U11 |
| IO106NB5F10/CLKHN | V9 |
| IO106PB5F10/CLKHP | V10 |
| IO107NB5F10 | Y10 |
| IO107PB5F10 | Y11 |
| IO108NB5F10 | AA9 |

| FG676 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO129PB4F12 | AA21 |
| IO131NB4F12 | AD22 |
| IO131PB4F12 | AD23 |
| IO132NB4F12 | AE23 |
| IO132PB4F12 | AE24 |
| IO133NB4F12 | AB20 |
| IO133PB4F12 | AA20 |
| IO134NB4F12 | AC21 |
| IO134PB4F12 | AC22 |
| IO135NB4F12 | AF22 |
| IO135PB4F12 | AF23 |
| IO137NB4F12 | AB19 |
| IO137PB4F12 | AA19 |
| IO139NB4F13 | AC19 |
| IO139PB4F13 | AC20 |
| IO140NB4F13 | AE21 |
| IO140PB4F13 | AE22 |
| IO141NB4F13 | AD20 |
| IO141PB4F13 | AD21 |
| IO143NB4F13 | AB17 |
| IO143PB4F13 | AB18 |
| IO144NB4F13 | AE19 |
| IO144PB4F13 | AE20 |
| IO145NB4F13 | AC17 |
| IO145PB4F13 | AC18 |
| IO146NB4F13 | AD18 |
| IO146PB4F13 | AD19 |
| IO147NB4F13 | AA17 |
| IO147PB4F13 | AA18 |
| IO148NB4F13 | AF20 |
| IO148PB4F13 | AF21 |
| IO149NB4F13 | AA16 |
| IO149PB4F13 | Y16 |
| IO151NB4F13 | AC16 |
| IO151PB4F13 | AB16 |
| IO153NB4F14 | AE17 |

| FG676 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO153PB4F14 | AE18 |
| IO154NB4F14 | AF17 |
| IO154PB4F14 | AF18 |
| IO155NB4F14 | AA15 |
| IO155PB4F14 | Y15 |
| IO157NB4F14 | AC15 |
| IO157PB4F14 | AB15 |
| IO159NB4F14/CLKEN | AE16 |
| IO159PB4F14/CLKEP | AF16 |
| IO160NB4F14/CLKFN | AE14 |
| IO160PB4F14/CLKFP | AE15 |
| **Bank 5** | |
| IO161NB5F15/CLKGN | AE12 |
| IO161PB5F15/CLKGP | AE13 |
| IO162NB5F15/CLKHN | AE11 |
| IO162PB5F15/CLKHP | AF11 |
| IO163NB5F15 | AC12 |
| IO163PB5F15 | AB12 |
| IO165NB5F15 | Y12 |
| IO165PB5F15 | AA13 |
| IO167NB5F15 | Y11 |
| IO167PB5F15 | AA12 |
| IO168NB5F15 | AF9 |
| IO168PB5F15 | AF10 |
| IO169NB5F15 | AB11 |
| IO169PB5F15 | AA11 |
| IO171NB5F16 | AE9 |
| IO171PB5F16 | AE10 |
| IO173NB5F16 | AC10 |
| IO173PB5F16 | AC11 |
| IO174NB5F16 | AE7 |
| IO174PB5F16 | AE8 |
| IO175NB5F16 | AC9 |
| IO175PB5F16 | AD9 |
| IO176NB5F16 | AF6 |
| IO176PB5F16 | AF7 |

| FG676 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO177NB5F16 | AA10 |
| IO177PB5F16 | AB10 |
| IO179NB5F16 | AD7 |
| IO179PB5F16 | AD8 |
| IO180NB5F16 | AC7 |
| IO180PB5F16 | AC8 |
| IO181NB5F17 | AA9 |
| IO181PB5F17 | AB9 |
| IO183NB5F17 | AD6 |
| IO183PB5F17 | AE6 |
| IO184NB5F17 | AE5 |
| IO184PB5F17 | AF5 |
| IO185NB5F17 | AA8 |
| IO185PB5F17 | AB8 |
| IO187NB5F17 | AC5 |
| IO187PB5F17 | AC6 |
| IO188NB5F17 | AD4 |
| IO188PB5F17 | AD5 |
| IO189NB5F17 | AB6 |
| IO189PB5F17 | AB7 |
| IO190NB5F17 | AF4 |
| IO190PB5F17 | AE4 |
| IO191NB5F17 | AE3 |
| IO191PB5F17 | AF3 |
| IO192NB5F17 | AA6 |
| IO192PB5F17 | AA7 |
| **Bank 6** | |
| IO193NB6F18 | Y5 |
| IO193PB6F18 | AA5 |
| IO194NB6F18 | AB3 |
| IO194PB6F18 | AC3 |
| IO195NB6F18 | Y4 |
| IO195PB6F18 | AA4 |
| IO196NB6F18 | AC2 |
| IO196PB6F18 | AD2 |
| IO197NB6F18 | W6 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO65PB1F6 | H20 |
| IO66NB1F6 | B23 |
| IO66PB1F6 | B21 |
| IO67NB1F6 | H21 |
| IO67PB1F6 | G21 |
| IO68NB1F6 | D22 |
| IO68PB1F6 | C22 |
| IO69NB1F6 | A25 |
| IO69PB1F6 | A24 |
| IO70NB1F6 | F22 |
| IO70PB1F6 | E22 |
| IO71NB1F6 | F21 |
| IO71PB1F6 | E21 |
| IO73NB1F6 | C24 |
| IO73PB1F6 | C23 |
| IO74NB1F6 | D24 |
| IO74PB1F6 | D23 |
| IO75NB1F6 | H23 |
| IO75PB1F6 | H22 |
| IO76NB1F7 | B25 |
| IO76PB1F7 | B24 |
| IO78NB1F7 | B26 |
| IO78PB1F7 | A26 |
| IO79NB1F7 | F23 |
| IO79PB1F7 | E23 |
| IO80NB1F7 | D25 |
| IO80PB1F7 | C25 |
| IO81NB1F7 | G23 |
| IO81PB1F7 | G22 |
| IO82NB1F7 | B27 |
| IO82PB1F7 | A27 |
| IO83NB1F7 | F24 |
| IO83PB1F7 | E24 |
| IO84NB1F7 | D26 |
| IO84PB1F7 | C26 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO85NB1F7 | F25 |
| IO85PB1F7 | E25 |
| **Bank 2** | |
| IO86NB2F8 | G26 |
| IO86PB2F8 | G25 |
| IO87NB2F8 | K23 |
| IO87PB2F8 | J23 |
| IO88NB2F8 | J24 |
| IO88PB2F8 | H24 |
| IO89NB2F8 | E29 |
| IO89PB2F8 | D29 |
| IO90NB2F8 | F27 |
| IO90PB2F8 | E27 |
| IO91NB2F8 | H26 |
| IO91PB2F8 | H25 |
| IO92NB2F8 | G28 |
| IO92PB2F8 | F28 |
| IO93NB2F8 | J26 |
| IO93PB2F8 | J25 |
| IO94NB2F8 | H27 |
| IO94PB2F8 | G27 |
| IO95NB2F8 | H29 |
| IO95PB2F8 | G29 |
| IO96NB2F9 | G30 |
| IO96PB2F9 | F30 |
| IO97NB2F9 | K25 |
| IO97PB2F9 | K24 |
| IO98NB2F9 | J28 |
| IO98PB2F9 | H28 |
| IO99NB2F9 | L23 |
| IO99PB2F9 | L24 |
| IO100NB2F9 | K27 |
| IO100PB2F9 | J27 |
| IO101PB2F9 | J30 |
| IO102NB2F9 | E30 |

| FG896 | |
|---|---|
| AX2000 Function | Pin Number |
| IO102PB2F9 | D30 |
| IO103NB2F9 | L26 |
| IO103PB2F9 | K26 |
| IO104NB2F9 | F29 |
| IO105NB2F9 | M25 |
| IO105PB2F9 | L25 |
| IO106NB2F9 | K30 |
| IO106PB2F9 | K29 |
| IO107NB2F10 | M23 |
| IO107PB2F10 | M24 |
| IO109NB2F10 | M27 |
| IO109PB2F10 | L27 |
| IO110NB2F10 | M28 |
| IO110PB2F10 | L28 |
| IO111NB2F10 | N22 |
| IO111PB2F10 | N23 |
| IO112NB2F10 | M29 |
| IO112PB2F10 | L29 |
| IO113NB2F10 | N26 |
| IO113PB2F10 | M26 |
| IO114NB2F10 | M30 |
| IO114PB2F10 | L30 |
| IO115NB2F10 | N28 |
| IO115PB2F10 | N27 |
| IO117NB2F10 | N25 |
| IO117PB2F10 | N24 |
| IO118NB2F11 | N29 |
| IO119NB2F11 | P22 |
| IO119PB2F11 | P23 |
| IO121NB2F11 | P25 |
| IO121PB2F11 | P24 |
| IO122NB2F11 | P28 |
| IO122PB2F11 | P27 |
| IO123NB2F11 | R26 |
| IO123PB2F11 | P26 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| IO259NB6F24 | AF7 |
| IO259PB6F24 | AG7 |
| IO260NB6F24 | AH3 |
| IO260PB6F24 | AH4 |
| IO261NB6F24 | AH5 |
| IO261PB6F24 | AJ5 |
| IO262NB6F24 | AE6 |
| IO262PB6F24 | AF6 |
| IO263NB6F24 | AF5 |
| IO263PB6F24 | AG5 |
| IO264NB6F24 | AD8 |
| IO264PB6F24 | AE8 |
| IO265NB6F24 | AF3 |
| IO265PB6F24 | AG3 |
| IO266NB6F24 | AC10 |
| IO266PB6F24 | AD10 |
| IO267NB6F25 | AD7 |
| IO267PB6F25 | AE7 |
| IO268NB6F25 | AD5 |
| IO268PB6F25 | AE5 |
| IO269NB6F25 | AE4 |
| IO269PB6F25 | AF4 |
| IO270NB6F25 | AB9 |
| IO270PB6F25 | AC9 |
| IO271NB6F25 | AC6 |
| IO271PB6F25 | AD6 |
| IO272NB6F25 | AB8 |
| IO272PB6F25 | AC8 |
| IO273NB6F25 | AE1 |
| IO273PB6F25 | AE2 |
| IO274NB6F25 | AA10 |
| IO274PB6F25 | AB10 |
| IO275NB6F25 | AB7 |
| IO275PB6F25 | AC7 |
| IO276NB6F25 | AD1 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| IO276PB6F25 | AD2 |
| IO277NB6F25 | AC4 |
| IO277PB6F25 | AC3 |
| IO278NB6F26 | AA8 |
| IO278PB6F26 | AA9 |
| IO279NB6F26 | AB5 |
| IO279PB6F26 | AB6 |
| IO280NB6F26 | Y10 |
| IO280PB6F26 | Y11 |
| IO281NB6F26 | AB3 |
| IO281PB6F26 | AB4 |
| IO282NB6F26 | Y7 |
| IO282PB6F26 | AA7 |
| IO283NB6F26 | AC2 |
| IO283PB6F26 | AC1 |
| IO284NB6F26 | Y9 |
| IO284PB6F26 | Y8 |
| IO285NB6F26 | AA5 |
| IO285PB6F26 | AA6 |
| IO286NB6F26 | W10 |
| IO286PB6F26 | W11 |
| IO287NB6F26 | AA3 |
| IO287PB6F26 | AA4 |
| IO288NB6F26 | W9 |
| IO288PB6F26 | W8 |
| IO289NB6F27 | AA1 |
| IO289PB6F27 | AA2 |
| IO290NB6F27 | W6 |
| IO290PB6F27 | Y6 |
| IO291NB6F27 | W5 |
| IO291PB6F27 | Y5 |
| IO292NB6F27 | V7 |
| IO292PB6F27 | W7 |
| IO293NB6F27 | W4 |
| IO293PB6F27 | Y4 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| IO294NB6F27 | V10 |
| IO294PB6F27 | V11 |
| IO295NB6F27 | Y1 |
| IO295PB6F27 | Y2 |
| IO296NB6F27 | W1 |
| IO296PB6F27 | W2 |
| IO297NB6F27 | V1 |
| IO297PB6F27 | V2 |
| IO298NB6F27 | V9 |
| IO298PB6F27 | V8 |
| IO299NB6F27 | U4 |
| IO299PB6F27 | V4 |
| **Bank 7** | |
| IO300NB7F28 | U10 |
| IO300PB7F28 | U11 |
| IO301NB7F28 | U2 |
| IO301PB7F28 | U1 |
| IO302NB7F28 | U6 |
| IO302PB7F28 | U7 |
| IO303NB7F28 | T3 |
| IO303PB7F28 | U3 |
| IO304NB7F28 | U9 |
| IO304PB7F28 | U8 |
| IO305NB7F28 | R2 |
| IO305PB7F28 | R1 |
| IO306NB7F28 | R4 |
| IO306PB7F28 | T4 |
| IO307NB7F28 | R5 |
| IO307PB7F28 | T5 |
| IO308NB7F28 | T11 |
| IO308PB7F28 | T10 |
| IO309NB7F28 | T6 |
| IO309PB7F28 | T7 |
| IO310NB7F29 | T9 |
| IO310PB7F29 | T8 |

| CQ256 | |
|---|---|
| AX2000 Function | Pin Number |
| IO242NB5F22 | 74 |
| IO242PB5F22 | 75 |
| IO243NB5F22 | 70 |
| IO243PB5F22 | 71 |
| IO244NB5F22 | 68 |
| IO244PB5F22 | 69 |
| **Bank 6** | |
| IO257PB6F24 | 60 |
| IO258NB6F24 | 58 |
| IO258PB6F24 | 59 |
| **Bank 6** | |
| IO279NB6F26 | 56 |
| IO279PB6F26 | 57 |
| IO280NB6F26 | 52 |
| IO280PB6F26 | 53 |
| IO281NB6F26 | 50 |
| IO281PB6F26 | 51 |
| IO282NB6F26 | 46 |
| IO282PB6F26 | 47 |
| IO284NB6F26 | 44 |
| IO284PB6F26 | 45 |
| IO285NB6F26 | 40 |
| IO285PB6F26 | 41 |
| IO286NB6F26 | 38 |
| IO286PB6F26 | 39 |
| IO287NB6F26 | 34 |
| IO287PB6F26 | 35 |
| **Bank 7 9** | |
| IO310NB7F29 | 30 |
| IO310PB7F29 | 31 |
| IO311NB7F29 | 26 |
| IO311PB7F29 | 27 |
| IO312NB7F29 | 24 |
| IO312PB7F29 | 25 |
| IO315NB7F29 | 20 |

| CQ256 | |
|---|---|
| AX2000 Function | Pin Number |
| IO315PB7F29 | 21 |
| IO316NB7F29 | 18 |
| IO316PB7F29 | 19 |
| IO317NB7F29 | 14 |
| IO317PB7F29 | 15 |
| IO318NB7F29 | 12 |
| IO318PB7F29 | 13 |
| IO320NB7F29 | 8 |
| IO320PB7F29 | 9 |
| **Bank 7** | |
| IO341NB7F31 | 6 |
| IO341PB7F31 | 7 |
| **Dedicated I/O** | |
| GND | 1 |
| GND | 5 |
| GND | 11 |
| GND | 17 |
| GND | 23 |
| GND | 29 |
| GND | 33 |
| GND | 37 |
| GND | 43 |
| GND | 49 |
| GND | 55 |
| GND | 62 |
| GND | 64 |
| GND | 65 |
| GND | 73 |
| GND | 79 |
| GND | 85 |
| GND | 91 |
| GND | 97 |
| GND | 103 |
| GND | 109 |
| GND | 115 |

| CQ256 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | 121 |
| GND | 128 |
| GND | 129 |
| GND | 132 |
| GND | 139 |
| GND | 145 |
| GND | 151 |
| GND | 157 |
| GND | 161 |
| GND | 165 |
| GND | 171 |
| GND | 177 |
| GND | 183 |
| GND | 190 |
| GND | 192 |
| GND | 193 |
| GND | 201 |
| GND | 207 |
| GND | 213 |
| GND | 219 |
| GND | 225 |
| GND | 231 |
| GND | 239 |
| GND | 245 |
| GND | 256 |
| PRA | 227 |
| PRB | 226 |
| PRC | 99 |
| PRD | 98 |
| TCK | 253 |
| TDI | 252 |
| TDO | 250 |
| TMS | 254 |
| TRST | 255 |
| VCCA | 3 |

| CQ352 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | 21 |
| GND | 27 |
| GND | 33 |
| GND | 39 |
| GND | 45 |
| GND | 51 |
| GND | 57 |
| GND | 63 |
| GND | 69 |
| GND | 75 |
| GND | 81 |
| GND | 88 |
| GND | 89 |
| GND | 97 |
| GND | 103 |
| GND | 109 |
| GND | 115 |
| GND | 121 |
| GND | 133 |
| GND | 145 |
| GND | 151 |
| GND | 157 |
| GND | 163 |
| GND | 169 |
| GND | 176 |
| GND | 177 |
| GND | 186 |
| GND | 192 |
| GND | 198 |
| GND | 204 |
| GND | 210 |
| GND | 216 |
| GND | 222 |
| GND | 228 |
| GND | 234 |

| CQ352 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | 240 |
| GND | 246 |
| GND | 252 |
| GND | 258 |
| GND | 264 |
| GND | 265 |
| GND | 274 |
| GND | 280 |
| GND | 286 |
| GND | 292 |
| GND | 298 |
| GND | 310 |
| GND | 322 |
| GND | 330 |
| GND | 334 |
| GND | 340 |
| GND | 345 |
| GND | 352 |
| PRA | 312 |
| PRB | 311 |
| PRC | 135 |
| PRD | 134 |
| TCK | 349 |
| TDI | 348 |
| TDO | 347 |
| TMS | 350 |
| TRST | 351 |
| VCCA | 3 |
| VCCA | 14 |
| VCCA | 32 |
| VCCA | 56 |
| VCCA | 74 |
| VCCA | 87 |
| VCCA | 102 |
| VCCA | 114 |

| CQ352 | |
|---|---|
| AX2000 Function | Pin Number |
| VCCA | 150 |
| VCCA | 162 |
| VCCA | 175 |
| VCCA | 191 |
| VCCA | 209 |
| VCCA | 233 |
| VCCA | 251 |
| VCCA | 263 |
| VCCA | 279 |
| VCCA | 291 |
| VCCA | 329 |
| VCCA | 339 |
| VCCDA | 2 |
| VCCDA | 44 |
| VCCDA | 90 |
| VCCDA | 91 |
| VCCDA | 116 |
| VCCDA | 117 |
| VCCDA | 130 |
| VCCDA | 131 |
| VCCDA | 132 |
| VCCDA | 148 |
| VCCDA | 149 |
| VCCDA | 174 |
| VCCDA | 178 |
| VCCDA | 221 |
| VCCDA | 266 |
| VCCDA | 268 |
| VCCDA | 293 |
| VCCDA | 294 |
| VCCDA | 307 |
| VCCDA | 308 |
| VCCDA | 309 |
| VCCDA | 327 |
| VCCDA | 328 |

# 4 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Revision | Changes | Page |
|---|---|---|
| Revision 18 (March 2012) | Table 2-1 • Absolute Maximum Ratings was updated to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419). | 2-1 |
| | Values for tristate leakage current IOZ, and IIH and IIL were added to Table 2-3 • Standby Current (SARs 35774, 32021). | 2-2 |
| | Figure 2-2 • VCCPLX and VCOMPLX Power Supply Connect was updated to correct the units for the resistance from "W" to Ω (SAR 36415). | 2-9 |
| | In the Introduction to the "User I/Os" section, the following sentence was added to clarify the slew rate setting (SAR 34943):<br>The slew rate setting is effective for both rising and falling edges. | 2-11 |
| | Figure 2-3 • Use of an External Resistor for 5 V Tolerance was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942). | 2-13 |
| | EQ 3 for 5 V tolerance was corrected to change Vdiode from 0.6 V to 0.7 V (SAR 36786). | 2-13 |
| | Additional information was added to the "Using the Weak Pull-Up and Pull-Down Circuits" section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945). | 2-17 |
| | The description for the $C_{INCLK}$ parameter in Table 2-18 • Input Capacitance was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944). | 2-21 |
| | Table 2-19 • I/O Input Rise Time and Fall Time* is new (SAR 34942). | 2-21 |
| | The minimum VIL for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-29 • DC Input and Output Levels and Table 2-33 • DC Input and Output Levels (SAR 34358). | 2-38, 2-40 |
| | Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the *Antifuse Macro Library Guide* was added to the "R-Cell" section (SAR 26413). | 2-58 |
| | The enable signal in Figure 2-32 • R-Cell Delays was corrected to show it is active low rather than active high (SAR 34946). | 2-59 |
| Revision 17 (September 2011) | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Axcelerator Family Device Status" table indicates the status for each device in the device family. | iii |
| | The "Features" section, "Programmable Interconnect Element" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865). | i, 1-1, 2-108 |