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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2016
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	168
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax125-1fg324

Poutputs = PI/O * po * Fpo

C_{load} = the output load (technology dependent)
VCCI = the output voltage (technology dependent)
po = the number of outputs
F_{po} = the average output frequency

Pmemory = P11 * Nblock * FRCLK + P12 * Nblock * FWCLK

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
F_{RCLK} = the read-clock frequency of the memory
F_{WCLK} = the write-clock frequency of the memory

PPLL = P13 * FCLK

F_{RefCLK} = the clock frequency of the clock input of the PLL
F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
Fs = 100 MHz
s = 1080
=> P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs = 79 mW
and Fs = 100 MHz
=> $P_{R\text{-}cells}$ = P7 * ms * Fs = 173 mW
mc = 1 (1 C-cell in this shift-register)
and Fs = 100 MHz
=> $P_{C\text{-}cells}$ = P8 * mc * Fs = 0.14 mW
F_{pi} ~ 0 MHz
and pi= 1 (1 reset input => this is why F_{pi}=0)
=> P_{inputs} = P9 * pi * F_{pi} = 0 mW
F_{po} = 50 MHz
and po = 1
=> $P_{outputs}$ = $P_{I/O}$ * po * F_{po}= 27.10 mW
No RAM/FIFO in this shift-register
=> P_{memory} = 0 mW
No PLL in this shift-register
=> P_{PLL} = 0 mW
$P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$ = 276 mW
P_{dc} = 7.5mA * 1.5V = 11.25 mW
$P_{total} = P_{dc} + P_{ac}$ = 11.25 mW + 276mW = 290.30 mW

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

Table 2-11 • **Compatible I/O Standards for Different VREF Values**

VREF	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5V and 3.3V Outputs)
0.75 V	HSTL (Class I)

Table 2-12 • **Compatible I/O Standards for Different VCCI Values**

VCCI[1]	Compatible Standards	VREF
3.3 V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVCMOS 2.5 V, GTL+ 2.5 V, LVDS[2]	1.0
2.5 V	LVCMOS 2.5 V, SSTL 2 (Classes I and II), LVDS[2]	1.25
1.8 V	LVCMOS 1.8 V	N/A
1.5 V	LVCMOS 1.5 V, HSTL Class I	0.75

Notes:

1. *VCCI is used for both inputs and outputs*
2. *VCCI tolerance is* ±5%

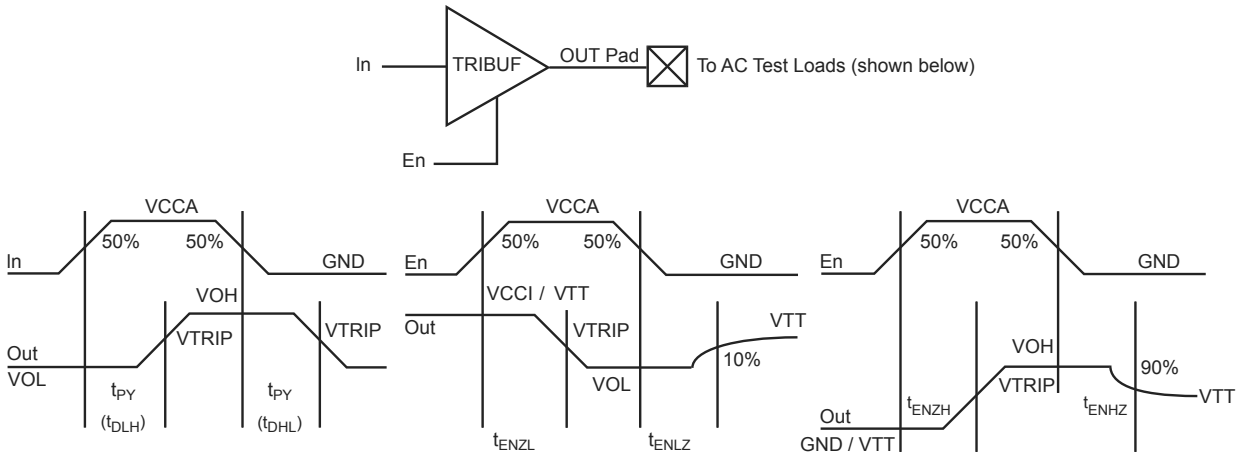


Figure 2-10 • **Output Buffer Delays**

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength =3 (16 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		11.03		12.56		14.77	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		11.42		13.01		15.29	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		11.04		12.58		14.79	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.86		1.88		1.88	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.50		2.51		2.52	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 4 (24mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		2.99		3.41		4.01	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.49		2.51		2.51	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.59		2.95		3.46	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.56		4.06		4.77	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, –3.5 V in undershoot, and 7.1 V in overshoot.

***Table 2-33* • DC Input and Output Levels**

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
PCI	–0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	–0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

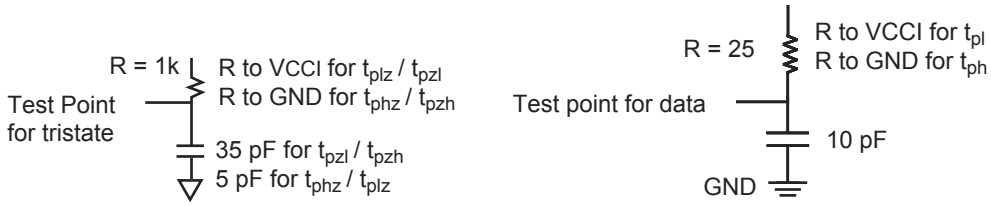


***Figure 2-18 •* AC Test Loads**

***Table 2-34* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

*Note: * Measuring Point = VTRIP*

Routing Specifications

Routing Resources

The routing structure found in Axcelerator devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the AX architecture: DirectConnect, CarryConnect, FastConnect, and Vertical and Horizontal Routing.

DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 2-35). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

Figure 2-35 • **DirectConnect and CarryConnect**

CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (Figure 2-35). The FCO output of the right C-cell of a two-C-cell Cluster drives the FCI input of the left C-cell in the two-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two-C-cell cluster to the FCI of the two-C-cell cluster immediately below it (see the "Carry-Chain Logic" section on page 2-56 for more information).

FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 2-36 on page 2-62). FastConnects provide a maximum delay of 0.3 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

single-ended, or voltage-referenced standard. The [H]CLKxN pad can only be used as a differential pair with [H]CLKxP.

The block marked “/i Delay Match” is a fixed delay equal to that of the i divider. The “/j Delay Match” block has the same function as its j divider counterpart.

Functional Description

Figure 2-48 on page 2-75 illustrates a block diagram of the PLL. The PLL contains two dividers, i and j, that allow frequency scaling of the clock signal:

- The i divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64, and the resultant frequency is available at the output of the PLL block.
- The j divider divides the PLL output by integer factors ranging from 1 to 64, and the divided clock is available at CLK1.
- The two dividers together can implement any combination of multiplication and division up to a maximum frequency of 1 GHz on CLK1. Both the CLK1 and CLK2 outputs have a fixed 50/50 duty cycle.
- The output frequencies of the two clocks are given by the following formulas (f_{REF} is the reference clock frequency):

$$f_{CLK1} = f_{REF} * (DividerI) / (DividerJ)$$

EQ 4

$$f_{CLK2} = f_{REF} * (DividerI)$$

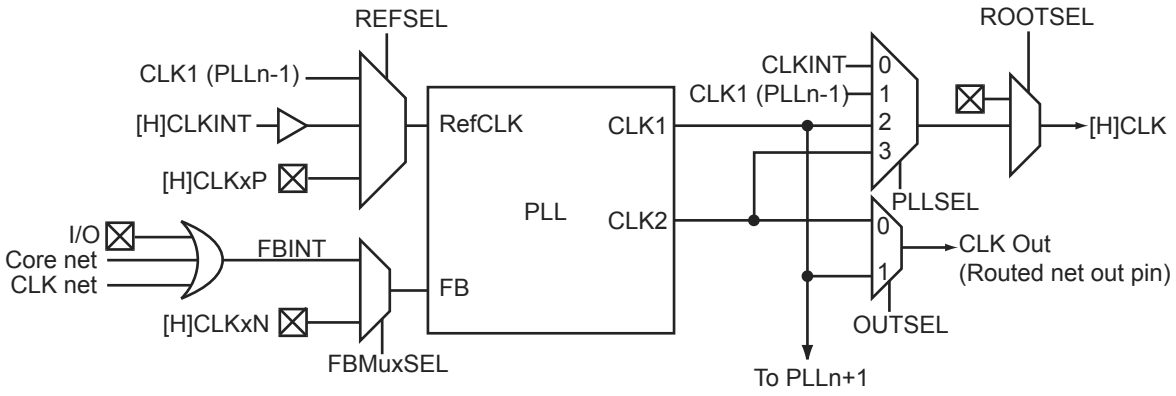
EQ 5

- CLK2 provides the PLL output directly—without division

The input and output frequency ranges are selected by LowFreq and Osc(2:0), respectively. These functions and their possible values are detailed in Table 2-80 on page 2-77.

The delay lines shown in Figure 2-48 on page 2-75 are programmable. The feedback clock path can be delayed (using the five DelayLine bits) relative to the reference clock (or vice versa) by up to 3.75 ns in increments of 250 ps. Table 2-80 on page 2-77 describes the usage of these bits. The delay increments are independent of frequency, so this results in phase changes that vary with frequency. The delay value is highly dependent on V_{CC} and the speed grade.

Figure 2-49 is a logical diagram of the various control signals to the PLL and shows how the PLL interfaces with the global and routing networks of the FPGA. Note that not all signals are user-accessible. These non-user-accessible signals are used by the place-and-route tool to control the configuration of the PLL. The user gains access to these control signals either based upon the connections built in the user's design or through the special macros (Table 2-84 on page 2-81) inserted into the design. For example, connecting the macro PLLOUT to CLK2 will control the OUTSEL signal.



Note: Not all signals are available to the user.

Figure 2-49 • **PLL Logical Interface**

***Table 2-83* • South PLL Connections**

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

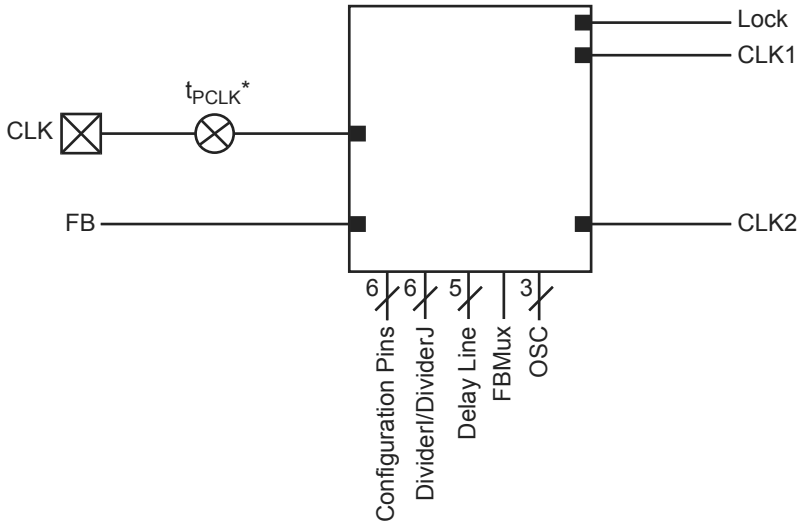
Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model



Note: t_{PCLK} is the delay in the clock signal

Figure 2-52 • **PLL Model**

***Table 2-93* • Sixteen RAM Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	13.40		13.40		13.40		ns
t_{WCKP}	WCLK Minimum Period	14.15		14.15		14.15		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		18.13		20.65		24.27	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		18.13		20.65		24.27	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		12.83		14.62		17.18	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	14.41		14.41		14.41		ns
t_{RCKP}	RCLK Minimum Period	15.14		15.14		15.14		ns

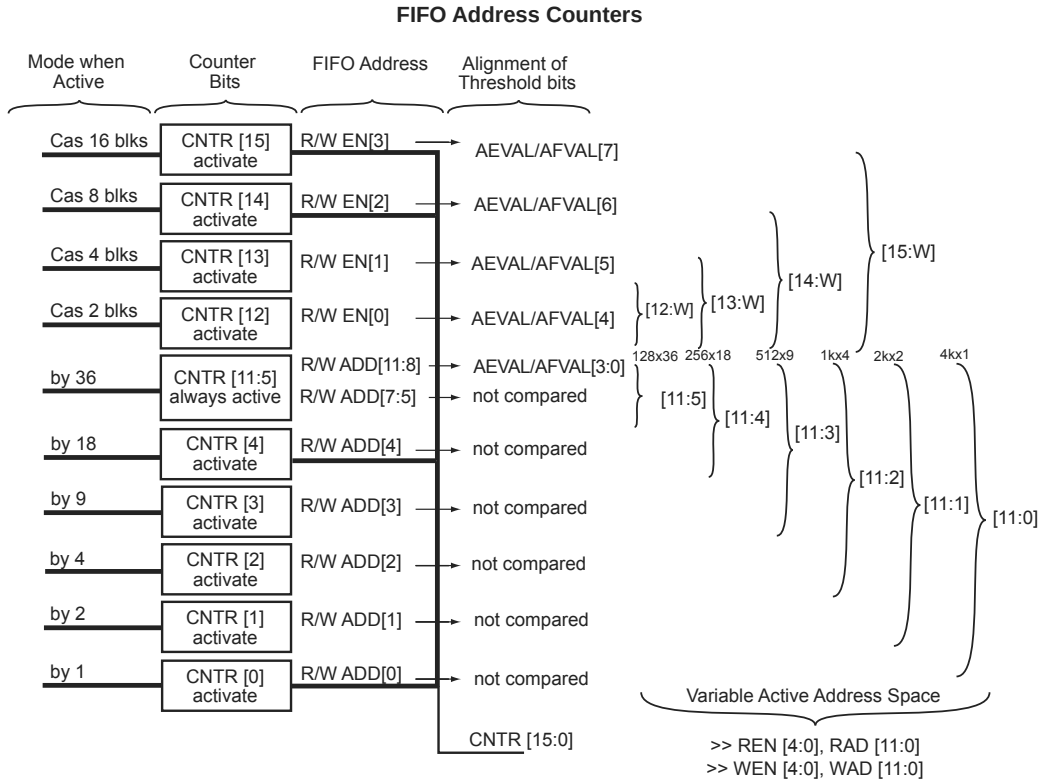
Note: Timing data for these sixteen cascaded RAM blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

FIFO Flag Logic

The FIFO is user configurable into various DEPTHs and WIDTHs. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.



Note: Inactive counter bits are set to zero.

Figure 2-62 • **FIFO Address Counters**

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

Table 2-94 • **FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

BG729	
AX1000 Function	Pin Number
IO218PB6F20	V2
IO219NB6F20	T1
IO219PB6F20	U1
IO220NB6F20	R5
IO220PB6F20	R6
IO221NB6F20	T3
IO221PB6F20	T4
IO222NB6F20	R2
IO222PB6F20	T2
IO223NB6F20	P8
IO223PB6F20	P9
IO224NB6F20	R3
IO224PB6F20	R4
Bank 7	
IO225NB7F21	P1
IO225PB7F21	R1
IO226NB7F21	P3
IO226PB7F21	P2
IO227NB7F21	N7
IO227PB7F21	P7
IO228NB7F21	P5
IO228PB7F21	P4
IO229NB7F21	N2
IO229PB7F21	N1
IO230NB7F21	N6
IO230PB7F21	P6
IO231NB7F21	N9
IO231PB7F21	N8
IO232NB7F21	N4
IO232PB7F21	N3
IO233NB7F21	M2
IO233PB7F21	M1
IO234NB7F21	M4
IO234PB7F21	M3
IO235NB7F21	M5
IO235PB7F21	N5
IO236NB7F22	L2

BG729	
AX1000 Function	Pin Number
IO236PB7F22	L1
IO237NB7F22	L4
IO237PB7F22	L3
IO238NB7F22	L6
IO238PB7F22	M6
IO239NB7F22	M8
IO239PB7F22	M7
IO240NB7F22	K2
IO240PB7F22	K1
IO241NB7F22	K4
IO241PB7F22	K3
IO242NB7F22	K5
IO242PB7F22	L5
IO243NB7F22	J2
IO243PB7F22	J1
IO244NB7F22	J4
IO244PB7F22	J3
IO245NB7F22	H2
IO245PB7F22	H1
IO246NB7F22	H4
IO246PB7F22	H3
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	J6
IO248PB7F23	K6
IO249NB7F23	H5
IO249PB7F23	J5
IO250NB7F23	G2
IO250PB7F23	G1
IO251NB7F23	K8
IO251PB7F23	K7
IO252NB7F23	G4
IO252PB7F23	G3
IO253NB7F23	F2
IO253PB7F23	F1
IO254NB7F23	G6
IO254PB7F23	H6

BG729	
AX1000 Function	Pin Number
IO255NB7F23	F5
IO255PB7F23	G5
IO256NB7F23	F3
IO256PB7F23	F4
IO257NB7F23	H7
IO257PB7F23	J7
Dedicated I/O	
GND	A1
GND	A2
GND	A25
GND	A26
GND	A27
GND	A3
GND	AC24
GND	AE1
GND	AE2
GND	AE25
GND	AE26
GND	AE27
GND	AE3
GND	AE5
GND	AF1
GND	AF2
GND	AF25
GND	AF26
GND	AF27
GND	AF3
GND	AG1
GND	AG2
GND	AG25
GND	AG26
GND	AG27
GND	AG3
GND	B1
GND	B2
GND	B25
GND	B26

FG324	
AX125 Function	**Pin Number**
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG484	
AX250 Function	**Pin Number**
Bank 0	
IO00NB0F0	D7
IO00PB0F0	D6
IO01NB0F0	E7
IO01PB0F0	E6
IO02NB0F0	C5
IO02PB0F0	C4
IO03NB0F0	C7
IO03PB0F0	C6
IO04NB0F0	E9
IO04PB0F0	E8
IO05NB0F0	D9
IO05PB0F0	D8
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0	C9
IO07PB0F0	C8
IO08NB0F0	A7
IO08PB0F0	A6
IO09NB0F0	B9
IO09PB0F0	B8
IO10NB0F0	A9
IO10PB0F0	A8
IO11NB0F0	B10
IO11PB0F0	A10
IO12NB0F0/HCLKAN	E11
IO12PB0F0/HCLKAP	E10
IO13NB0F0/HCLKBN	D12
IO13PB0F0/HCLKBP	D11
Bank 1	
IO14NB1F1/HCLKCN	F13
IO14PB1F1/HCLKCP	F12
IO15NB1F1/HCLKDN	E14
IO15PB1F1/HCLKDP	E13
IO16NB1F1	C13
IO16PB1F1	C12

FG484	
AX250 Function	**Pin Number**
IO17NB1F1	B14
IO17PB1F1	B13
IO18NB1F1	A14
IO18PB1F1	A13
IO19NB1F1	A16
IO19PB1F1	A15
IO20NB1F1	B16
IO20PB1F1	B15
IO21NB1F1	C17
IO21PB1F1	C16
IO22NB1F1	F15
IO22PB1F1	F14
IO23NB1F1	D16
IO23PB1F1	D15
IO24NB1F1	E16
IO24PB1F1	E15
IO25NB1F1	F18
IO25PB1F1	F17
IO26NB1F1	D18
IO26PB1F1	E17
IO27NB1F1	G16
IO27PB1F1	G15
Bank 2	
IO28NB2F2	F19
IO28PB2F2	E19
IO29NB2F2	J16
IO29PB2F2	H16
IO30NB2F2	E20
IO30PB2F2	D20
IO31NB2F2	J17
IO31PB2F2	H17
IO32NB2F2	G20
IO32PB2F2	F20
IO33NB2F2	H19
IO33PB2F2	G19
IO34NB2F2	E22

FG484	
AX250 Function	**Pin Number**
IO34PB2F2	D22
IO35NB2F2	J18
IO35PB2F2	H18
IO36NB2F2	G21
IO36PB2F2	F21
IO37NB2F2	K19
IO37PB2F2	J19
IO38NB2F2	J20
IO38PB2F2	H20
IO39NB2F2	L16
IO39PB2F2	K16
IO40NB2F2	J21
IO40PB2F2	H21
IO41NB2F2	L17
IO41PB2F2	K17
IO42NB2F2	J22
IO42PB2F2	H22
IO43NB2F2	L18
IO43PB2F2	K18
IO44NB2F2	L20
IO44PB2F2	K20
Bank 3	
IO45NB3F3	M19
IO45PB3F3	L19
IO46NB3F3	M21
IO46PB3F3	L21
IO47NB3F3	N17
IO47PB3F3	M17
IO48NB3F3	N18
IO48PB3F3	N19
IO49NB3F3	N16
IO49PB3F3	M16
IO50NB3F3	N20
IO50PB3F3	M20
IO51NB3F3	P21
IO51PB3F3	N21

FG676	
AX500 Function	**Pin Number**
IO153PB7F14	M6
IO154NB7F14	K2
IO154PB7F14	L2
IO155NB7F14	K3
IO155PB7F14	L3
IO156NB7F14	L5
IO156PB7F14	L4
IO157NB7F14	L6
IO157PB7F14	L7
IO158NB7F15	J1
IO158PB7F15	K1
IO159NB7F15	J4
IO159PB7F15	K4
IO160NB7F15	H2
IO160PB7F15	J2
IO161NB7F15	K6
IO161PB7F15	K5
IO162NB7F15	H3
IO162PB7F15	J3
IO163NB7F15	G2
IO163PB7F15	G1
IO164NB7F15	G4
IO164PB7F15	H4
IO165NB7F15	F3
IO165PB7F15	G3
IO166NB7F15	E2
IO166PB7F15	F2
IO167NB7F15	F5
IO167PB7F15	G5
Dedicated I/O	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26

FG676	
AX500 Function	**Pin Number**
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10

FG676	
AX500 Function	**Pin Number**
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26

FG896	
AX2000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX2000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	Pin Number
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

FG1152	
AX2000 Function	Pin Number
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H31
NC	H33
NC	J1
NC	J3
NC	J34
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17

FG1152	
AX2000 Function	Pin Number
PRB	F18
PRC	AD18
PRD	AH18
TCK	J9
TDI	F7
TDO	L10
TMS	H8
TRST	E6
VCCA	AA13
VCCA	AA22
VCCA	AB14
VCCA	AB15
VCCA	AB16
VCCA	AB17
VCCA	AB18
VCCA	AB19
VCCA	AB20
VCCA	AB21
VCCA	AF8
VCCA	AK28
VCCA	G30
VCCA	G5
VCCA	N14
VCCA	N15
VCCA	N16
VCCA	N17
VCCA	N18
VCCA	N19
VCCA	N20
VCCA	N21
VCCA	P13
VCCA	P22
VCCA	R13
VCCA	R22
VCCA	T13

FG1152	
AX2000 Function	Pin Number
VCCA	T22
VCCA	U13
VCCA	U22
VCCA	V13
VCCA	V22
VCCA	W13
VCCA	W22
VCCA	Y13
VCCA	Y22
VCCDA	AF26
VCCDA	AF9
VCCDA	AG17
VCCDA	AG18
VCCDA	AH14
VCCDA	AH15
VCCDA	AH17
VCCDA	AH20
VCCDA	AH21
VCCDA	AK29
VCCDA	AK6
VCCDA	E15
VCCDA	E29
VCCDA	E7
VCCDA	F15
VCCDA	F21
VCCDA	F5
VCCDA	G20
VCCDA	H17
VCCDA	H18
VCCDA	H28
VCCDA	J18
VCCDA	V27
VCCDA	V6
VCCIB0	A5
VCCIB0	B5

CQ352	
AX1000 Function	**Pin Number**
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX1000 Function	**Pin Number**
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

Revision	Changes	Page
Revision 8 (continued)	The following changes were made in the "FG676"(AX500) section: AE2, AE25 Change from NC to GND. AF2, AF25 Changed from GND to NC AB4, AF24, C1, C26 Changed from V_{CCDA} to V_{CCA} AD15 Change from V_{CCDA} to V_{COMPLE} AD17 Changed from V_{COMPLE} to V_{CCDA}	3-37
	In the "FG896" (AX2000) section, the AK28 changed from VCCIB5 to VCCIB4.	3-52
	The "CQ352" and "CG624" sections are new.	3-98, 3-115
Revision 7 (Advance v1.6)	All I/O FIFO capability was removed.	n/a
	Table 1 was updated.	i
	Figure 1-9 was updated.	1-7
	Figure 2-5 was updated.	2-16
	The "Using an I/O Register" section was updated.	2-16
	The AX250 and AX1000 descriptions were added to the "FG484"section.	3-21
Revision 6 (Advance v1.5)	Table 2-3 was updated.	2-2
	Figure 2-1 was updated.	2-8
	Figure 2-48 was updated.	2-75
	Figure 2-52 was updated.	2-82
Revision 5 (Advance v1.4)	In the "PQ208" table, pin 196 was missing, but it has been added in this version with a function of GND.	3-84
	The following pins in the "FG484" table for AX500 were changed: Pin G7 is GND/LP Pins AB8, C10, C11, C14, AB16 are NC.	3-21
	The "FG676" table was updated.	3-37
Revision 4 (Advance v1.3)	The "Device Resources" section was updated for the CS180.	ii
	The "Programmable Interconnect Element" and Figure 1-2 are new.	1-1 and 1-2
	The "CS180" table is new.	3-1
	The "PQ208" tables for the AX500 were updated. The following pins were not defined in the previous version: GND 21 IO106PB5F10/CLKHP 71 GND 136	3-84
Revision 3 (Advance v1.2)	Table 1, "Ordering Information", "Device Resources", and the Product Plan table were updated.	i, ii
	The following figures and tables were updated: Figure 1-3 Figure 1-8 (new) Table 2-3 Figure 2-2 Table 2-8 Figure 2-11	 1-2 1-6 2-2 2-9 2-12 2-23
	The "Design Environment" section was updated.	1-7
	The "Package Thermal Characteristics" was updated.	2-6