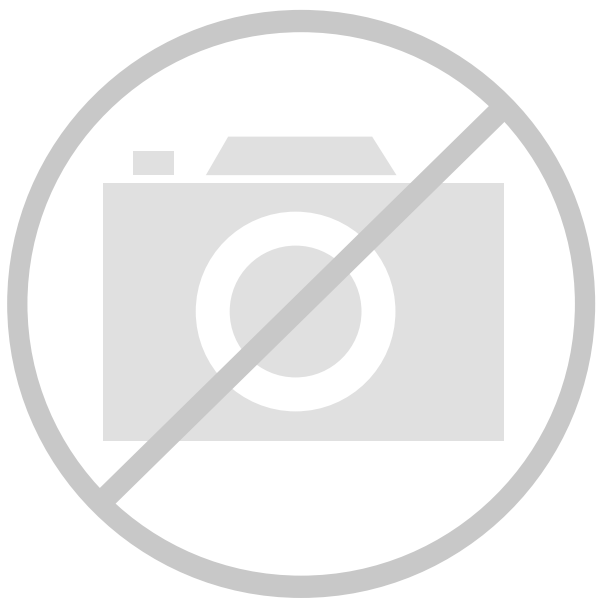




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2016
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	138
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax125-2fgg256i

Table 2-15, Table 2-16, and Table 2-17 list all the available macro names differentiated by I/O standard, type, slew rate, and drive strength.

Table 2-15 • Macros for Single-Ended I/O Standards

Standard	VCCI	Macro Names
LVTTTL	3.3 V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_H_8, OUTBUF_H_12, OUTBUF_H_16, OUTBUF_H_24, TRIBUF, TRIBUF_S_8, TRIBUF_S_12, TRIBUF_S_16, TRIBUF_S_24, TRIBUF_H_8, TRIBUF_H_12, TRIBUF_H_16, TRIBUF_H_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_H_8, BIBUF_H_12, BIBUF_H_16, BIBUF_H_24
3.3 V PCI	3.3 V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUF_PCI, BIBUF_PCI
3.3 V PCI-X	3.3 V	CLKBUF_PCI-X, HCLKBUF_PCI-X, INBUF_PCI-X, OUTBUF_PCI-X, TRIBUF_PCI-X, BIBUF_PCI-X
LVC MOS25	2.5 V	CLKBUF_LVC MOS25, HCLKBUF_LVC MOS25, INBUF_LVC MOS25, OUTBUF_LVC MOS25, TRIBUF_LVC MOS25, BIBUF_LVC MOS25
LVC MOS18	1.8 V	CLKBUF_LVC MOS18, HCLKBUF_LVC MOS18, INBUF_LVC MOS18, OUTBUF_LVC MOS18, TRIBUF_LVC MOS18, BIBUF_LVC MOS18
LVC MOS15 (JESD8-11)	1.5 V	CLKBUF_LVC MOS15, HCLKBUF_LVC MOS15, INBUF_LVC MOS15, OUTBUF_LVC MOS15, TRIBUF_LVC MOS15, BIBUF_LVC MOS15

Table 2-16 • I/O Macros for Differential I/O Standards

Standard	VCCI	Macro Names
LVPECL	3.3 V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL
LVDS	2.5 V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS

Table 2-17 • I/O Macros for Voltage-Referenced I/O Standards

Standard	VCCI	VREF	Macro Names
GTL+	3.3 V	1.0 V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUF_GTP33, BIBUF_GTP33
GTL+	2.5 V	1.0 V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUF_GTP25, BIBUF_GTP25
SSTL2 Class I	2.5 V	1.25 V	CLKBUF_SSTL2_I, HCLKBUF_SSTL2_I, INBUF_SSTL2_I, OUTBUF_SSTL2_I, TRIBUF_SSTL2_I, BIBUF_SSTL2_I
SSTL2 Class II	2.5 V	1.25 V	CLKBUF_SSTL2_II, HCLKBUF_SSTL2_II, INBUF_SSTL2_II, OUTBUF_SSTL2_II, TRIBUF_SSTL2_II, BIBUF_SSTL2_II
SSTL3 Class I	3.3 V	1.5 V	CLKBUF_SSTL3_I, HCLKBUF_SSTL3_I, INBUF_SSTL3_I, OUTBUF_SSTL3_I, TRIBUF_SSTL3_I, BIBUF_SSTL3_I
SSTL3 Class II	3.3 V	1.5 V	CLKBUF_SSTL3_II, HCLKBUF_SSTL3_II, INBUF_SSTL3_II, OUTBUF_SSTL3_II, TRIBUF_SSTL3_II, BIBUF_SSTL3_II
HSTL Class I	1.5 V	0.75 V	CLKBUF_HSTL_I, HCLKBUF_HSTL_I, INBUF_HSTL_I, OUTBUF_HSTL_I, TRIBUF_HSTL_I, BIBUF_HSTL_I

Table 2-36 • 3.3 V PCI-X I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI-X Output Module Timing								
t _{DP}	Input Buffer	1.57		1.79		2.10		ns
t _{PY}	Output Buffer	2.10		2.40		2.82		ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low	1.61		1.62		1.63		ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High	1.59		1.60		1.61		ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z	2.65		3.02		3.55		ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z	3.11		3.55		4.17		ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register	0.67		0.77		0.90		ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time	0.13		0.15		0.17		ns
t _{HASYN}	Asynchronous Removal Time	0.00		0.00		0.00		ns
t _{CLR}	Asynchronous Clear-to-Q	0.23		0.27		0.31		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.23		0.27		0.31		ns

Differential Standards

Physical Implementation

Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O Cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350 mV.

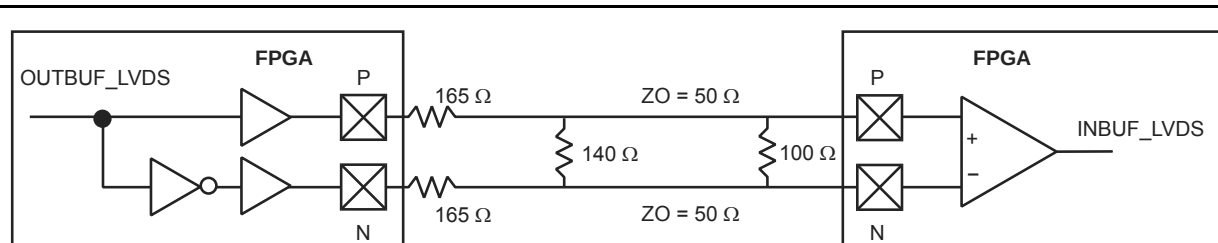


Figure 2-25 • LVDS Board-Level Implementation

The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2 V to 2.2 V for a differential input with 400 mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (note that the driver is not a current-mode driver). This driver provides a nominal constant current of 3.5 mA. When this current flows through a 100 Ω termination resistor on the receiver side, a voltage swing of 350 mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350 mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

Table 2-56 • DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI ¹	Supply Voltage	2.375	2.5	2.625	V
VOH	Output High Voltage	1.25	1.425	1.6	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM2	Input Common Mode Voltage	0.2	1.25	2.2	V

Notes:

1. $\pm 5\%$
2. Differential input voltage = ± 350 mV.

Module Specifications

C-Cell

Introduction

The C-cell is one of the two logic module types in the AX architecture. It is the combinatorial logic resource in the Axcelerator device. The AX architecture implements a new combinatorial cell that is an extension of the C-cell implemented in the SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The C-cell features the following (Figure 2-27):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns.
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns.

This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with Microsemi's extensive macro library (please see the *Antifuse Macro Library Guide* for a complete listing of available Axcelerator macros).

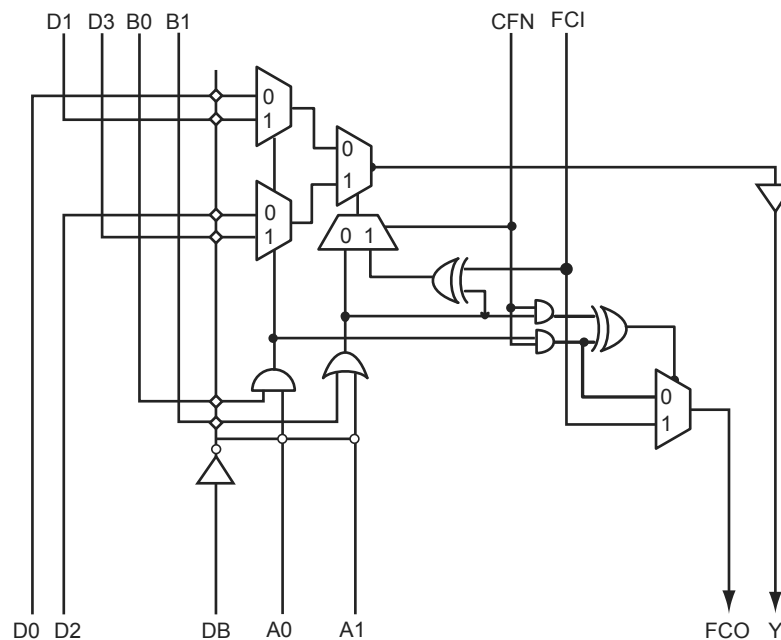


Figure 2-27 • C-Cell

Timing Model and Waveforms

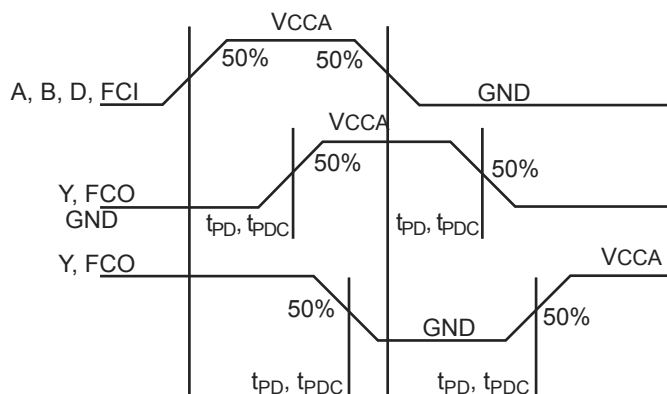


Figure 2-28 • C-Cell Timing Model and Waveforms

Timing Characteristics

Table 2-62 • C-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t _{PD}	Any input to output Y	0.74		0.84		0.99		ns
t _{PDC}	Any input to carry chain output (FCO)	0.57		0.64		0.76		ns
t _{PDB}	Any input through DB when one input is used	0.95		1.09		1.28		ns
t _{CCY}	Input to carry chain (FCI) to Y	0.61		0.69		0.82		ns
t _{CC}	Input to carry chain (FCI) to carry chain output (FCO)	0.08		0.09		0.11		ns

CLK1 and CLK2

Both PLL outputs, CLK1 and CLK2, can be used to drive a global resource, an adjacent PLL RefCLK input, or a net in the FPGA core. Not all drive combinations are possible (Table 2-81).

Table 2-81 • PLL General Connections Rules

CLK1	CLK2
HCLK	HCLK
CLK	CLK
HCLK	Routed net output
Routed net output	HCLK
HCLK	NONE
NONE	HCLK
CLK	NONE
NONE	CLK

Note: The PLL outputs remain Low when REFCLK is constant (either Low or High).

Restrictions on CLK1 and CLK2

- When both are driving global resources, they must be driving the same type of global resource (i.e. either HCLK or CLK).
- Only one can drive a routed net at any given time.

Table 2-82 and Table 2-83 specify all the possible CLK1 and CLK2 connections for the north and south PLLs. HCLK1 and HCLK2 are used to denote the different HCLK networks when two are being driven at the same time by a single PLL (Note that HCLK1 is the primary clock resource associated with the PLL, and HCLK2 is the clock resource associated with the adjacent PLL). Likewise, CLK1 and CLK2 are used to denote the different CLK networks when two are being driven at the same time by a single PLL (Figure 2-48 on page 2-75).

Table 2-82 • North PLL Connections

CLK1	CLK2
HCLK1	Routed net
HCLK1	Unused
HCLK2	HCLK1
HCLK2	Routed net
HCLK2	Both HCLK1 and routed net
HCLK2	Unused
Unused	HCLK1
Unused	Routed net
Unused	Both HCLK1 and routed net
Unused	Unused
Routed net	HCLK1
Routed net	Unused
Both HCLK1 and HCLK2	Routed net
Both HCLK1 and HCLK2	Unused
Both HCLK1 and routed net	Unusable
Both HCLK2 and routed net	HCLK1
Both HCLK2 and routed net	Unused
HCLK1, HCLK2, and routed net	Unusable

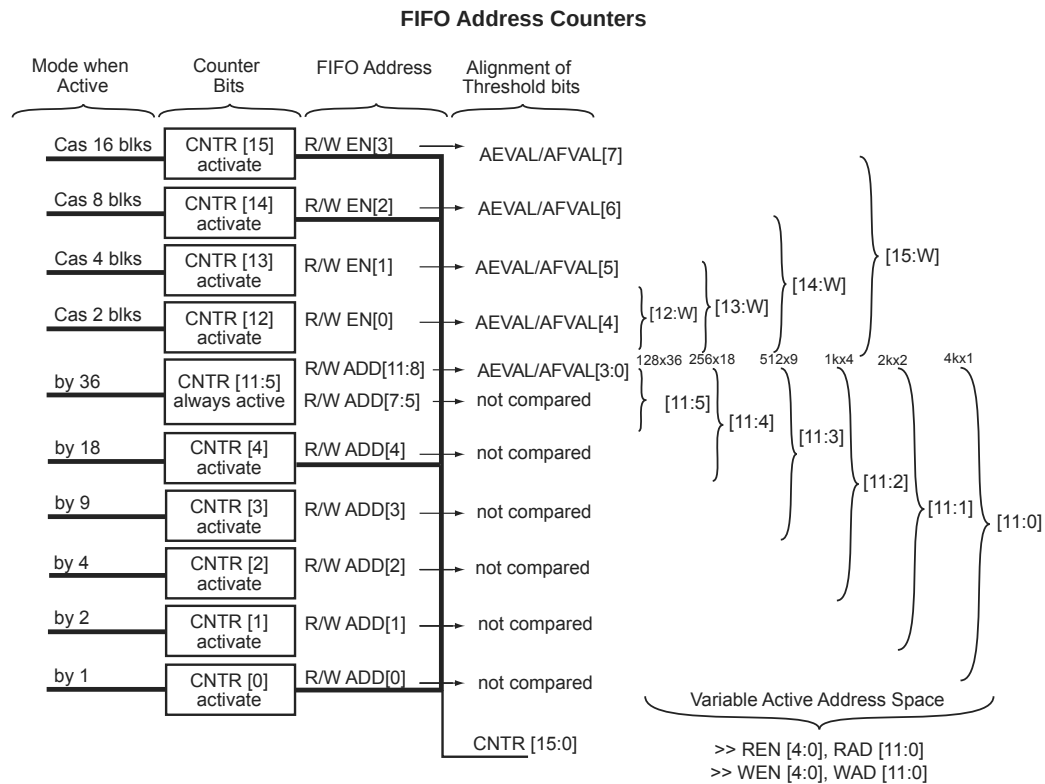
Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g. CLK1 driving HCLK1, and HCLK2 is not supported).

FIFO Flag Logic

The FIFO is user configurable into various DEPTHS and WIDTHS. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.



Note: Inactive counter bits are set to zero.

Figure 2-62 • FIFO Address Counters

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

Table 2-94 • FIFO Flag Logic

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] with AE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] with AE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] with AE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] with AE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] with AE/FVAL[7:0]

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 2-64). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 2-64).

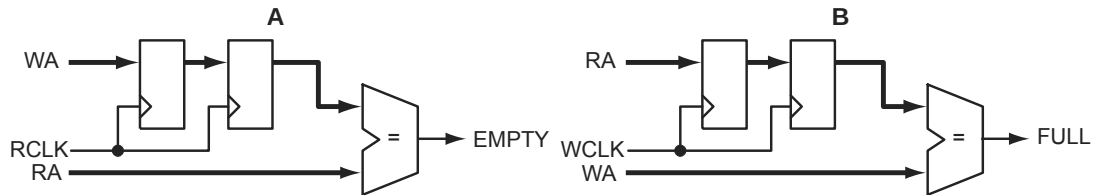


Figure 2-64 • Overflow and Underflow Control

FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 2-96.

Table 2-96 • FIFO Width Configurations

WIDTH(2:0)	W x D
000	1 x 4k
001	2 x 2k
010	4 x 1k
011	9 x 512
100	18 x 256
101	36 x 128
11x	reserved

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-86 on page 2-87 describes the FIFO depth options for various data width and memory blocks.

Interface

Figure 2-65 on page 2-99 shows a logic block diagram of the Accelerator FIFO module.

Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using SmartGen, the user only needs to specify the depth and width of the necessary FIFO blocks. SmartGen automatically configures these blocks to optimize performance.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO54PB1F5	E20	IO72PB2F6	J23	IO91NB2F8	N25
IO55NB1F5	E21	IO73NB2F6	H24	IO91PB2F8	N24
IO55PB1F5	D21	IO73PB2F6	H23	IO92NB2F8	N27
IO56NB1F5	H19	IO74NB2F7	L21	IO92PB2F8	N26
IO56PB1F5	G19	IO74PB2F7	K21	IO93NB2F8	P26
IO57NB1F5	D22	IO75NB2F7	G27	IO93PB2F8	P27
IO57PB1F5	C22	IO75PB2F7	F27	IO94NB2F8	N19
IO58NB1F5	B23	IO76NB2F7	K23	IO94PB2F8	N20
IO58PB1F5	A23	IO76PB2F7	K22	IO95NB2F8	P23
IO59NB1F5	D23	IO77NB2F7	H26	IO95PB2F8	P22
IO59PB1F5	C23	IO77PB2F7	H25	Bank 3	
IO60NB1F5	G21	IO78NB2F7	K25	IO96NB3F9	P25
IO60PB1F5	G20	IO78PB2F7	K24	IO96PB3F9	P24
IO61NB1F5	E23	IO79NB2F7	J26	IO97NB3F9	R26
IO61PB1F5	E22	IO79PB2F7	J25	IO97PB3F9	R27
IO62NB1F5	F22	IO80NB2F7	M20	IO98NB3F9	P21
IO62PB1F5	F21	IO80PB2F7	L20	IO98PB3F9	P20
IO63NB1F5	H20	IO81NB2F7	J27	IO99NB3F9	R24
IO63PB1F5	J19	IO81PB2F7	H27	IO99PB3F9	R25
Bank 2		IO82NB2F7	L23	IO100NB3F9	T26
IO64NB2F6	J21	IO82PB2F7	L22	IO100PB3F9	T27
IO64PB2F6	H21	IO83NB2F7	L25	IO101NB3F9	T24
IO65NB2F6	F24	IO83PB2F7	L24	IO101PB3F9	T25
IO65PB2F6	F23	IO84NB2F7	N21	IO102NB3F9	R20
IO66NB2F6	F26	IO84PB2F7	M21	IO102PB3F9	R21
IO66PB2F6	F25	IO85NB2F8	K27	IO103NB3F9	R23
IO67NB2F6	E26	IO85PB2F8	K26	IO103PB3F9	R22
IO67PB2F6	E25	IO86NB2F8	M23	IO104NB3F9	U26
IO68NB2F6	J22	IO86PB2F8	M22	IO104PB3F9	U27
IO68PB2F6	H22	IO87NB2F8	M25	IO105NB3F9	U24
IO69NB2F6	G24	IO87PB2F8	M24	IO105PB3F9	U25
IO69PB2F6	G23	IO88NB2F8	L27	IO106NB3F9	R19
IO70NB2F6	K20	IO88PB2F8	L26	IO106PB3F9	P19
IO70PB2F6	J20	IO89NB2F8	M27	IO107NB3F10	V26
IO71NB2F6	G26	IO89PB2F8	M26	IO107PB3F10	V27
IO71PB2F6	G25	IO90NB2F8	N23	IO108NB3F10	T23
IO72NB2F6	J24	IO90PB2F8	N22	IO108PB3F10	T22

FG484	
AX500 Function	Pin Number
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	Pin Number
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	Pin Number
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9

FG676	
AX500 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21

FG676	
AX500 Function	Pin Number
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG896	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8

FG896	
AX2000 Function	Pin Number
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15

FG896	
AX2000 Function	Pin Number
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20

FG896	
AX2000 Function	Pin Number
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
Bank 3	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26

FG896	
AX2000 Function	Pin Number
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27

FG896	
AX2000 Function	Pin Number
IO163NB3F15	AC26
IO163PB3F15	AB26
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23
IO170PB3F15	AA23
Bank 4	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23

FG896	
AX2000 Function	Pin Number
IO180PB4F16	AG24
IO181NB4F17	AK24
IO181PB4F17	AK25
IO182NB4F17	AD22
IO182PB4F17	AC22
IO183NB4F17	AF22
IO183PB4F17	AF23
IO184NB4F17	AE21
IO184PB4F17	AE22
IO185NB4F17	AJ23
IO185PB4F17	AJ24
IO187NB4F17	AH22
IO187PB4F17	AH23
IO188NB4F17	AD21
IO188PB4F17	AC21
IO189PB4F17	AK22
IO190NB4F17	AF20
IO190PB4F17	AF21
IO191NB4F17	AG21
IO191PB4F17	AG22
IO192NB4F17	AE19
IO192PB4F17	AE20
IO195NB4F18	AK21
IO195PB4F18	AJ21
IO196NB4F18	AD19
IO196PB4F18	AD20
IO197NB4F18	AJ20
IO197PB4F18	AK20
IO198NB4F18	AC19
IO198PB4F18	AC20
IO199NB4F18	AG19
IO199PB4F18	AG20
IO200NB4F18	AH19
IO200PB4F18	AH20
IO201NB4F18	AK19

FG896	
AX2000 Function	Pin Number
IO201PB4F18	AJ19
IO202NB4F18	AC18
IO202PB4F18	AB18
IO206NB4F19	AE18
IO206PB4F19	AD18
IO207NB4F19	AJ17
IO207PB4F19	AJ18
IO208NB4F19	AE17
IO208PB4F19	AD17
IO209NB4F19	AK17
IO210NB4F19	AC17
IO210PB4F19	AB17
IO211NB4F19	AJ16
IO211PB4F19	AK16
IO212NB4F19/CLKEN	AG18
IO212PB4F19/CLKEP	AH18
IO213NB4F19/CLKFN	AG16
IO213PB4F19/CLKFP	AG17
Bank 5	
IO214NB5F20/CLKGN	AG14
IO214PB5F20/CLKGP	AG15
IO215NB5F20/CLKHN	AG13
IO215PB5F20/CLKHP	AH13
IO216NB5F20	AB14
IO216PB5F20	AC15
IO217NB5F20	AK15
IO217PB5F20	AJ15
IO218NB5F20	AE14
IO218PB5F20	AD14
IO219NB5F20	AK14
IO219PB5F20	AJ14
IO222NB5F20	AB13
IO222PB5F20	AC14
IO223NB5F21	AJ12
IO223PB5F21	AJ13

FG896	
AX2000 Function	Pin Number
IO225NB5F21	AH11
IO225PB5F21	AH12
IO226NB5F21	AC13
IO226PB5F21	AD13
IO227NB5F21	AE12
IO227PB5F21	AE13
IO228NB5F21	AG11
IO228PB5F21	AG12
IO229NB5F21	AK11
IO229PB5F21	AK12
IO230NB5F21	AC12
IO230PB5F21	AD12
IO232NB5F21	AE11
IO232PB5F21	AF11
IO233NB5F21	AJ10
IO233PB5F21	AJ11
IO234NB5F21	AC11
IO234PB5F21	AD11
IO236NB5F22	AK9
IO236PB5F22	AK10
IO237NB5F22	AG9
IO237PB5F22	AG10
IO238NB5F22	AF9
IO238PB5F22	AF10
IO239NB5F22	AH8
IO239PB5F22	AH9
IO240NB5F22	AC10
IO240PB5F22	AD10
IO242NB5F22	AE9
IO242PB5F22	AE10
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IO244PB5F22	AK7
IO245NB5F23	AF8

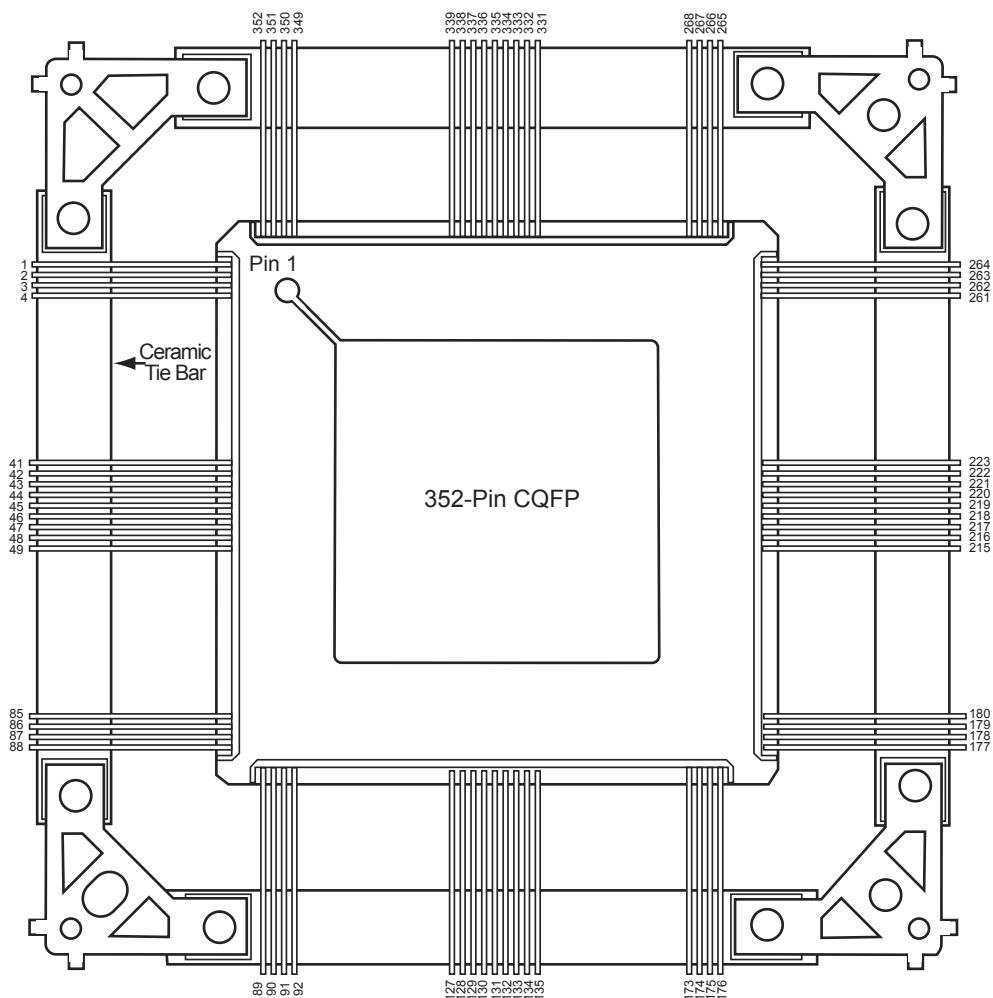
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AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO103PB2F9	M28	IO121NB2F11	T27	IO138NB3F12	Y29
IO104NB2F9	M34	IO121PB2F11	T26	IO138PB3F12	W29
IO104PB2F9	L34	IO122NB2F11	T30	IO139NB3F13	Y27
IO105NB2F9	P27	IO122PB2F11	T29	IO139PB3F13	W27
IO105PB2F9	N27	IO123NB2F11	U28	IO140NB3F13	AA33
IO106NB2F9	M32	IO123PB2F11	T28	IO140PB3F13	Y33
IO106PB2F9	M31	IO124NB2F11	T31	IO141NB3F13	Y25
IO107NB2F10	P25	IO124PB2F11	T32	IO141PB3F13	Y24
IO107PB2F10	P26	IO125NB2F11	U24	IO142NB3F13	AA31
IO108NB2F10	N33	IO125PB2F11	U25	IO142PB3F13	Y31
IO108PB2F10	M33	IO126NB2F11	U33	IO143NB3F13	AA28
IO109NB2F10	P29	IO126PB2F11	U34	IO143PB3F13	Y28
IO109PB2F10	N29	IO127NB2F11	U26	IO144NB3F13	AA34
IO110NB2F10	P30	IO127PB2F11	U27	IO144PB3F13	Y34
IO110PB2F10	N30	IO128NB2F11	U31	IO145NB3F13	AA26
IO111NB2F10	R24	IO128PB2F11	U32	IO145PB3F13	Y26
IO111PB2F10	R25	Bank 3		IO146NB3F13	AA29
IO112NB2F10	P31	IO129NB3F12	V29	IO146PB3F13	AA30
IO112PB2F10	N31	IO129PB3F12	U29	IO147NB3F13	AB30
IO113NB2F10	R28	IO130NB3F12	V31	IO147PB3F13	AB29
IO113PB2F10	P28	IO130PB3F12	V32	IO148NB3F13	AB32
IO114NB2F10	P32	IO131NB3F12	V24	IO148PB3F13	AA32
IO114PB2F10	N32	IO131PB3F12	V25	IO149NB3F13	AB27
IO115NB2F10	R30	IO132NB3F12	W28	IO149PB3F13	AA27
IO115PB2F10	R29	IO132PB3F12	V28	IO150NB3F14	AC31
IO116NB2F10	P34	IO133NB3F12	W26	IO150PB3F14	AB31
IO116PB2F10	P33	IO133PB3F12	V26	IO151NB3F14	AD33
IO117NB2F10	R27	IO134NB3F12	W33	IO151PB3F14	AC33
IO117PB2F10	R26	IO134PB3F12	V33	IO152NB3F14	AC28
IO118NB2F11	R34	IO135NB3F12	W25	IO152PB3F14	AB28
IO118PB2F11	R33	IO135PB3F12	W24	IO153NB3F14	AB25
IO119NB2F11	T24	IO136NB3F12	W31	IO153PB3F14	AA25
IO119PB2F11	T25	IO136PB3F12	W32	IO154NB3F14	AD32
IO120NB2F11	T33	IO137NB3F12	Y30	IO154PB3F14	AC32
IO120PB2F11	T34	IO137PB3F12	W30	IO155NB3F14	AD29

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
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VCOMPLE	86
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VPUMP	158

CQ352



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 18 (March 2012)	Table 2-1 • Absolute Maximum Ratings was updated to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419).	2-1
	Values for tristate leakage current IOZ, and I _{IH} and I _{IL} were added to Table 2-3 • Standby Current (SARs 35774, 32021).	2-2
	Figure 2-2 • VCCPLX and VCOMPLX Power Supply Connect was updated to correct the units for the resistance from "W" to Ω (SAR 36415).	2-9
	In the Introduction to the "User I/Os" section, the following sentence was added to clarify the slew rate setting (SAR 34943): The slew rate setting is effective for both rising and falling edges.	2-11
	Figure 2-3 • Use of an External Resistor for 5 V Tolerance was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942).	2-13
	EQ 3 for 5 V tolerance was corrected to change V _{diode} from 0.6 V to 0.7 V (SAR 36786).	2-13
	Additional information was added to the "Using the Weak Pull-Up and Pull-Down Circuits" section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945).	2-17
	The description for the C _{INCLK} parameter in Table 2-18 • Input Capacitance was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944).	2-21
	Table 2-19 • I/O Input Rise Time and Fall Time* is new (SAR 34942).	2-21
	The minimum V _{IL} for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-29 • DC Input and Output Levels and Table 2-33 • DC Input and Output Levels (SAR 34358).	2-38, 2-40
	Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the <i>Antifuse Macro Library Guide</i> was added to the "R-Cell" section (SAR 26413).	2-58
Revision 17 (September 2011)	The enable signal in Figure 2-32 • R-Cell Delays was corrected to show it is active low rather than active high (SAR 34946).	2-59
	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Axcelerator Family Device Status" table indicates the status for each device in the device family.	iii
	The "Features" section, "Programmable Interconnect Element" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865).	i, 1-1, 2-108