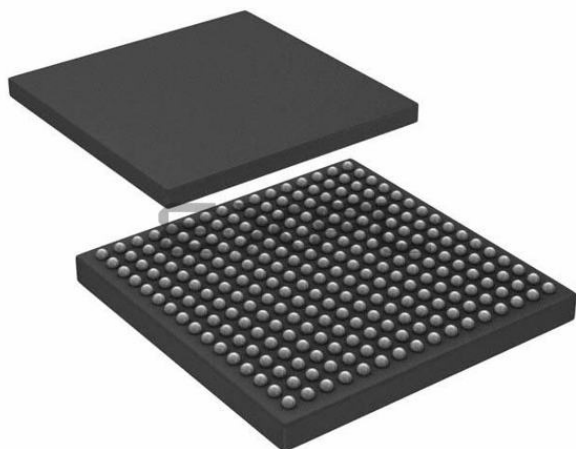




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2016
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	138
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax125-fg256

Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II, Microsemi's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-109).

Summary

Microsemi's Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an Axcelerator design yet still achieve high performance and efficient device utilization.

Related Documents

Application Notes

Simultaneous Switching Noise and Signal Integrity

http://www.microsemi.com/soc/documents/SSN_AN.pdf

Axcelerator Family PLL and Clock Management

http://www.microsemi.com/soc/documents/AX_PLL_AN.pdf

Implementation of Security in Actel Antifuse FPGAs

http://www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

User's Guides and Manuals

Antifuse Macro Library Guide

http://www.microsemi.com/soc/documents/libguide_UG.pdf

SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder

http://www.microsemi.com/soc/documents/genguide_ug.pdf

Silicon Sculptor II User's Guide

http://www.microsemi.com/soc/documents/silisculptII_sculpt3_ug.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs

http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

Understanding Actel Antifuse Device Security

http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

Miscellaneous

Libero IDE flow diagram

<http://www.microsemi.com/soc/products/tools/libero/flow.html>

2 – Detailed Specifications

Operating Conditions

Table 2-1 lists the absolute maximum ratings of Axcelerator devices. Stresses beyond the ratings may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommendations in Table 2-2.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCA	DC Core Supply Voltage	–0.3 to 1.7	V
VCCI	DC I/O Supply Voltage	–0.3 to 3.75	V
VREF	DC I/O Reference Voltage	–0.3 to 3.75	V
VI	Input Voltage	–0.5 to 4.1	V
VO	Output Voltage	–0.5 to 3.75	V
TSTG	Storage Temperature	–60 to +150	°C
VCCDA*	Supply Voltage for Differential I/Os	–0.3 to 3.75	V

Note: * Should be the maximum of all VCCI.

Table 2-2 • Recommended Operating Conditions

Parameter Range	Commercial	Industrial	Military	Units
Ambient Temperature (T_A) ¹	0 to +70	–40 to +85	–55 to +125	°C
1.5 V Core Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.5 V I/O Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.8 V I/O Supply Voltage	1.71 to 1.89	1.71 to 1.89	1.71 to 1.89	V
2.5 V I/O Supply Voltage	2.375 to 2.625	2.375 to 2.625	2.375 to 2.625	V
3.3 V I/O Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCDA Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VPUMP Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Notes:

1. Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.
2. $T_J \text{ max} = 125^\circ\text{C}$

Power-Up/Down Sequence

All Axcelerator I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. VCCDA should be powered up before (or coincidentally with) VCCA and VCCI to ensure the behavior of user I/Os at system start-up. Conversely, VCCDA should be powered down after (or coincidentally with) VCCA and VCCI. Note that VCCI and VCCA can be powered up in any sequence with respect to each other, provided the requirement with respect to VCCDA is satisfied.

Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Note that there are no tristated or bidirectional I/O buffers for differential standards.

Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users need to:

1. Instantiate an input buffer (with the required I/O standard)
2. Instantiate the DDR_REG macro (Figure 2-6)
3. Connect the output from the Input buffer to the input of the DDR macro

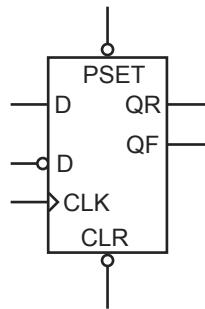


Figure 2-6 • DDR Register

Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required VCCI and VREF voltages for an I/O. The generic buffer macros require the LVTTTL standard with slow slew rate and 24 mA-drive strength. LVTTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (e.g. INBUF_LVDS) or a pair of differential outputs (e.g. OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (i.e. INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

1.5 V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-29 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.35 VCCI	0.65 VCCI	3.6	0.4	VCCI - 0.4	8 mA	-8 mA

AC Loadings

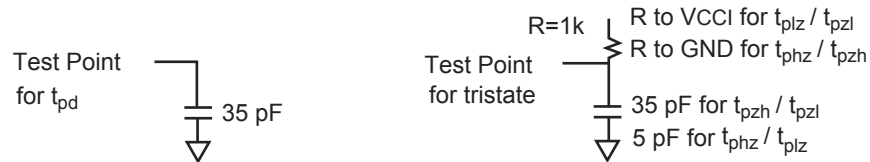


Table 2-30 • AC Test Loads

Table 2-31 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	1.5	0.5V _{CCI}	N/A	35

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-32 • 1.5V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.4 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS15 (JESD8-11) I/O Module Timing								
t _{DP}	Input Buffer		3.59		4.09		4.81	ns
t _{PY}	Output Buffer		6.05		6.89		8.10	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.31		3.34		3.34	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.56		4.58		4.59	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.37		7.25		8.52	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.94		7.90		9.29	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

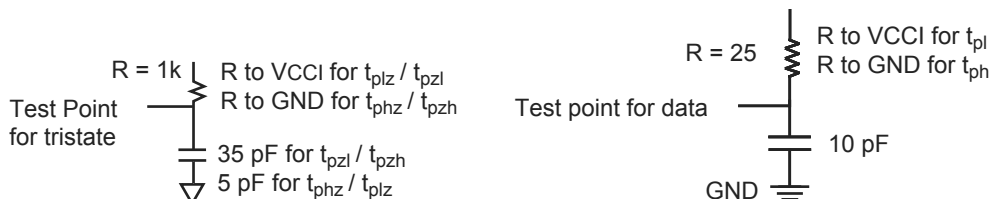


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

The ClockTileDist Cluster contains an HCLKMux (HM) module for each of the four HCLK trees and a CLKMux (CM) module for each of the CLK trees. The HCLK branches then propagate horizontally through the middle of the core tile to HCLKColDist (HD) modules in every SuperCluster column. The CLK branches propagate vertically through the center of the core tile to CLKRowDist (RD) modules in every SuperCluster row. Together, the HCLK and CLK branches provide for a low-skew global fanout within the core tile (Figure 2-40 and Figure 2-41).

Figure 2-40 • CTD, CD, and HD Module Layout

Figure 2-41 • HCLK and CLK Distribution within a Core Tile

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111". If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:
The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microsemi identity, part number, and version number in a specific JTAG format.
2. USERCODE:
The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.
3. Boundary-Scan Register (BSR):
Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.
4. Bypass Register (BYR):
This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

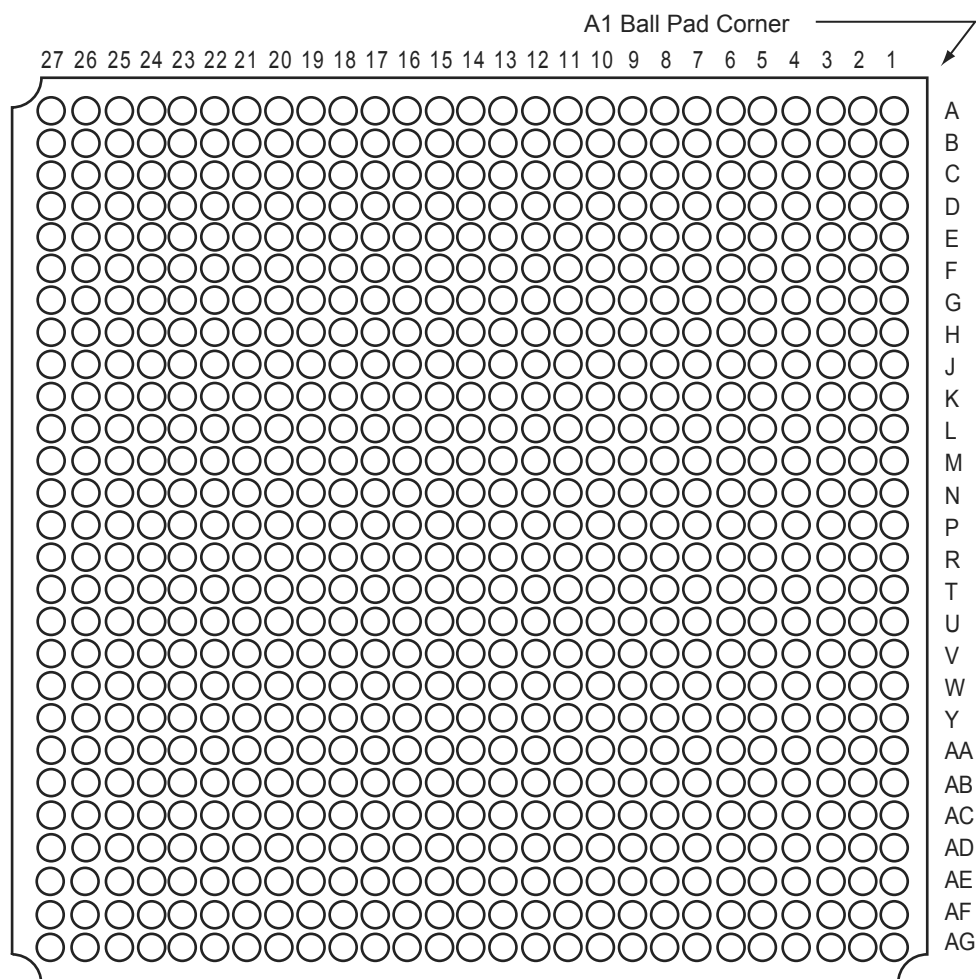
Special Fuses

Security

Microsemi antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden

3 – Package Pin Assignments

BG729



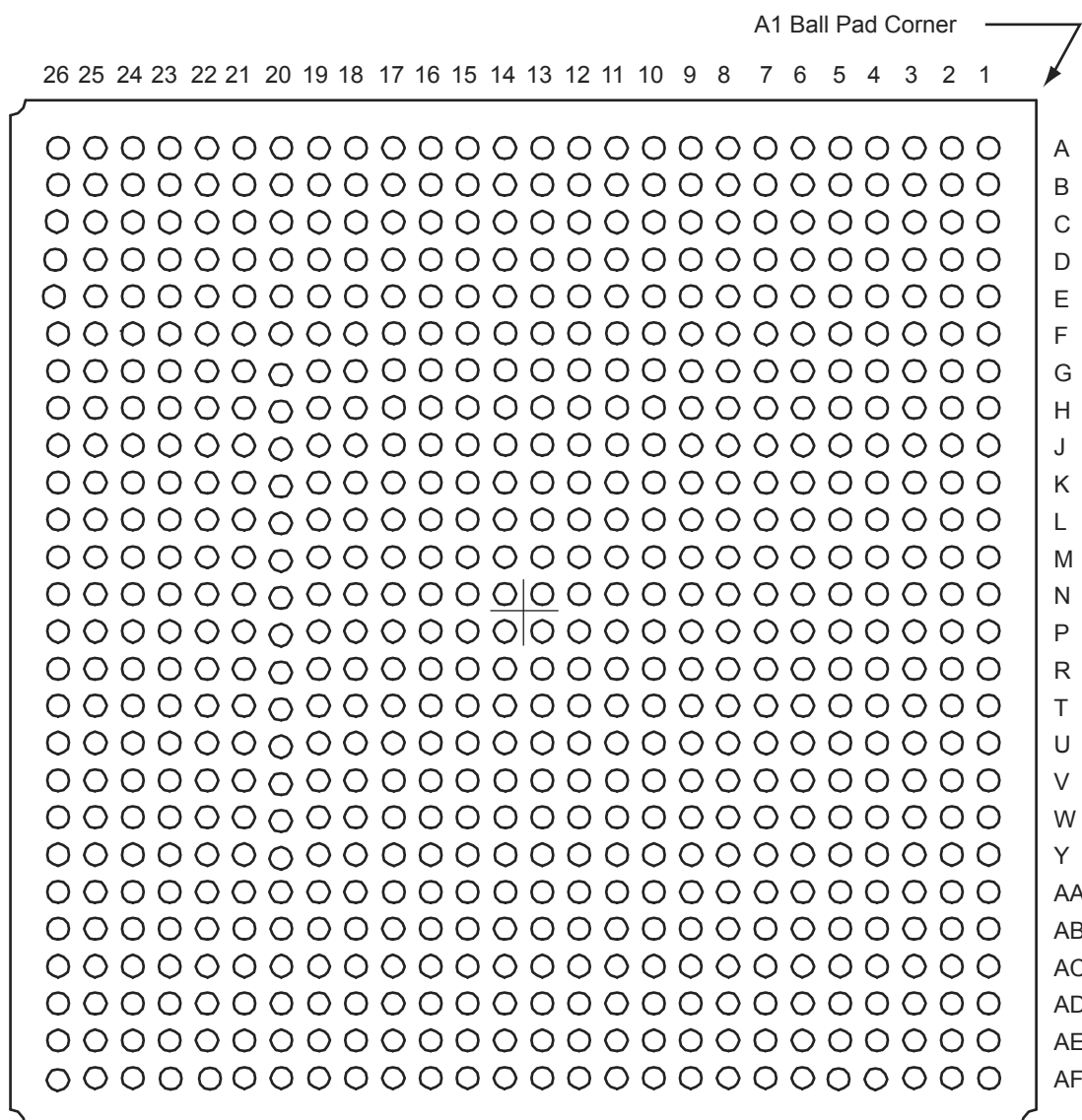
Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 0		IO20NB2F2	F15	IO41PB3F3	L14
IO01NB0F0	B4	IO20PB2F2	E15	Bank 4	
IO01PB0F0	B3	IO21NB2F2	C16	IO42NB4F4	N12
IO03NB0F0	A4	IO21PB2F2	B16	IO42PB4F4	N13
IO03PB0F0	A3	IO22NB2F2	H13	IO43NB4F4	T14
IO04NB0F0	B6	IO22PB2F2	G13	IO43PB4F4	R14
IO04PB0F0	B5	IO23NB2F2	E16	IO44PB4F4	T15
IO06NB0F0	A6	IO23PB2F2	D16	IO45NB4F4	R12
IO06PB0F0	A5	IO25NB2F2	H15	IO45PB4F4	R13
IO07NB0F0/HCLKAN	B8	IO25PB2F2	G15	IO46NB4F4	P11
IO07PB0F0/HCLKAP	B7	IO26NB2F2	H14	IO46PB4F4	P12
IO08NB0F0/HCLKBN	A9	IO26PB2F2	G14	IO47PB4F4	T11
IO08PB0F0/HCLKBP	A8	IO27NB2F2	G16	IO48NB4F4	T12
Bank 1		IO27PB2F2	F16	IO48PB4F4	T13
IO09NB1F1/HCLKCN	C10	IO28NB2F2	K15	IO49NB4F4/CLKEN	R9
IO09PB1F1/HCLKCP	C9	IO28PB2F2	K16	IO49PB4F4/CLKEP	R10
IO10NB1F1/HCLKDN	B11	IO29NB2F2	J16	IO50NB4F4/CLKFN	T8
IO10PB1F1/HCLKDP	B10	IO29PB2F2	H16	IO50PB4F4/CLKFP	T9
IO12NB1F1	A13	Bank 3		Bank 5	
IO12PB1F1	A12	IO30NB3F3	K13	IO51NB5F5/CLKGN	P7
IO13NB1F1	B13	IO30PB3F3	J13	IO51PB5F5/CLKGP	P8
IO13PB1F1	B12	IO31NB3F3	K14	IO52NB5F5/CLKHN	R6
IO14NB1F1	C12	IO31PB3F3	J14	IO52PB5F5/CLKHP	R7
IO14PB1F1	C11	IO33NB3F3	L15	IO54NB5F5	T5
IO15NB1F1	A15	IO33PB3F3	L16	IO54PB5F5	T6
IO15PB1F1	B14	IO35NB3F3	P16	IO55NB5F5	P5
IO16NB1F1	C15	IO35PB3F3	N16	IO55PB5F5	P6
IO16PB1F1	C14	IO36PB3F3	M16	IO56NB5F5	T3
IO17NB1F1	D13	IO37NB3F3	P15	IO56PB5F5	T4
IO17PB1F1	D12	IO37PB3F3	R16	IO57NB5F5	R3
Bank 2		IO39NB3F3	N15	IO57PB5F5	R4
IO18NB2F2	F13	IO39PB3F3	M15	IO58NB5F5	R1
IO18PB2F2	E13	IO40NB3F3	M13	IO58PB5F5	T2
IO19NB2F2	F14	IO40PB3F3	L13	IO59NB5F5	N4
IO19PB2F2	E14	IO41NB3F3	M14	IO59PB5F5	N5

FG324	
AX125 Function	Pin Number
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG676



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG676	
AX500 Function	Pin Number
IO102PB4F9	AB15
IO103NB4F9/CLKEN	AE16
IO103PB4F9/CLKEP	AF16
IO104NB4F9/CLKFN	AE14
IO104PB4F9/CLKFP	AE15
Bank 5	
IO105NB5F10/CLKGN	AE12
IO105PB5F10/CLKGP	AE13
IO106NB5F10/CLKHN	AE11
IO106PB5F10/CLKHP	AF11
IO107NB5F10	Y12
IO107PB5F10	AA13
IO108NB5F10	AC12
IO108PB5F10	AB12
IO109NB5F10	AC10
IO109PB5F10	AC11
IO110NB5F10	AF9
IO110PB5F10	AF10
IO111NB5F10	Y11
IO111PB5F10	AA12
IO112NB5F10	AE9
IO112PB5F10	AE10
IO113NB5F10	AC9
IO113PB5F10	AD9
IO114NB5F11	AF6
IO114PB5F11	AF7
IO115NB5F11	AA10
IO115PB5F11	AB10
IO116NB5F11	AE7
IO116PB5F11	AE8
IO117NB5F11	AD7
IO117PB5F11	AD8
IO118NB5F11	AC7
IO118PB5F11	AC8
IO119NB5F11	AD6

FG676	
AX500 Function	Pin Number
IO119PB5F11	AE6
IO120NB5F11	AE5
IO120PB5F11	AF5
IO121NB5F11	AF4
IO121PB5F11	AE4
IO122NB5F11	AC5
IO122PB5F11	AC6
IO123NB5F11	AD4
IO123PB5F11	AD5
IO124NB5F11	AB6
IO124PB5F11	AB7
IO125NB5F11	AE3
IO125PB5F11	AF3
Bank 6	
IO126NB6F12	AB3
IO126PB6F12	AC3
IO127NB6F12	AA2
IO127PB6F12	AB2
IO128NB6F12	AC2
IO128PB6F12	AD2
IO129NB6F12	Y1
IO129PB6F12	AA1
IO130NB6F12	Y3
IO130PB6F12	AA3
IO131NB6F12	U6
IO131PB6F12	V6
IO132NB6F12	W2
IO132PB6F12	Y2
IO133NB6F12	V4
IO133PB6F12	W4
IO134NB6F12	V3
IO134PB6F12	W3
IO135NB6F12	V1
IO135PB6F12	V2
IO136NB6F13	U4

FG676	
AX500 Function	Pin Number
IO136PB6F13	U5
IO137NB6F13	T6
IO137PB6F13	T7
IO138NB6F13	T5
IO138PB6F13	T4
IO139NB6F13	R6
IO139PB6F13	R7
IO140NB6F13	T3
IO140PB6F13	U3
IO141NB6F13	U1
IO141PB6F13	U2
IO142NB6F13	R2
IO142PB6F13	T2
IO143NB6F13	P3
IO143PB6F13	R3
IO144NB6F13	P5
IO144PB6F13	P4
IO145NB6F13	P6
IO145PB6F13	P7
IO146NB6F13	R1
IO146PB6F13	T1
Bank 7	
IO147NB7F14	N6
IO147PB7F14	N7
IO148NB7F14	N5
IO148PB7F14	N4
IO149NB7F14	N2
IO149PB7F14	N3
IO150NB7F14	L1
IO150PB7F14	M1
IO151NB7F14	M2
IO151PB7F14	M3
IO152NB7F14	M5
IO152PB7F14	M4
IO153NB7F14	M7

FG896	
AX1000 Function	Pin Number
IO51PB1F4	E21
IO52NB1F4	F22
IO52PB1F4	E22
IO53NB1F4	B25
IO53PB1F4	B24
IO54NB1F5	D24
IO54PB1F5	D23
IO55NB1F5	F23
IO55PB1F5	E23
IO56NB1F5	H21
IO56PB1F5	G21
IO57NB1F5	D25
IO57PB1F5	C25
IO58NB1F5	F24
IO58PB1F5	E24
IO59NB1F5	D26
IO59PB1F5	C26
IO60NB1F5	G23
IO60PB1F5	G22
IO61NB1F5	B27
IO61PB1F5	A27
IO62NB1F5	F25
IO62PB1F5	E25
IO63NB1F5	H23
IO63PB1F5	H22
Bank 2	
IO64NB2F6	K23
IO64PB2F6	J23
IO65NB2F6	J24
IO65PB2F6	H24
IO66NB2F6	H26
IO66PB2F6	H25
IO67NB2F6	G26
IO67PB2F6	G25
IO68NB2F6	K25

FG896	
AX1000 Function	Pin Number
IO68PB2F6	K24
IO69NB2F6	F27
IO69PB2F6	E27
IO70NB2F6	J26
IO70PB2F6	J25
IO71NB2F6	H27
IO71PB2F6	G27
IO72NB2F6	J28
IO72PB2F6	H28
IO73NB2F6	G28
IO73PB2F6	F28
IO74NB2F7	L23
IO74PB2F7	L24
IO75NB2F7	L26
IO75PB2F7	K26
IO76NB2F7	M25
IO76PB2F7	L25
IO77NB2F7	K27
IO77PB2F7	J27
IO78NB2F7	M27
IO78PB2F7	L27
IO79NB2F7	K30
IO79PB2F7	K29
IO80NB2F7	M23
IO80PB2F7	M24
IO81NB2F7	M28
IO81PB2F7	L28
IO82NB2F7	N26
IO82PB2F7	M26
IO83NB2F7	N25
IO83PB2F7	N24
IO84NB2F7	N22
IO84PB2F7	N23
IO85NB2F8	M29
IO85PB2F8	L29

FG896	
AX1000 Function	Pin Number
IO86NB2F8	N28
IO86PB2F8	N27
IO87NB2F8	P29
IO87PB2F8	P30
IO88NB2F8	P25
IO88PB2F8	P24
IO89NB2F8	P28
IO89PB2F8	P27
IO90NB2F8	P22
IO90PB2F8	P23
IO91NB2F8	R26
IO91PB2F8	P26
IO92NB2F8	R24
IO92PB2F8	R25
IO93NB2F8	R29
IO93PB2F8	R30
IO94NB2F8	R22
IO94PB2F8	R23
IO95NB2F8	T27
IO95PB2F8	R27
Bank 3	
IO96NB3F9	T29
IO96PB3F9	T30
IO97NB3F9	U29
IO97PB3F9	U30
IO98NB3F9	T22
IO98PB3F9	T23
IO99NB3F9	U26
IO99PB3F9	T26
IO100NB3F9	U24
IO100PB3F9	T24
IO101NB3F9	V28
IO101PB3F9	U28
IO102NB3F9	U23
IO102PB3F9	U22

FG896	
AX1000 Function	Pin Number
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3

FG896	
AX1000 Function	Pin Number
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG896	
AX2000 Function	Pin Number
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
Bank 3	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26

FG896	
AX2000 Function	Pin Number
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27

FG896	
AX2000 Function	Pin Number
IO163NB3F15	AC26
IO163PB3F15	AB26
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23
IO170PB3F15	AA23
Bank 4	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23

FG896	
AX2000 Function	Pin Number
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	Pin Number
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

CQ256		CQ256	
AX2000 Function	Pin Number	AX2000 Function	Pin Number
VCCA	4	VCCDA	224
VCCA	22	VCCDA	236
VCCA	42	VCCDA	237
VCCA	61	VCCDA	251
VCCA	63	VCCIB0	230
VCCA	84	VCCIB0	244
VCCA	108	VCCIB1	200
VCCA	127	VCCIB1	206
VCCA	131	VCCIB1	218
VCCA	150	VCCIB2	164
VCCA	170	VCCIB2	176
VCCA	189	VCCIB2	182
VCCA	191	VCCIB3	138
VCCA	212	VCCIB3	144
VCCA	238	VCCIB3	156
VCCDA	2	VCCIB4	102
VCCDA	32	VCCIB4	114
VCCDA	66	VCCIB4	120
VCCDA	67	VCCIB5	72
VCCDA	86	VCCIB5	78
VCCDA	87	VCCIB5	90
VCCDA	94	VCCIB6	36
VCCDA	95	VCCIB6	48
VCCDA	96	VCCIB6	54
VCCDA	106	VCCIB7	10
VCCDA	107	VCCIB7	16
VCCDA	126	VCCIB7	28
VCCDA	130	VPUMP	195
VCCDA	160		
VCCDA	194		
VCCDA	196		
VCCDA	214		
VCCDA	215		
VCCDA	222		
VCCDA	223		

CQ352	
AX250 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
VCCA	U17	VCCIB2	D23	VCCIB7	E4
VCCA	U9	VCCIB2	E22	VCCIB7	K9
VCCA	Y4	VCCIB2	K17	VCCIB7	L9
VCCDA	A12	VCCIB2	L17	VCCIB7	M10
VCCDA	AA13	VCCIB2	M16	VCCPLA	E12
VCCDA	AA15	VCCIB3	AA22	VCCPLB	J12
VCCDA	AA7	VCCIB3	AB23	VCCPLC	E14
VCCDA	AC11	VCCIB3	AC24	VCCPLD	H14
VCCDA	AD11	VCCIB3	AC25	VCCPLE	Y14
VCCDA	AE17	VCCIB3	P16	VCCPLF	U14
VCCDA	B15	VCCIB3	R17	VCCPLG	Y12
VCCDA	C15	VCCIB3	T17	VCCPLH	U12
VCCDA	C6	VCCIB4	AB21	VCOMPLA	F12
VCCDA	D13	VCCIB4	AC22	VCOMPLB	H12
VCCDA	E13	VCCIB4	AD23	VCOMPLC	F14
VCCDA	E19	VCCIB4	AE23	VCOMPLD	J14
VCCDA	G5	VCCIB4	T14	VCOMPLE	AA14
VCCDA	N21	VCCIB4	U15	VCOMPLF	V14
VCCDA	N5	VCCIB4	U16	VCOMPLG	AA12
VCCDA	W21	VCCIB5	AB5	VCOMPLH	V12
VCCIB0	A3	VCCIB5	AC4	VPUMP	E20
VCCIB0	B3	VCCIB5	AD3		
VCCIB0	C4	VCCIB5	AE3		
VCCIB0	D5	VCCIB5	T12		
VCCIB0	J10	VCCIB5	U10		
VCCIB0	J11	VCCIB5	U11		
VCCIB0	K12	VCCIB6	AA4		
VCCIB1	A23	VCCIB6	AB3		
VCCIB1	B23	VCCIB6	AC1		
VCCIB1	C22	VCCIB6	AC2		
VCCIB1	D21	VCCIB6	P10		
VCCIB1	J15	VCCIB6	R9		
VCCIB1	J16	VCCIB6	T9		
VCCIB1	K14	VCCIB7	C1		
VCCIB2	C24	VCCIB7	C2		
VCCIB2	C25	VCCIB7	D3		