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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2016
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	138
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax125-fgg256

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 4 (24 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		10.45		11.90		13.99	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		10.61		12.08		14.21	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		10.47		11.93		14.02	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.92		1.94		1.94	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.57		2.58		2.59	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

1.5 V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-29 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.35 VCCI	0.65 VCCI	3.6	0.4	VCCI - 0.4	8 mA	-8 mA

AC Loadings

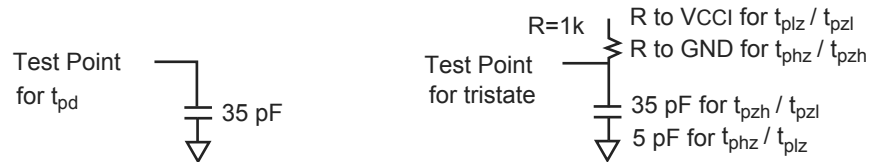


Table 2-30 • AC Test Loads

Table 2-31 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	1.5	0.5V _{CCI}	N/A	35

Note: * Measuring Point = VTRIP

Differential Standards

Physical Implementation

Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O Cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350 mV.

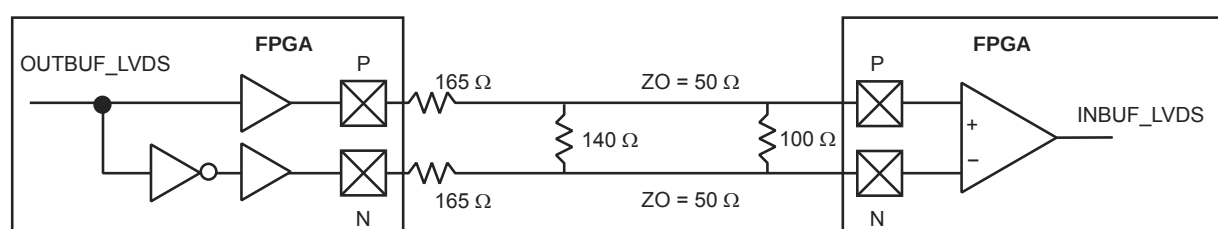


Figure 2-25 • LVDS Board-Level Implementation

The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2 V to 2.2 V for a differential input with 400 mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (note that the driver is not a current-mode driver). This driver provides a nominal constant current of 3.5 mA. When this current flows through a 100 Ω termination resistor on the receiver side, a voltage swing of 350 mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350 mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

Table 2-56 • DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI ¹	Supply Voltage	2.375	2.5	2.625	V
VOH	Output High Voltage	1.25	1.425	1.6	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM2	Input Common Mode Voltage	0.2	1.25	2.2	V

Notes:

1. ±5%
2. Differential input voltage = ±350 mV.

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

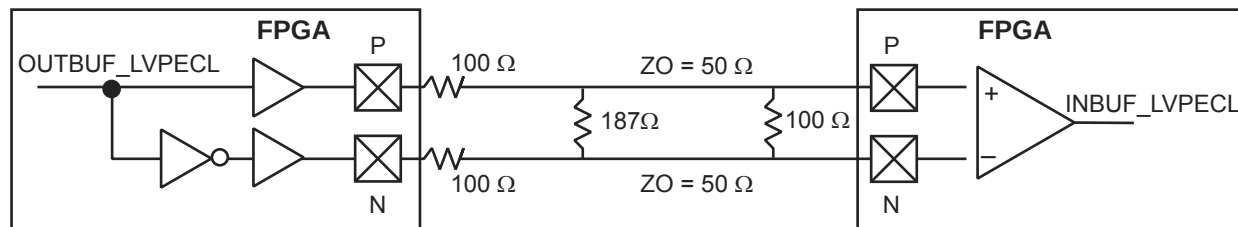


Figure 2-26 • LVPECL Board-Level Implementation

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS since the output voltage levels are different. Please note that the VOH levels are 200 mV below the standard LVPECL levels.

Table 2-59 • DC Input and Output Levels

DC Parameter	Min.		Typ.		Max.		Units
	Min.	Max.	Min.	Max.	Min.	Max.	
VCCI	3		3.3		3.6		V
VOH	1.8	2.11	1.92	2.28	2.13	2.41	V
VOL	0.96	1.27	1.06	1.43	1.3	1.57	V
VIH	1.49	2.72	1.49	2.72	1.49	2.72	V
VIL	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3		0.3		0.3		V

Table 2-60 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.6 – 0.3	1.6 + 0.3	1.6

Note: * Measuring Point = VTRIP

Timing Models and Waveforms

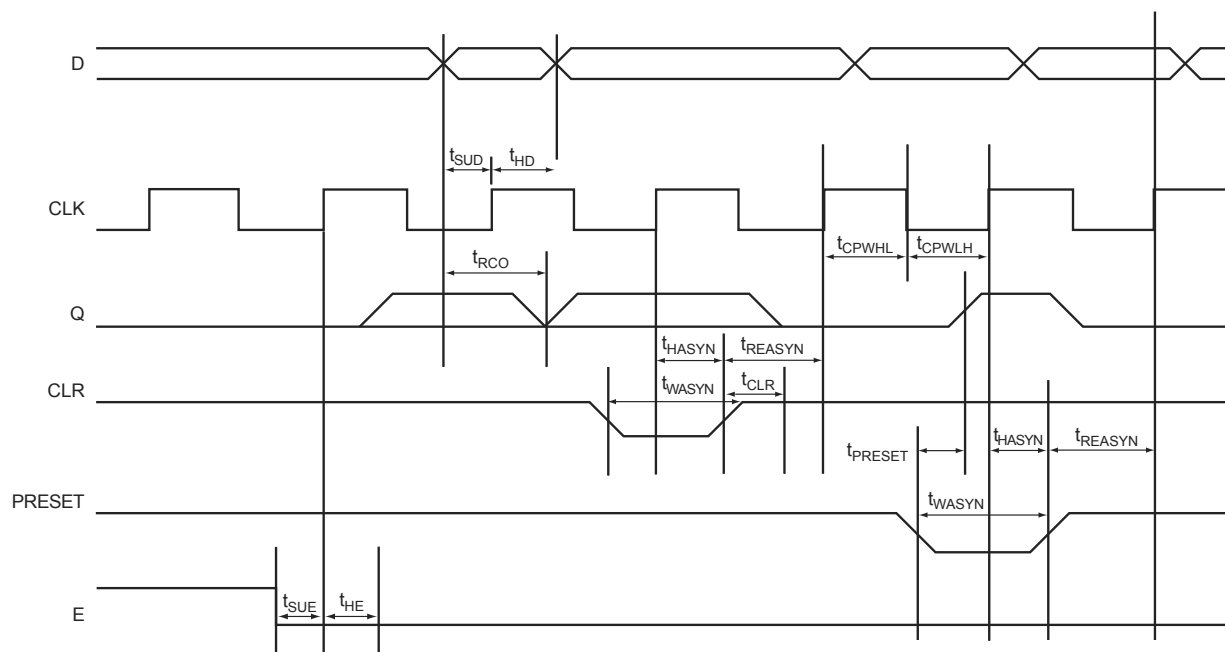


Figure 2-32 • R-Cell Delays

Timing Characteristics

Table 2-63 • R-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
R-Cell Propagation Delays								
t _{RCO}	Sequential Clock-to-Q		0.67		0.77		0.90	ns
t _{CLR}	Asynchronous Clear-to-Q		0.67		0.77		0.90	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.36		0.36		0.36	ns
t _{SUD}	Flip-Flop Data Input Set-Up		0.34		0.34		0.34	ns
t _{SUE}	Flip-Flop Enable Input Set-Up		0.00		0.00		0.00	ns
t _{HD}	Flip-Flop Data Input Hold		0.67		0.77		0.90	ns
t _{HE}	Flip-Flop Enable Input Hold		0.67		0.77		0.90	ns
t _{WASYN}	Asynchronous Pulse Width	0.48		0.48		0.48		ns
t _{REASYN}	Asynchronous Recovery Time		0.23		0.27		0.31	ns
t _{HASYN}	Asynchronous Removal Time		0.36		0.36		0.36	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.36		0.36		0.36		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.36		0.36		0.36		ns

Table 2-67 • AX500 Predicted Routing Delays
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $T_J = 70^\circ\text{C}$

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-68 • AX1000 Predicted Routing Delays
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $T_J = 70^\circ\text{C}$

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.45	0.51	0.60	ns
t_{RD2}	Routing delay for FO2	0.53	0.60	0.71	ns
t_{RD3}	Routing delay for FO3	0.56	0.63	0.74	ns
t_{RD4}	Routing delay for FO4	0.63	0.71	0.84	ns
t_{RD5}	Routing delay for FO5	0.73	0.82	0.97	ns
t_{RD6}	Routing delay for FO6	0.99	1.13	1.32	ns
t_{RD7}	Routing delay for FO7	1.02	1.15	1.36	ns
t_{RD8}	Routing delay for FO8	1.48	1.68	1.97	ns
t_{RD16}	Routing delay for FO16	2.57	2.91	3.42	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Table 2-72 • AX500 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.35		2.68		3.15	ns
t _{HCKH}	Input High to Low		2.44		2.79		3.27	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-73 • AX1000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-74 • AX2000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-77 • AX500 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		2.31		2.63		3.09	ns
t _{RCKH}	Input High to Low		2.44		2.78		3.27	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-78 • AX1000 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-79 • AX2000 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-38).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-39).

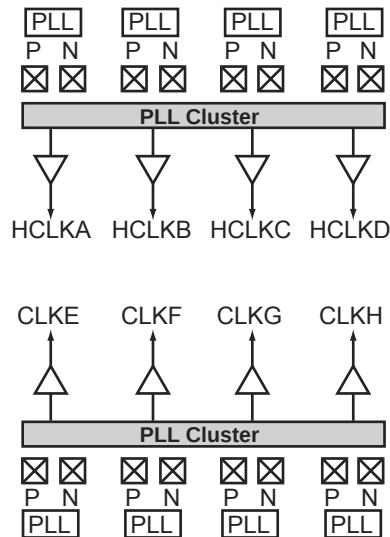


Figure 2-38 • PLL Group

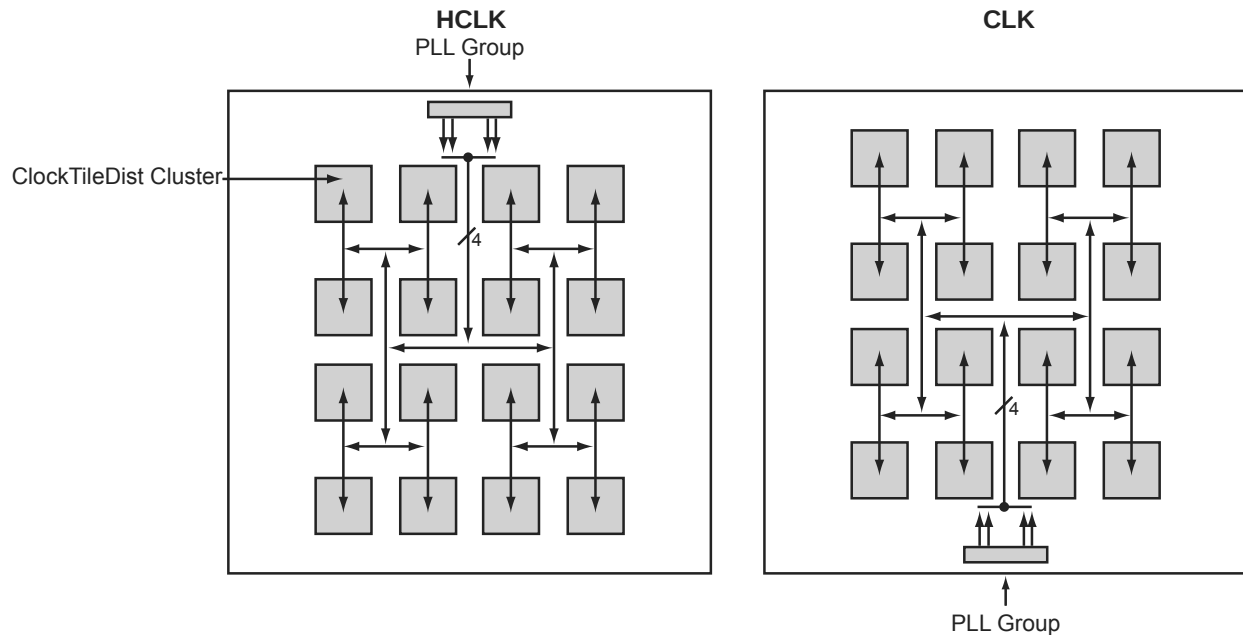


Figure 2-39 • Example of HCLK and CLK Distributions on the AX2000

PLL Configurations

The following rules apply to the different PLL inputs and outputs:

Reference Clock

The RefCLK can be driven by (Figure 2-50):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. CLK1 output of an adjacent PLL
3. [H]CLKxP (single-ended or voltage-referenced)
4. [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Feedback Clock

The feedback clock can be driven by (Figure 2-51 on page 2-78):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
3. An internal signal from the PLL block

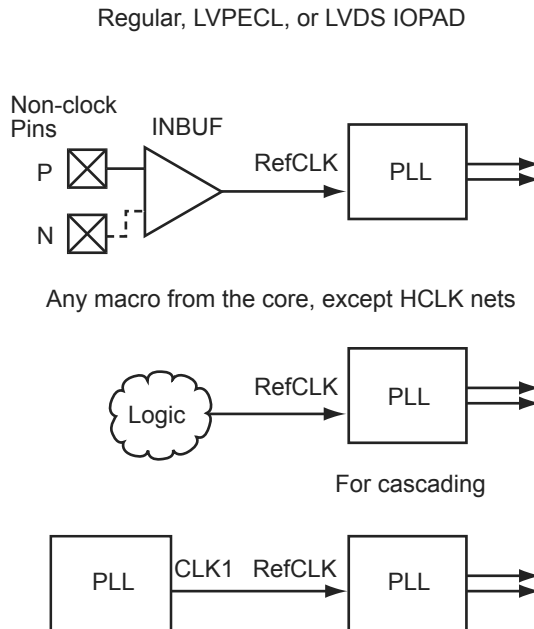


Figure 2-50 • Reference Clock Connections

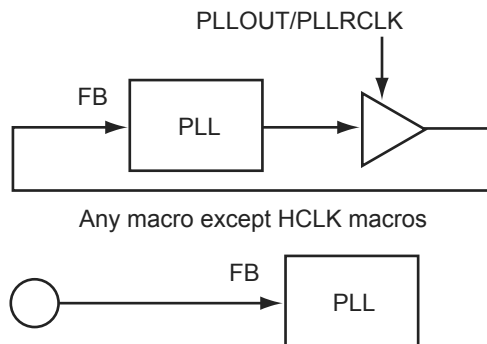


Figure 2-51 • Feedback Clock Connections

Timing Characteristics

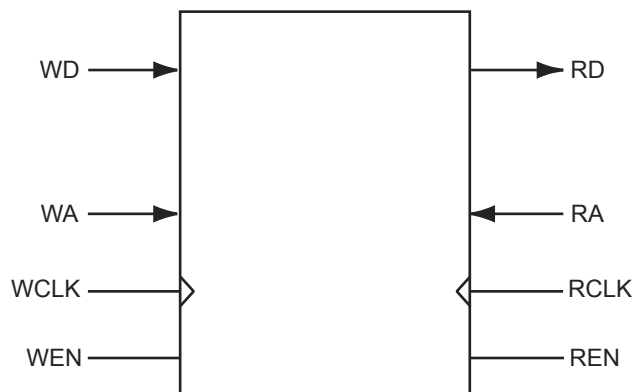


Figure 2-58 • SRAM Model

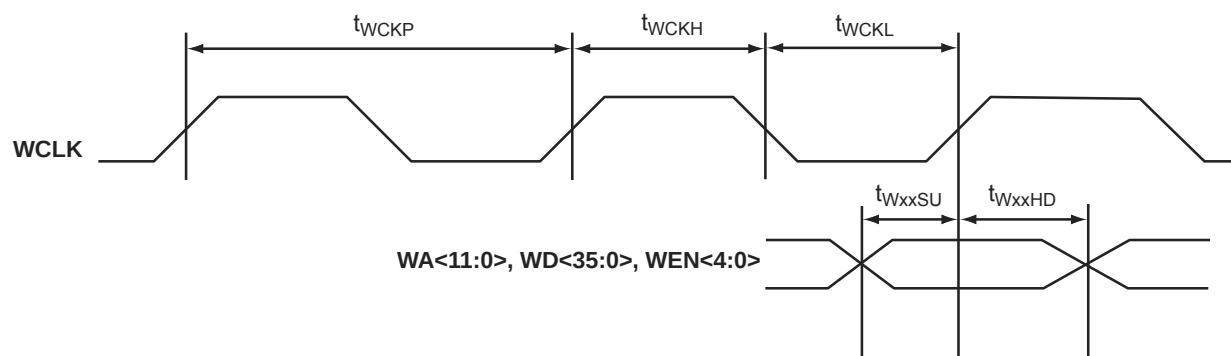


Figure 2-59 • RAM Write Timing Waveforms

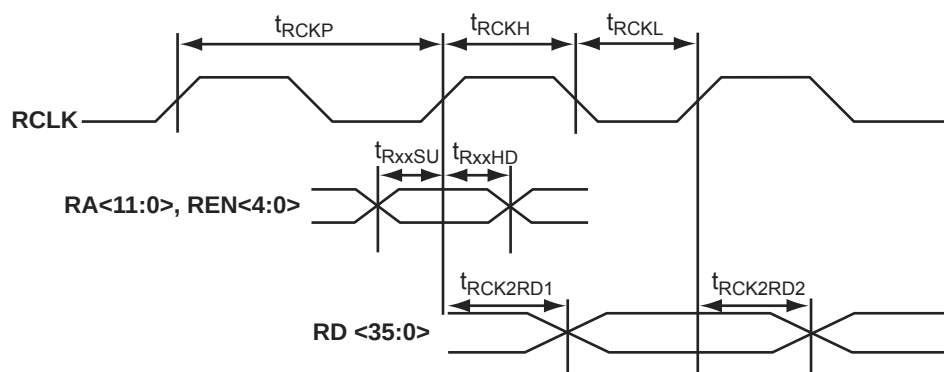


Figure 2-60 • RAM Read Timing Waveforms

Timing Characteristics

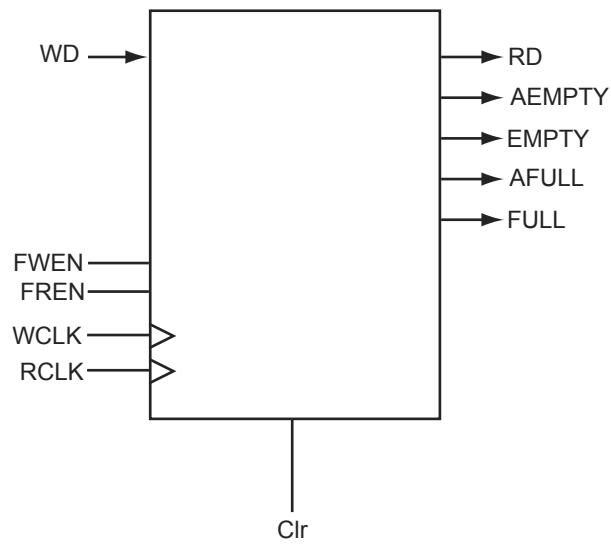


Figure 2-66 • FIFO Model

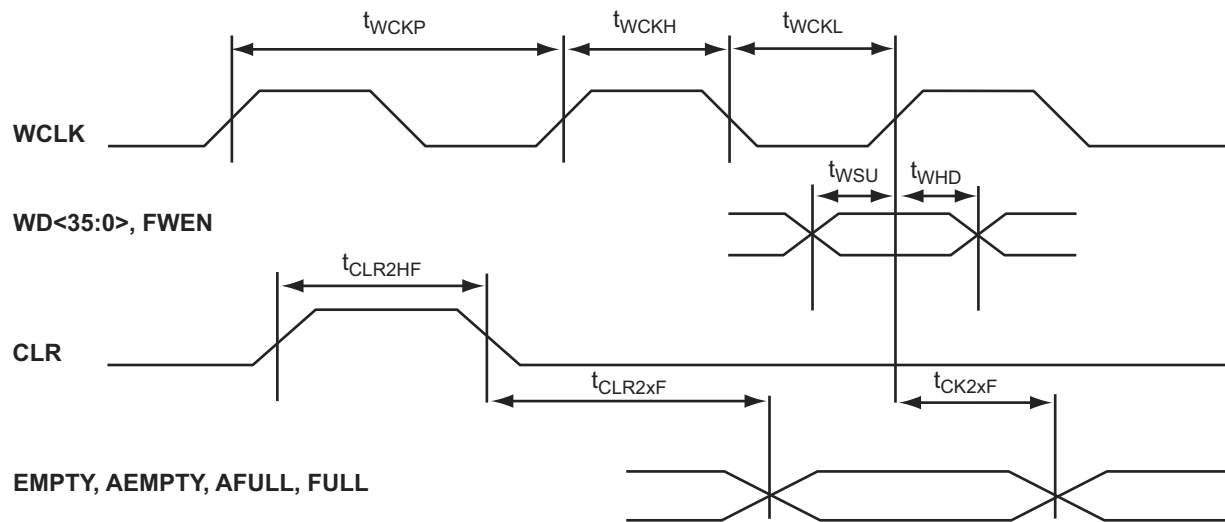


Figure 2-67 • FIFO Write Timing

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 0		IO20NB2F2	F15	IO41PB3F3	L14
IO01NB0F0	B4	IO20PB2F2	E15	Bank 4	
IO01PB0F0	B3	IO21NB2F2	C16	IO42NB4F4	N12
IO03NB0F0	A4	IO21PB2F2	B16	IO42PB4F4	N13
IO03PB0F0	A3	IO22NB2F2	H13	IO43NB4F4	T14
IO04NB0F0	B6	IO22PB2F2	G13	IO43PB4F4	R14
IO04PB0F0	B5	IO23NB2F2	E16	IO44PB4F4	T15
IO06NB0F0	A6	IO23PB2F2	D16	IO45NB4F4	R12
IO06PB0F0	A5	IO25NB2F2	H15	IO45PB4F4	R13
IO07NB0F0/HCLKAN	B8	IO25PB2F2	G15	IO46NB4F4	P11
IO07PB0F0/HCLKAP	B7	IO26NB2F2	H14	IO46PB4F4	P12
IO08NB0F0/HCLKBN	A9	IO26PB2F2	G14	IO47PB4F4	T11
IO08PB0F0/HCLKBP	A8	IO27NB2F2	G16	IO48NB4F4	T12
Bank 1		IO27PB2F2	F16	IO48PB4F4	T13
IO09NB1F1/HCLKCN	C10	IO28NB2F2	K15	IO49NB4F4/CLKEN	R9
IO09PB1F1/HCLKCP	C9	IO28PB2F2	K16	IO49PB4F4/CLKEP	R10
IO10NB1F1/HCLKDN	B11	IO29NB2F2	J16	IO50NB4F4/CLKFN	T8
IO10PB1F1/HCLKDP	B10	IO29PB2F2	H16	IO50PB4F4/CLKFP	T9
IO12NB1F1	A13	Bank 3		Bank 5	
IO12PB1F1	A12	IO30NB3F3	K13	IO51NB5F5/CLKGN	P7
IO13NB1F1	B13	IO30PB3F3	J13	IO51PB5F5/CLKGP	P8
IO13PB1F1	B12	IO31NB3F3	K14	IO52NB5F5/CLKHN	R6
IO14NB1F1	C12	IO31PB3F3	J14	IO52PB5F5/CLKHP	R7
IO14PB1F1	C11	IO33NB3F3	L15	IO54NB5F5	T5
IO15NB1F1	A15	IO33PB3F3	L16	IO54PB5F5	T6
IO15PB1F1	B14	IO35NB3F3	P16	IO55NB5F5	P5
IO16NB1F1	C15	IO35PB3F3	N16	IO55PB5F5	P6
IO16PB1F1	C14	IO36PB3F3	M16	IO56NB5F5	T3
IO17NB1F1	D13	IO37NB3F3	P15	IO56PB5F5	T4
IO17PB1F1	D12	IO37PB3F3	R16	IO57NB5F5	R3
Bank 2		IO39NB3F3	N15	IO57PB5F5	R4
IO18NB2F2	F13	IO39PB3F3	M15	IO58NB5F5	R1
IO18PB2F2	E13	IO40NB3F3	M13	IO58PB5F5	T2
IO19NB2F2	F14	IO40PB3F3	L13	IO59NB5F5	N4
IO19PB2F2	E14	IO41NB3F3	M14	IO59PB5F5	N5

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
Bank 0		IO17NB1F1	B14	IO34PB2F2	D22
IO00NB0F0	D7	IO17PB1F1	B13	IO35NB2F2	J18
IO00PB0F0	D6	IO18NB1F1	A14	IO35PB2F2	H18
IO01NB0F0	E7	IO18PB1F1	A13	IO36NB2F2	G21
IO01PB0F0	E6	IO19NB1F1	A16	IO36PB2F2	F21
IO02NB0F0	C5	IO19PB1F1	A15	IO37NB2F2	K19
IO02PB0F0	C4	IO20NB1F1	B16	IO37PB2F2	J19
IO03NB0F0	C7	IO20PB1F1	B15	IO38NB2F2	J20
IO03PB0F0	C6	IO21NB1F1	C17	IO38PB2F2	H20
IO04NB0F0	E9	IO21PB1F1	C16	IO39NB2F2	L16
IO04PB0F0	E8	IO22NB1F1	F15	IO39PB2F2	K16
IO05NB0F0	D9	IO22PB1F1	F14	IO40NB2F2	J21
IO05PB0F0	D8	IO23NB1F1	D16	IO40PB2F2	H21
IO06NB0F0	B7	IO23PB1F1	D15	IO41NB2F2	L17
IO06PB0F0	B6	IO24NB1F1	E16	IO41PB2F2	K17
IO07NB0F0	C9	IO24PB1F1	E15	IO42NB2F2	J22
IO07PB0F0	C8	IO25NB1F1	F18	IO42PB2F2	H22
IO08NB0F0	A7	IO25PB1F1	F17	IO43NB2F2	L18
IO08PB0F0	A6	IO26NB1F1	D18	IO43PB2F2	K18
IO09NB0F0	B9	IO26PB1F1	E17	IO44NB2F2	L20
IO09PB0F0	B8	IO27NB1F1	G16	IO44PB2F2	K20
IO10NB0F0	A9	IO27PB1F1	G15	Bank 3	
IO10PB0F0	A8	Bank 2		IO45NB3F3	M19
IO11NB0F0	B10	IO28NB2F2	F19	IO45PB3F3	L19
IO11PB0F0	A10	IO28PB2F2	E19	IO46NB3F3	M21
IO12NB0F0/HCLKAN	E11	IO29NB2F2	J16	IO46PB3F3	L21
IO12PB0F0/HCLKAP	E10	IO29PB2F2	H16	IO47NB3F3	N17
IO13NB0F0/HCLKBN	D12	IO30NB2F2	E20	IO47PB3F3	M17
IO13PB0F0/HCLKBP	D11	IO30PB2F2	D20	IO48NB3F3	N18
Bank 1		IO31NB2F2	J17	IO48PB3F3	N19
IO14NB1F1/HCLKCN	F13	IO31PB2F2	H17	IO49NB3F3	N16
IO14PB1F1/HCLKCP	F12	IO32NB2F2	G20	IO49PB3F3	M16
IO15NB1F1/HCLKDN	E14	IO32PB2F2	F20	IO50NB3F3	N20
IO15PB1F1/HCLKDP	E13	IO33NB2F2	H19	IO50PB3F3	M20
IO16NB1F1	C13	IO33PB2F2	G19	IO51NB3F3	P21
IO16PB1F1	C12	IO34NB2F2	E22	IO51PB3F3	N21

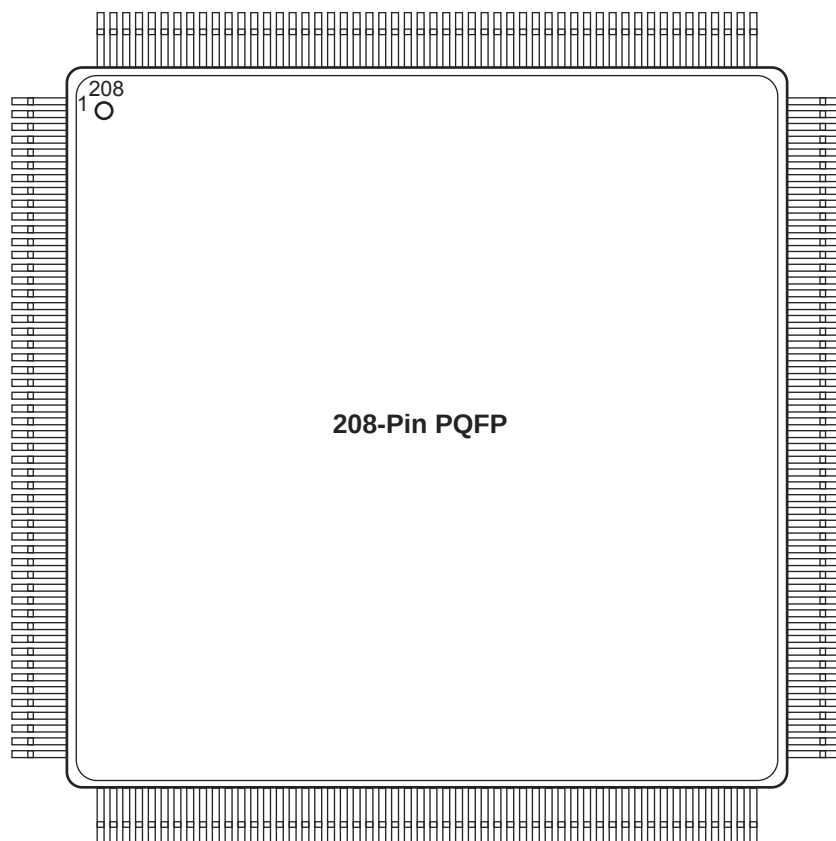
FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9

FG676	
AX500 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21

FG676	
AX500 Function	Pin Number
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	T12	GND	W19	NC	AJ4
GND	T13	GND	Y11	NC	AK14
GND	T14	GND	Y20	NC	AK15
GND	T15	GND/LP	E4	NC	AK16
GND	T16	NC	A16	NC	AK17
GND	T17	NC	A26	NC	AK22
GND	T18	NC	A4	NC	AK4
GND	T19	NC	A6	NC	AK5
GND	T28	NC	AA30	NC	B16
GND	T3	NC	AB1	NC	B18
GND	U12	NC	AB30	NC	B21
GND	U13	NC	AC2	NC	B23
GND	U14	NC	AC29	NC	B26
GND	U15	NC	AD1	NC	B4
GND	U16	NC	AD2	NC	B6
GND	U17	NC	AD30	NC	B8
GND	U18	NC	AE1	NC	C27
GND	U19	NC	AE15	NC	D1
GND	V1	NC	AE16	NC	D2
GND	V12	NC	AE2	NC	D29
GND	V13	NC	AE30	NC	D30
GND	V14	NC	AF1	NC	E1
GND	V15	NC	AF2	NC	E2
GND	V16	NC	AF29	NC	E29
GND	V17	NC	AF30	NC	E30
GND	V18	NC	AG1	NC	F15
GND	V19	NC	AG2	NC	F16
GND	V30	NC	AG29	NC	F29
GND	W12	NC	AG30	NC	F30
GND	W13	NC	AH27	NC	G1
GND	W14	NC	AH4	NC	G29
GND	W15	NC	AJ14	NC	G30
GND	W16	NC	AJ15	NC	H29
GND	W17	NC	AJ16	NC	J1
GND	W18	NC	AJ27	NC	J30

PQ208



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

PQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
V _{CCDA}	1
V _{CCDA}	26
V _{CCDA}	53
V _{CCDA}	63
V _{CCDA}	78
V _{CCDA}	95
V _{CCDA}	105
V _{CCDA}	130
V _{CCDA}	157
V _{CCDA}	167
V _{CCDA}	182
V _{CCDA}	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX500 Function	Pin Number
GND	94
GND	99
GND	113
GND	119
GND	125
GND	143
GND	136
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX500 Function	Pin Number
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	200
VCCIB0	193
VCCIB1	172
VCCIB1	163
VCCIB2	149
VCCIB2	135
VCCIB3	124
VCCIB3	112
VCCIB4	98
VCCIB4	89
VCCIB5	68
VCCIB5	58
VCCIB6	45
VCCIB6	31
VCCIB7	20
VCCIB7	8
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

CQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

CQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158