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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	136
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	256-BFCQFP with Tie Bar
Supplier Device Package	256-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-1cq256m

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

2 – Detailed Specifications

Operating Conditions

Table 2-1 lists the absolute maximum ratings of Axcelerator devices. Stresses beyond the ratings may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommendations in Table 2-2.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCCA	DC Core Supply Voltage	–0.3 to 1.7	V
VCCI	DC I/O Supply Voltage	–0.3 to 3.75	V
VREF	DC I/O Reference Voltage	–0.3 to 3.75	V
VI	Input Voltage	–0.5 to 4.1	V
VO	Output Voltage	–0.5 to 3.75	V
TSTG	Storage Temperature	–60 to +150	°C
VCCDA*	Supply Voltage for Differential I/Os	–0.3 to 3.75	V

*Note: * Should be the maximum of all VCCI.*

Table 2-2 • **Recommended Operating Conditions**

Parameter Range	Commercial	Industrial	Military	Units
Ambient Temperature (T_A)[1]	0 to +70	–40 to +85	–55 to +125	°C
1.5 V Core Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.5 V I/O Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.8 V I/O Supply Voltage	1.71 to 1.89	1.71 to 1.89	1.71 to 1.89	V
2.5 V I/O Supply Voltage	2.375 to 2.625	2.375 to 2.625	2.375 to 2.625	V
3.3 V I/O Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCDA Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VPUMP Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*
2. *T_J max = 125°C*

Power-Up/Down Sequence

All Axcelerator I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. VCCDA should be powered up before (or coincidentally with) VCCA and VCCI to ensure the behavior of user I/Os at system start-up. Conversely, VCCDA should be powered down after (or coincidentally with) VCCA and VCCI. Note that VCCI and VCCA can be powered up in any sequence with respect to each other, provided the requirement with respect to VCCDA is satisfied.

Calculating Power Dissipation

Table 2-3 • **Standby Current**

Device	Temperature	ICCA	ICCDA	ICCBANK		ICCPLL	ICCCP[1]		IIH, IIL, IOZ[2]	Units
		Standby Current (Core)	Standby Current, Differential I/O	Standby Current per I/O Bank		Standby Current per PLL	Standby Current, Charge Pump			
				2.5 V VCCI	3.3 V VCCI		Active	Bypassed Mode		
AX125	Typical at 25°C	1.5	1.5	0.2	0.3	0.2	0.3	0.01	±0.01	mA
	70°C	15	6	0.5	0.75	1	0.4	0.01	±0.01	mA
	85°C	25	6	0.6	0.8	1	0.4	0.2	±0.01	mA
	125°C	50	8	1	1.5	2	0.4	0.5	±0.01	mA
AX250	Typical at 25°C	1.5	1.4	0.25	0.4	0.2	0.3	0.01	±0.01	mA
	70°C	30	7	0.8	0.9	1	0.4	0.01	±0.01	mA
	85°C	40	7	0.8	1	1	0.4	0.2	±0.01	mA
	125°C	70	9	1.3	1.8	2	0.4	0.5	±0.01	mA
AX500	Typical at 25°C	5	1.4	0.4	0.75	0.2	0.3	0.01	±0.01	mA
	70°C	60	7	1	1.5	1	0.4	0.01	±0.01	mA
	85°C	80	7	1	1.9	1	0.4	0.2	±0.01	mA
	125°C	180	9	1.75	2.5	1.5	0.4	0.5	±0.01	mA
AX1000	Typical at 25°C	7.5	1.5	0.5	1.25	0.2	0.3	0.01	±0.01	mA
	70°C	80	8	1.5	3	1	0.4	0.01	±0.01	mA
	85°C	120	8	1.5	3.4	1	0.4	0.2	±0.01	mA
	125°C	200	10	3	4	1.5	0.4	0.5	±0.01	mA
AX2000	Typical at 25°C	20	1.6	0.7	1.5	0.2	0.3	0.01	±0.01	mA
	70°C	160	10	2	7	1	0.4	0.01	±0.01	mA
	85°C	200	10	3	8	1	0.4	0.2	±0.01	mA
	125°C	500	15	4	10	1.5	0.4	0.5	±0.01	mA

Notes:

1. *ICCCP Active is the ICCDA or the Internal Charge Pump current. ICCCP Bypassed mode is the External Charge Pump current IIH (VPUMP pin).*
2. *IIH, IIL, or IOZ values are measured with inputs at the same level as VCCI for IIH and GND for IIL and IOZ.*

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		3.30		3.76		4.42	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.74		4.26		5.00	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.06		3.49		4.10	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.29		2.30		2.31	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-40* • 3.3 V GTL+ I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V GTL+I/O Module Timing								
t_{DP}	Input Buffer		1.71		1.95		2.29	ns
t_{PY}	Output Buffer		1.13		1.29		1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Buffer Module

Introduction

An additional resource inside each SuperCluster is the Buffer (B) module (Figure 1-4 on page 1-3). When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the AX architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium-to-high-fanout nets.

Timing Models and Waveforms

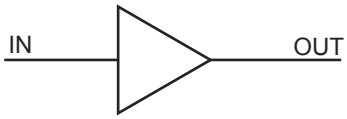


Figure 2-33 • **Buffer Module Timing Model**

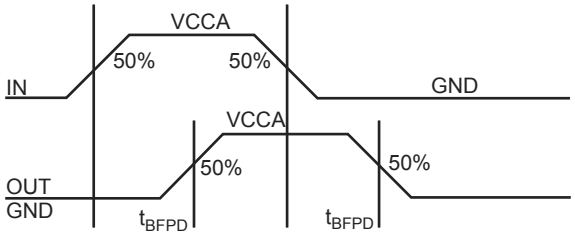


Figure 2-34 • **Buffer Module Waveform**

Timing Characteristics

Table 2-64 • **Buffer Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Buffer Module Propagation Delays								
t_{BFPD}	Any input to output Y		0.12		0.14		0.16	ns

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-37 on page 2-62). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 2-37). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

Figure 2-36 • **FastConnect Routing**

Figure 2-37 • **Horizontal and Vertical Tracks**

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t_{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t_{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t_{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t_{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t_{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t_{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t_{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t_{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t_{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

PLLRCLK and PLLHCLK

PLLRCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 2-44).

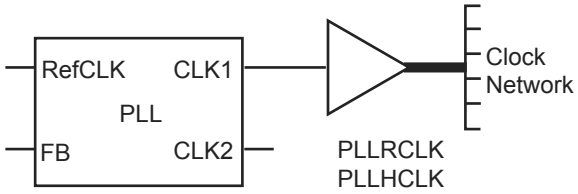


Figure 2-44 • **PLLRCLK and PLLHCLK**

Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc. (Figure 2-45).

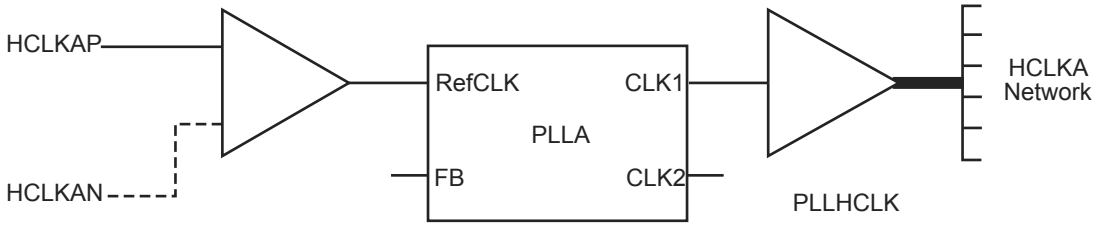


Figure 2-45 • **Example of HCLKA Driven from a PLL with External Clock Source**

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 2-46).

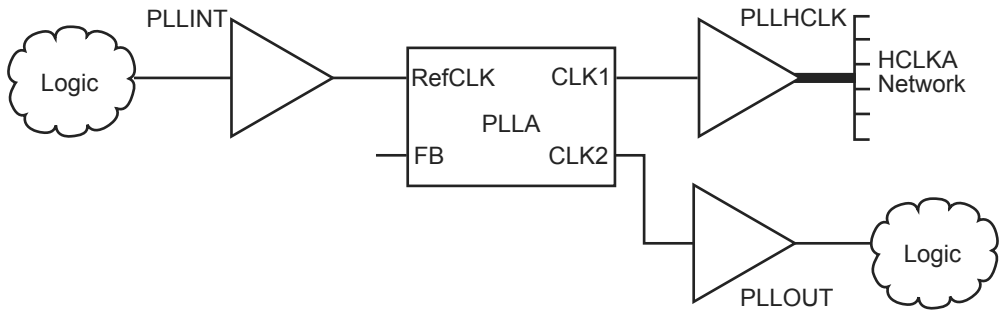


Figure 2-46 • **Example of PLLINT and PLLOUT Usage**

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

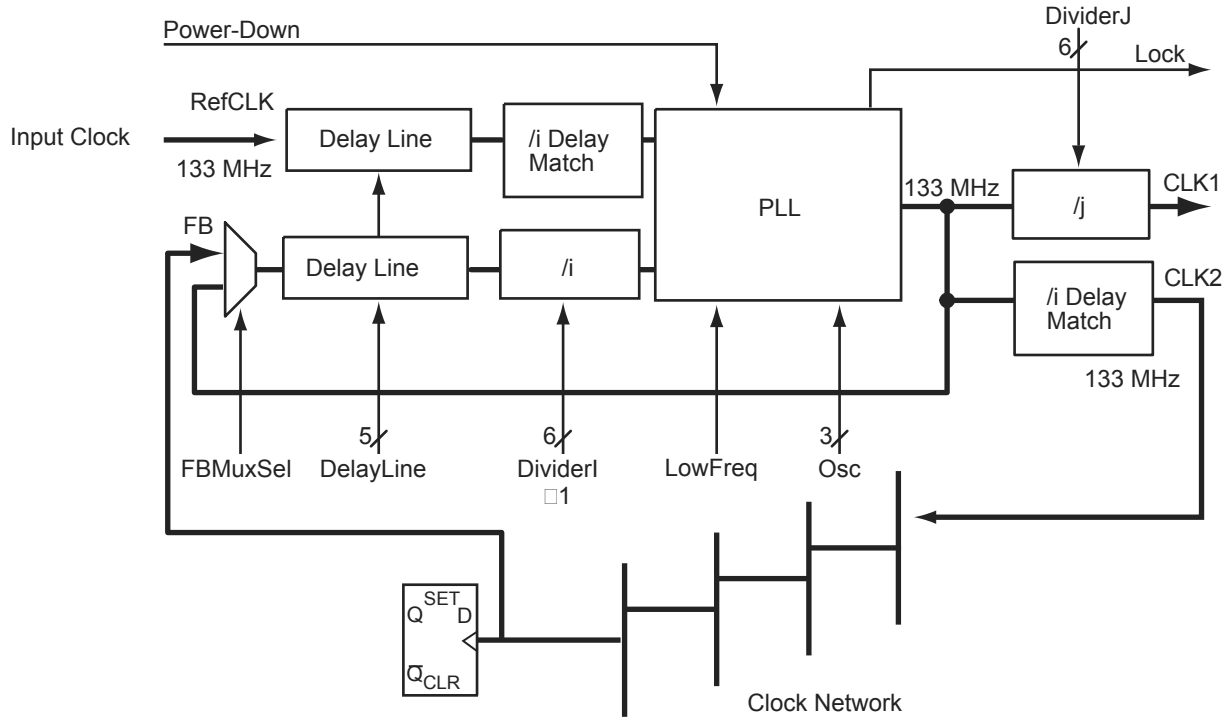


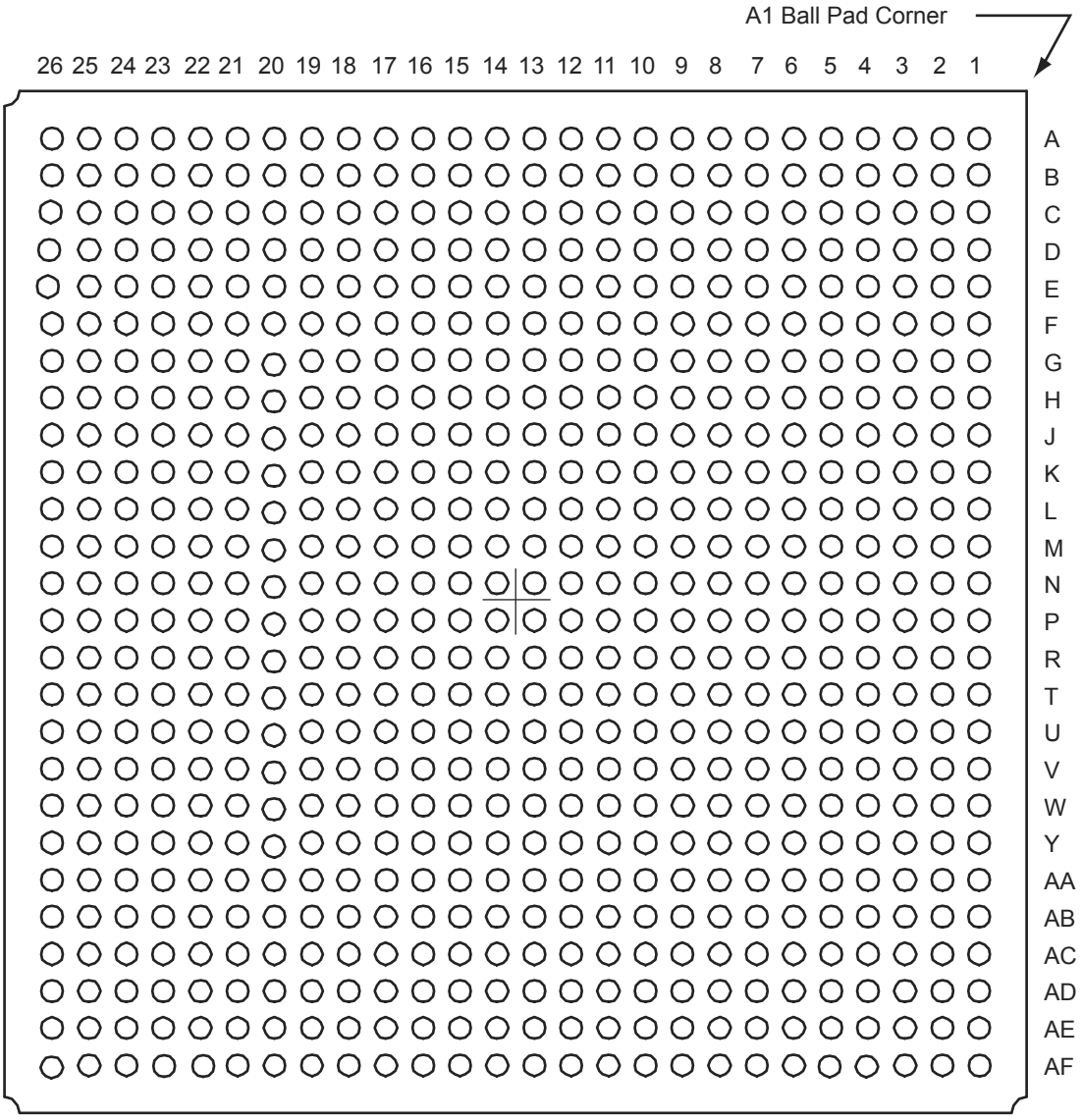
Figure 2-56 • **Using the PLL for Clock Deskewing**

***Table 2-93* • Sixteen RAM Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	13.40		13.40		13.40		ns
t_{WCKP}	WCLK Minimum Period	14.15		14.15		14.15		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		18.13		20.65		24.27	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		18.13		20.65		24.27	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		12.83		14.62		17.18	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	14.41		14.41		14.41		ns
t_{RCKP}	RCLK Minimum Period	15.14		15.14		15.14		ns

Note: Timing data for these sixteen cascaded RAM blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

FG676



Note

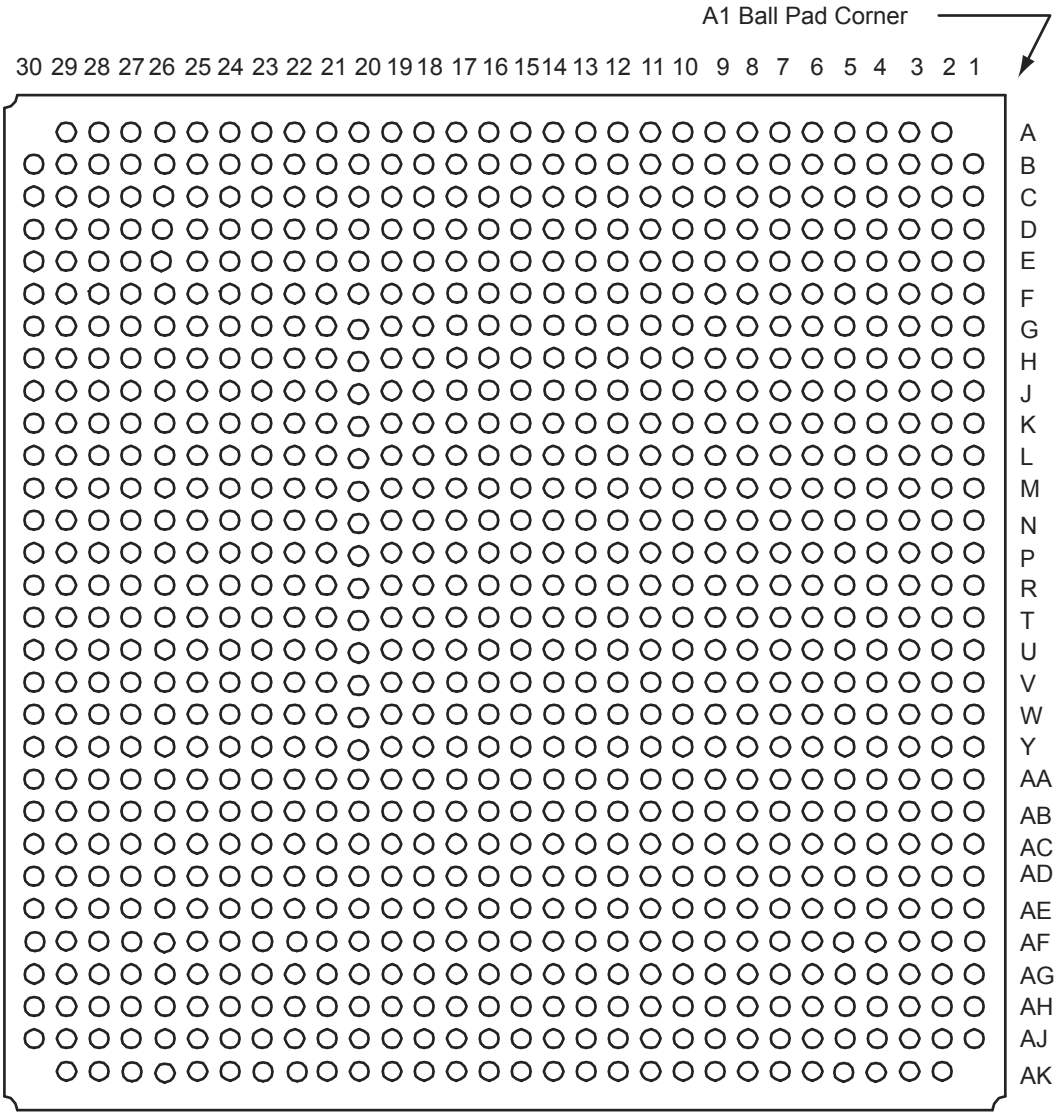
For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG676	
AX1000 Function	**Pin Number**
Bank 0	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10

FG676	
AX1000 Function	**Pin Number**
IO21PB0F1	C10
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
Bank 1	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20

FG676	
AX1000 Function	**Pin Number**
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20
IO52PB1F4	C20
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
Bank 2	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24

FG896



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG896	
AX2000 Function	Pin Number
IO65PB1F6	H20
IO66NB1F6	B23
IO66PB1F6	B21
IO67NB1F6	H21
IO67PB1F6	G21
IO68NB1F6	D22
IO68PB1F6	C22
IO69NB1F6	A25
IO69PB1F6	A24
IO70NB1F6	F22
IO70PB1F6	E22
IO71NB1F6	F21
IO71PB1F6	E21
IO73NB1F6	C24
IO73PB1F6	C23
IO74NB1F6	D24
IO74PB1F6	D23
IO75NB1F6	H23
IO75PB1F6	H22
IO76NB1F7	B25
IO76PB1F7	B24
IO78NB1F7	B26
IO78PB1F7	A26
IO79NB1F7	F23
IO79PB1F7	E23
IO80NB1F7	D25
IO80PB1F7	C25
IO81NB1F7	G23
IO81PB1F7	G22
IO82NB1F7	B27
IO82PB1F7	A27
IO83NB1F7	F24
IO83PB1F7	E24
IO84NB1F7	D26
IO84PB1F7	C26

FG896	
AX2000 Function	Pin Number
IO85NB1F7	F25
IO85PB1F7	E25
Bank 2	
IO86NB2F8	G26
IO86PB2F8	G25
IO87NB2F8	K23
IO87PB2F8	J23
IO88NB2F8	J24
IO88PB2F8	H24
IO89NB2F8	E29
IO89PB2F8	D29
IO90NB2F8	F27
IO90PB2F8	E27
IO91NB2F8	H26
IO91PB2F8	H25
IO92NB2F8	G28
IO92PB2F8	F28
IO93NB2F8	J26
IO93PB2F8	J25
IO94NB2F8	H27
IO94PB2F8	G27
IO95NB2F8	H29
IO95PB2F8	G29
IO96NB2F9	G30
IO96PB2F9	F30
IO97NB2F9	K25
IO97PB2F9	K24
IO98NB2F9	J28
IO98PB2F9	H28
IO99NB2F9	L23
IO99PB2F9	L24
IO100NB2F9	K27
IO100PB2F9	J27
IO101PB2F9	J30
IO102NB2F9	E30

FG896	
AX2000 Function	Pin Number
IO102PB2F9	D30
IO103NB2F9	L26
IO103PB2F9	K26
IO104NB2F9	F29
IO105NB2F9	M25
IO105PB2F9	L25
IO106NB2F9	K30
IO106PB2F9	K29
IO107NB2F10	M23
IO107PB2F10	M24
IO109NB2F10	M27
IO109PB2F10	L27
IO110NB2F10	M28
IO110PB2F10	L28
IO111NB2F10	N22
IO111PB2F10	N23
IO112NB2F10	M29
IO112PB2F10	L29
IO113NB2F10	N26
IO113PB2F10	M26
IO114NB2F10	M30
IO114PB2F10	L30
IO115NB2F10	N28
IO115PB2F10	N27
IO117NB2F10	N25
IO117PB2F10	N24
IO118NB2F11	N29
IO119NB2F11	P22
IO119PB2F11	P23
IO121NB2F11	P25
IO121PB2F11	P24
IO122NB2F11	P28
IO122PB2F11	P27
IO123NB2F11	R26
IO123PB2F11	P26

FG1152	
AX2000 Function	Pin Number
IO51PB1F4	J20
IO52NB1F4	B20
IO52PB1F4	A20
IO53NB1F4	F20
IO53PB1F4	E20
IO54NB1F5	B21
IO54PB1F5	A21
IO55NB1F5	K21
IO55PB1F5	J21
IO56NB1F5	D21
IO56PB1F5	C21
IO57NB1F5	G22
IO57PB1F5	G21
IO58NB1F5	E22
IO58PB1F5	E21
IO59NB1F5	D22
IO59PB1F5	C22
IO60NB1F5	B23
IO60PB1F5	A23
IO61NB1F5	H22
IO61PB1F5	H21
IO62NB1F5	C24
IO62PB1F5	C23
IO63NB1F5	F23
IO63PB1F5	F22
IO64NB1F6	B24
IO64PB1F6	A24
IO65NB1F6	J22
IO65PB1F6	K22
IO66NB1F6	B25
IO66PB1F6	A25
IO67NB1F6	K23
IO67PB1F6	J23
IO68NB1F6	F24
IO68PB1F6	E24

FG1152	
AX2000 Function	Pin Number
IO69NB1F6	C27
IO69PB1F6	C26
IO70NB1F6	H24
IO70PB1F6	G24
IO71NB1F6	H23
IO71PB1F6	G23
IO72NB1F6	B28
IO72PB1F6	A28
IO73NB1F6	E26
IO73PB1F6	E25
IO74NB1F6	F26
IO74PB1F6	F25
IO75NB1F6	K25
IO75PB1F6	K24
IO76NB1F7	D27
IO76PB1F7	D26
IO77NB1F7	B29
IO77PB1F7	A29
IO78NB1F7	D28
IO78PB1F7	C28
IO79NB1F7	H25
IO79PB1F7	G25
IO80NB1F7	F27
IO80PB1F7	E27
IO81NB1F7	J25
IO81PB1F7	J24
IO82NB1F7	D29
IO82PB1F7	C29
IO83NB1F7	H26
IO83PB1F7	G26
IO84NB1F7	F28
IO84PB1F7	E28
IO85NB1F7	H27
IO85PB1F7	G27
Bank 2	

FG1152	
AX2000 Function	Pin Number
IO86NB2F8	J28
IO86PB2F8	J27
IO87NB2F8	M25
IO87PB2F8	L25
IO88NB2F8	L26
IO88PB2F8	K26
IO89NB2F8	G31
IO89PB2F8	F31
IO90NB2F8	H29
IO90PB2F8	G29
IO91NB2F8	K28
IO91PB2F8	K27
IO92NB2F8	J30
IO92PB2F8	H30
IO93NB2F8	L28
IO93PB2F8	L27
IO94NB2F8	K29
IO94PB2F8	J29
IO95NB2F8	K31
IO95PB2F8	J31
IO96NB2F9	J32
IO96PB2F9	H32
IO97NB2F9	M27
IO97PB2F9	M26
IO98NB2F9	L30
IO98PB2F9	K30
IO99NB2F9	N25
IO99PB2F9	N26
IO100NB2F9	M29
IO100PB2F9	L29
IO101NB2F9	L33
IO101PB2F9	L32
IO102NB2F9	K34
IO102PB2F9	K33
IO103NB2F9	N28

FG1152	
AX2000 Function	**Pin Number**
IO311NB7F29	N3
IO311PB7F29	P3
IO312NB7F29	P7
IO312PB7F29	R7
IO313NB7F29	P6
IO313PB7F29	R6
IO314NB7F29	M2
IO314PB7F29	N2
IO315NB7F29	N4
IO315PB7F29	P4
IO316NB7F29	R9
IO316PB7F29	R8
IO317NB7F29	N5
IO317PB7F29	P5
IO318NB7F29	R10
IO318PB7F29	R11
IO319NB7F29	L2
IO319PB7F29	L1
IO320NB7F29	N8
IO320PB7F29	P8
IO321NB7F30	M6
IO321PB7F30	N6
IO322NB7F30	P10
IO322PB7F30	P9
IO323NB7F30	L3
IO323PB7F30	M3
IO324NB7F30	M7
IO324PB7F30	N7
IO325NB7F30	K2
IO325PB7F30	K1
IO326NB7F30	G2
IO326PB7F30	H2
IO327NB7F30	L6
IO327PB7F30	L5
IO328NB7F30	N10

FG1152	
AX2000 Function	**Pin Number**
IO328PB7F30	N9
IO329NB7F30	J4
IO329PB7F30	K4
IO330NB7F30	J5
IO330PB7F30	K5
IO331NB7F30	M10
IO331PB7F30	M9
IO332NB7F31	L8
IO332PB7F31	M8
IO333NB7F31	F2
IO333PB7F31	F1
IO334NB7F31	J6
IO334PB7F31	K6
IO335NB7F31	H4
IO335PB7F31	H3
IO336NB7F31	K7
IO336PB7F31	L7
IO337NB7F31	G4
IO337PB7F31	G3
IO338NB7F31	K9
IO338PB7F31	L9
IO339NB7F31	H6
IO339PB7F31	H5
IO340NB7F31	H7
IO340PB7F31	J7
IO341NB7F31	J8
IO341PB7F31	K8
Dedicated I/O	
GND	A13
GND	A2
GND	A22
GND	A27
GND	A3
GND	A31
GND	A32

FG1152	
AX2000 Function	**Pin Number**
GND	A33
GND	A4
GND	A8
GND	AA14
GND	AA15
GND	AA16
GND	AA17
GND	AA18
GND	AA19
GND	AA20
GND	AA21
GND	AB1
GND	AB13
GND	AB22
GND	AB34
GND	AC12
GND	AC23
GND	AC30
GND	AC5
GND	AD11
GND	AD24
GND	AD31
GND	AD4
GND	AE3
GND	AE32
GND	AF2
GND	AF33
GND	AG1
GND	AG27
GND	AG34
GND	AG8
GND	AH28
GND	AH7
GND	AJ29
GND	AJ6

CQ352	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282

CQ352	
AX2000 Function	Pin Number
IO71NB1F6	277
IO71PB1F6	278
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224

CQ352	
AX2000 Function	Pin Number
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15

CG624	
AX1000 Function	Pin Number
IO131NB4F12	V19
IO131PB4F12	W19
IO133NB4F12	Y18
IO133PB4F12	Y19
IO135NB4F12	W18
IO135PB4F12	V18
IO137NB4F12	Y17
IO137PB4F12	AA17
IO138NB4F12	AB19
IO138PB4F12	AB18
IO139NB4F13	AA19
IO139PB4F13	U18
IO140NB4F13	AC20
IO140PB4F13	AC21
IO141NB4F13	AD17
IO141PB4F13	AD18
IO142NB4F13	AD21
IO142PB4F13	AD22
IO143NB4F13	AB17
IO143PB4F13	AC17
IO144PB4F13	AE22
IO145NB4F13	AE15
IO145PB4F13	AE16
IO146NB4F13	AD19
IO146PB4F13	AD20
IO147NB4F13	AD15
IO147PB4F13	AD16
IO148PB4F13	AE21
IO149NB4F13	AD14
IO149PB4F13	AC14
IO150NB4F13	AE19
IO150PB4F13	AE20
IO151NB4F13	V17
IO151PB4F13	W17
IO152NB4F14	AB16
IO152PB4F14	W16

CG624	
AX1000 Function	Pin Number
IO153NB4F14	Y15
IO153PB4F14	Y16
IO155NB4F14	V15
IO155PB4F14	V16
IO156NB4F14	AB14
IO156PB4F14	AB15
IO157NB4F14	AE14
IO157PB4F14	AC18
IO158NB4F14	AC15
IO158PB4F14	AC19
IO159NB4F14/CLKEN	W14
IO159PB4F14/CLKEP	W15
IO160NB4F14/CLKFN	AC13
IO160PB4F14/CLKFP	AD13
Bank 5	
IO161NB5F15/CLKGN	W13
IO161PB5F15/CLKGP	Y13
IO162NB5F15/CLKHN	AC12
IO162PB5F15/CLKHP	AD12
IO163NB5F15	V9
IO163PB5F15	V10
IO164NB5F15	V11
IO164PB5F15	T13
IO165NB5F15	U13
IO165PB5F15	V13
IO167NB5F15	W11
IO167PB5F15	W12
IO168NB5F15	AB6
IO168PB5F15	AA6
IO169NB5F15	V8
IO169PB5F15	V7
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	AB8
IO172PB5F16	AC8
IO173NB5F16	AA11

CG624	
AX1000 Function	Pin Number
IO173PB5F16	Y11
IO174NB5F16	AB10
IO174PB5F16	AB11
IO175NB5F16	AC9
IO175PB5F16	AE9
IO177NB5F16	AA8
IO177PB5F16	Y8
IO178NB5F16	Y6
IO178PB5F16	W6
IO179NB5F16	Y10
IO179PB5F16	W10
IO180NB5F16	Y7
IO180PB5F16	W7
IO181NB5F17	AD9
IO181PB5F17	AD10
IO182NB5F17	AE10
IO182PB5F17	AE11
IO183NB5F17	AD7
IO183PB5F17	AD8
IO184NB5F17	AB9
IO185NB5F17	AE6
IO185PB5F17	AE7
IO186NB5F17	AE4
IO186PB5F17	AE5
IO187NB5F17	AA9
IO187PB5F17	Y9
IO188NB5F17	U8
IO189NB5F17	AD5
IO189PB5F17	AD6
IO191NB5F17	AC5
IO191PB5F17	AC6
IO192NB5F17	AB7
IO192PB5F17	AC7
Bank 6	
IO193NB6F18	U6
IO193PB6F18	U5