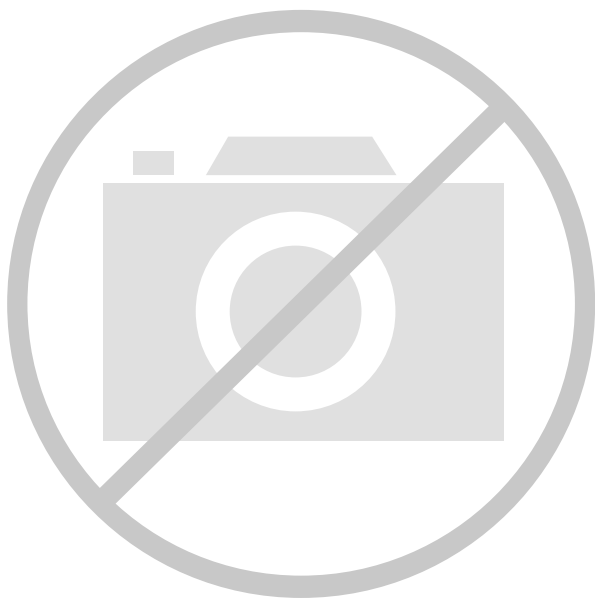




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	198
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	352-BFCQFP with Tie Bar
Supplier Device Package	352-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-1cq352m

Design Environment

The Axcelerator family of FPGAs is fully supported by both Microsemi's Libero[®] Integrated Design Environment and Designer FPGA Development software. Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE Flow* diagram located on the Microsemi SoC Products Group website). Libero IDE includes Synplify[®] Actel Edition (AE) from Synplicity[®], ViewDraw[®] AE from Mentor Graphics[®], ModelSim[®] HDL Simulator from Mentor Graphics, WaveFormer Lite[™] AE from SynaptiCAD[®], and Designer software from Microsemi.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor which support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Microsemi's back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Programming support is provided through Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. In addition, BP Microsystems offers multi-site programmers that provide qualified support for Microsemi devices. Factory programming is available for high-volume production needs.

In-System Diagnostic and Debug Capabilities

The Axcelerator family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation (Figure 1-9).

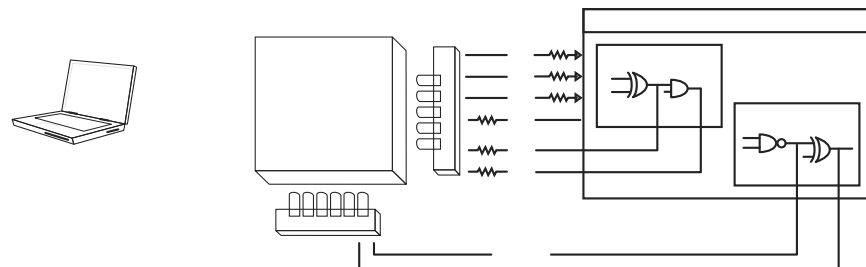


Figure 1-9 • Probe Setup

$$P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po}$$

C_{load} = the output load (technology dependent)
 V_{CCI} = the output voltage (technology dependent)
 po = the number of outputs
 F_{po} = the average output frequency

$$P_{\text{memory}} = P_{11} * N_{\text{block}} * FR_{\text{CLK}} + P_{12} * N_{\text{block}} * FW_{\text{CLK}}$$

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
 F_{RCLK} = the read-clock frequency of the memory
 F_{WCLK} = the write-clock frequency of the memory

$$P_{\text{PLL}} = P_{13} * F_{\text{CLK}}$$

F_{RefCLK} = the clock frequency of the clock input of the PLL
 F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
 F_s = 100 MHz
 s = 1080

$$\Rightarrow P_{\text{HCLK}} = (P_1 + P_2 * s + P_3 * \sqrt{s}) * F_s = 79 \text{ mW}$$

and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{R-cells}} = P_7 * ms * F_s = 173 \text{ mW}$$

mc = 1 (1 C-cell in this shift-register)
and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{C-cells}} = P_8 * mc * F_s = 0.14 \text{ mW}$$

$F_{pi} \sim 0 \text{ MHz}$

and $pi = 1$ (1 reset input => this is why $F_{pi} = 0$)

$$\Rightarrow P_{\text{inputs}} = P_9 * pi * F_{pi} = 0 \text{ mW}$$

$F_{po} = 50 \text{ MHz}$

and $po = 1$

$$\Rightarrow P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po} = 27.10 \text{ mW}$$

No RAM/FIFO in this shift-register

$$\Rightarrow P_{\text{memory}} = 0 \text{ mW}$$

No PLL in this shift-register

$$\Rightarrow P_{\text{PLL}} = 0 \text{ mW}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}} = 276 \text{ mW}$$

$$P_{\text{dc}} = 7.5\text{mA} * 1.5\text{V} = 11.25 \text{ mW}$$

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}} = 11.25 \text{ mW} + 276\text{mW} = 290.30 \text{ mW}$$

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		12.14		13.83		16.26	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Class II

Table 2-53 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16

AC Loadings

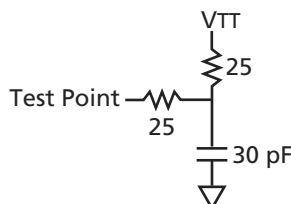


Figure 2-24 • AC Test Loads

Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-55 • 3.3 V SSTL3 Class II I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V SSTL3 Class II I/O Module Timing								
t _{DP}	Input Buffer		1.85		2.10		2.47	ns
t _{PY}	Output Buffer		2.17		2.47		2.91	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

R-Cell

Introduction

The R-cell, the sequential logic resource of the Axcelerator devices, is the second logic module type in the AX family architecture. It includes clock inputs for all eight global resources of the Axcelerator architecture as well as global presets and clears (Figure 2-31).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-Cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).
- Independent active-low asynchronous clear (CLR).
- Independent active-low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
 - One of the four high performance hardwired fast clocks (HCLKs)
 - One of the four routed clocks (CLKs)
 - User signals
- Global power-on clear (GCLR) and preset (GPSET), which drive each flip-flop on a chip-wide basis.
 - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET = 1 at device power-up. When the option is checked, GCLR = 1 and GPSET = 0. Both pins are pulled High when the device is in user mode. Refer to the "Simulation Support for GCLR/GPSET in Axcelerator" section of the *Antifuse Macro Library Guide* for information on simulation support for GCLR and GPSET.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Microsemi's extensive macro library (see the *Antifuse Macro Library Guide* for a complete listing of available AX macros).

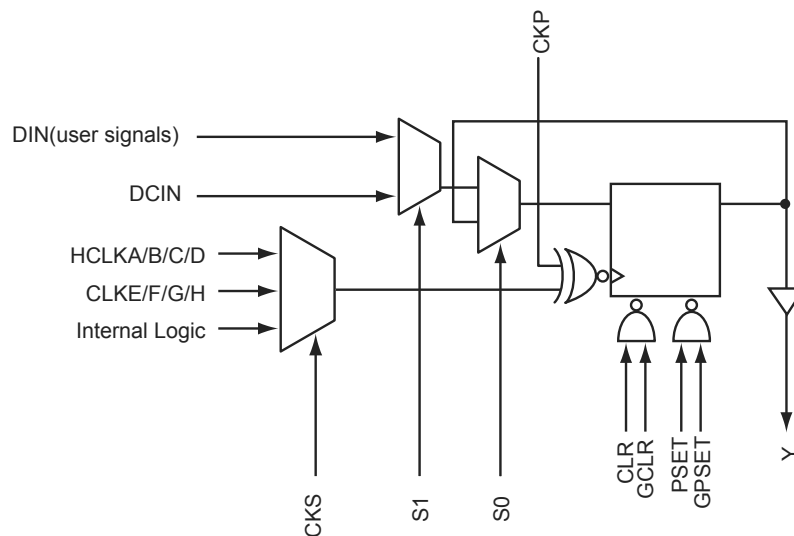


Figure 2-31 • R-Cell

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t _{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t _{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t _{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t _{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t _{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t _{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t _{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t _{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t _{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t _{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t _{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t _{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t _{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t _{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t _{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t _{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t _{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t _{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

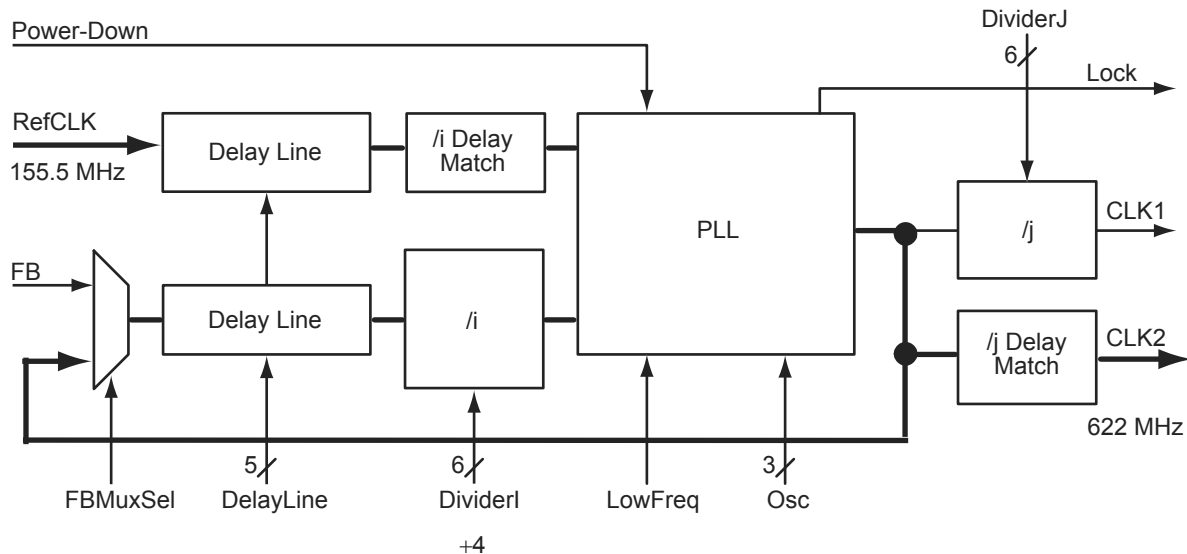


Figure 2-53 • Using the PLL 155.5 MHz In, 622 MHz Out

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

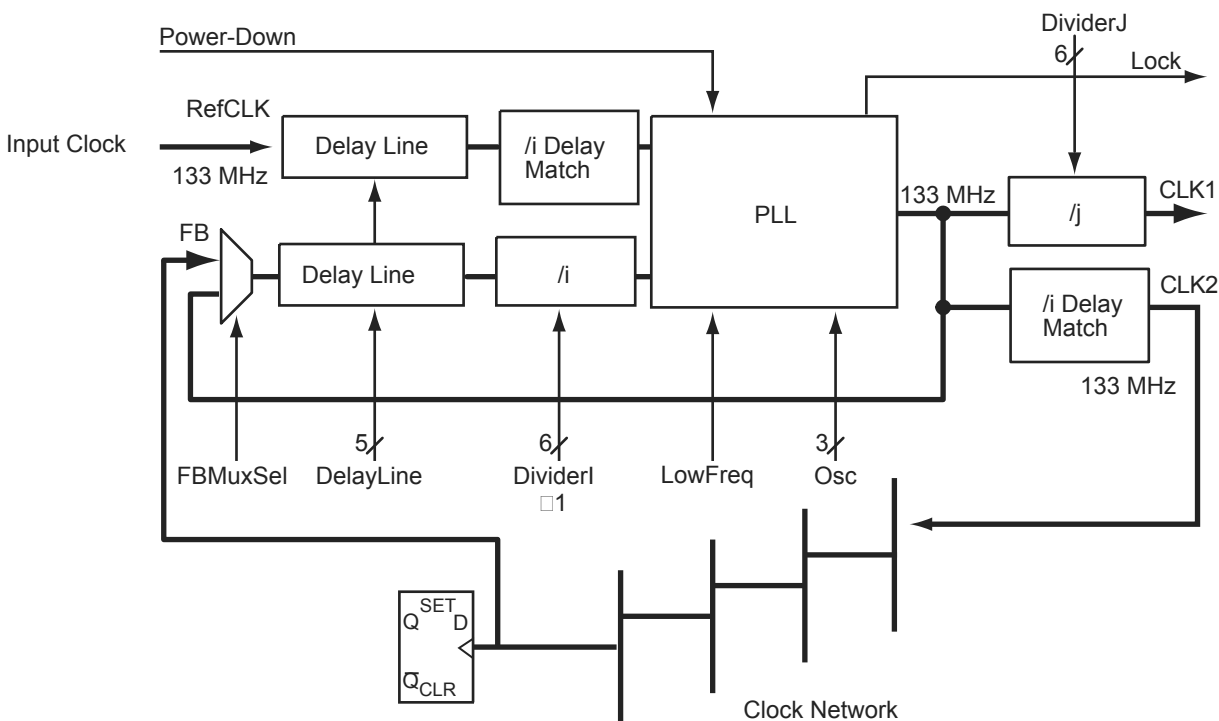


Figure 2-56 • Using the PLL for Clock Deskewing

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-86). Each block has independent read and write ports which enable simultaneous read and write operations.

Table 2-86 • Memory Block WxD Options

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in Table 2-87.

Table 2-87 • Allowable RW and WW Values

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

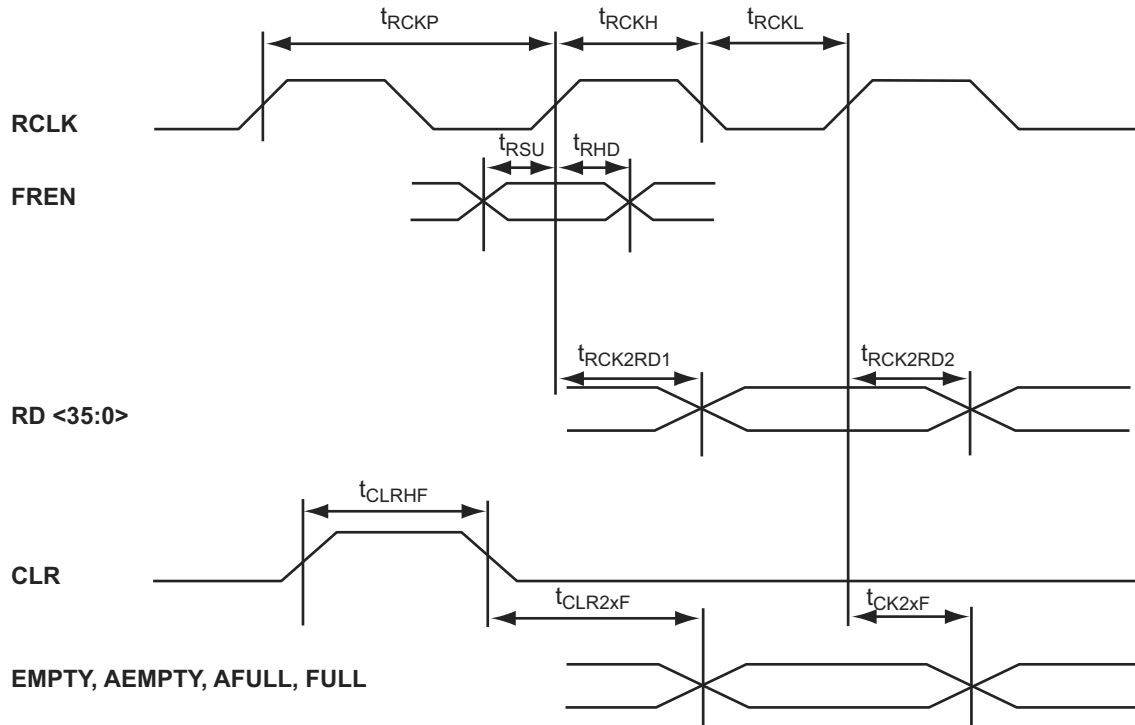


Figure 2-68 • FIFO Read Timing

mode if desired. Please note, if the I/O bank is not disabled, differential I/Os belonging to the I/O bank will still consume normal power, even when operating in the low power mode.

The Axcelerator device will resume normal operation 10 μ s after the LP pin is pulled Low.

To further reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e. high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

In addition, any PLL in use can be powered down to further reduce power consumption. This can be done with the PowerDown pin driven Low. Driving this pin High restarts the PLL with the output clock(s) being stable once lock is restored.

JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the Table 2-103.

Table 2-103 • JTAG Instruction Code

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload / Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
Reserved	All others
Bypass	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low, asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1 k Ω resistor.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a VCCA and/or VCCDA voltage drop.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO163PB5F15	AA14	IO182NB5F17	AF7	IO200NB6F18	AA4
IO164NB5F15	AE13	IO182PB5F17	AG7	IO200PB6F18	AA5
IO164PB5F15	AF13	IO183NB5F17	AD7	IO201NB6F18	W5
IO165NB5F15	AF12	IO183PB5F17	AE7	IO201PB6F18	W6
IO165PB5F15	AG12	IO184NB5F17	AC7	IO202NB6F18	AB1
IO166NB5F15	AD12	IO184PB5F17	AC8	IO202PB6F18	AC1
IO166PB5F15	AE12	IO185NB5F17	AF6	IO203NB6F19	Y3
IO167NB5F15	Y13	IO185PB5F17	AG6	IO203PB6F19	AA3
IO167PB5F15	AA13	IO186NB5F17	AB7	IO204NB6F19	AA2
IO168NB5F15	AD11	IO186PB5F17	AB8	IO204PB6F19	AB2
IO168PB5F15	AE11	IO187NB5F17	Y9	IO205NB6F19	U8
IO169NB5F15	AG11	IO187PB5F17	AA9	IO205PB6F19	V8
IO169PB5F15	AF11	IO188NB5F17	AD6	IO206NB6F19	V5
IO170NB5F15	AB11	IO188PB5F17	AE6	IO206PB6F19	V6
IO170PB5F15	AC11	IO189NB5F17	AB6	IO207NB6F19	Y1
IO171NB5F16	AF10	IO189PB5F17	AC6	IO207PB6F19	AA1
IO171PB5F16	AG10	IO190NB5F17	AF5	IO208NB6F19	W4
IO172NB5F16	AD10	IO190PB5F17	AG5	IO208PB6F19	Y4
IO172PB5F16	AE10	IO191NB5F17	AA6	IO209NB6F19	T7
IO173NB5F16	Y12	IO191PB5F17	AA7	IO209PB6F19	U7
IO173PB5F16	AA12	IO192NB5F17	Y8	IO210NB6F19	W2
IO174NB5F16	AB10	IO192PB5F17	AA8	IO210PB6F19	Y2
IO174PB5F16	AC10	Bank 6		IO211NB6F19	U5
IO175NB5F16	AF9	IO193NB6F18	W8	IO211PB6F19	U6
IO175PB5F16	AG9	IO193PB6F18	Y7	IO212NB6F19	V3
IO176NB5F16	AD9	IO194NB6F18	AB5	IO212PB6F19	W3
IO176PB5F16	AE9	IO194PB6F18	AC5	IO213NB6F19	R9
IO177NB5F16	Y11	IO195NB6F18	AC2	IO213PB6F19	T8
IO177PB5F16	AA11	IO195PB6F18	AC3	IO214NB6F20	U4
IO178NB5F16	AF8	IO196NB6F18	AC4	IO214PB6F20	V4
IO178PB5F16	AG8	IO196PB6F18	AD4	IO215NB6F20	T5
IO179NB5F16	AD8	IO197NB6F18	Y5	IO215PB6F20	T6
IO179PB5F16	AE8	IO197PB6F18	Y6	IO216NB6F20	V1
IO180NB5F16	AB9	IO198NB6F18	AB3	IO216PB6F20	W1
IO180PB5F16	AC9	IO198PB6F18	AB4	IO217NB6F20	R7
IO181NB5F17	Y10	IO199NB6F18	V7	IO217PB6F20	R8
IO181PB5F17	AA10	IO199PB6F18	W7	IO218NB6F20	U2

FG676	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10

FG676	
AX1000 Function	Pin Number
IO21PB0F1	C10
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
Bank 1	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20

FG676	
AX1000 Function	Pin Number
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20
IO52PB1F4	C20
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
Bank 2	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24

FG896	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8

FG896	
AX2000 Function	Pin Number
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15

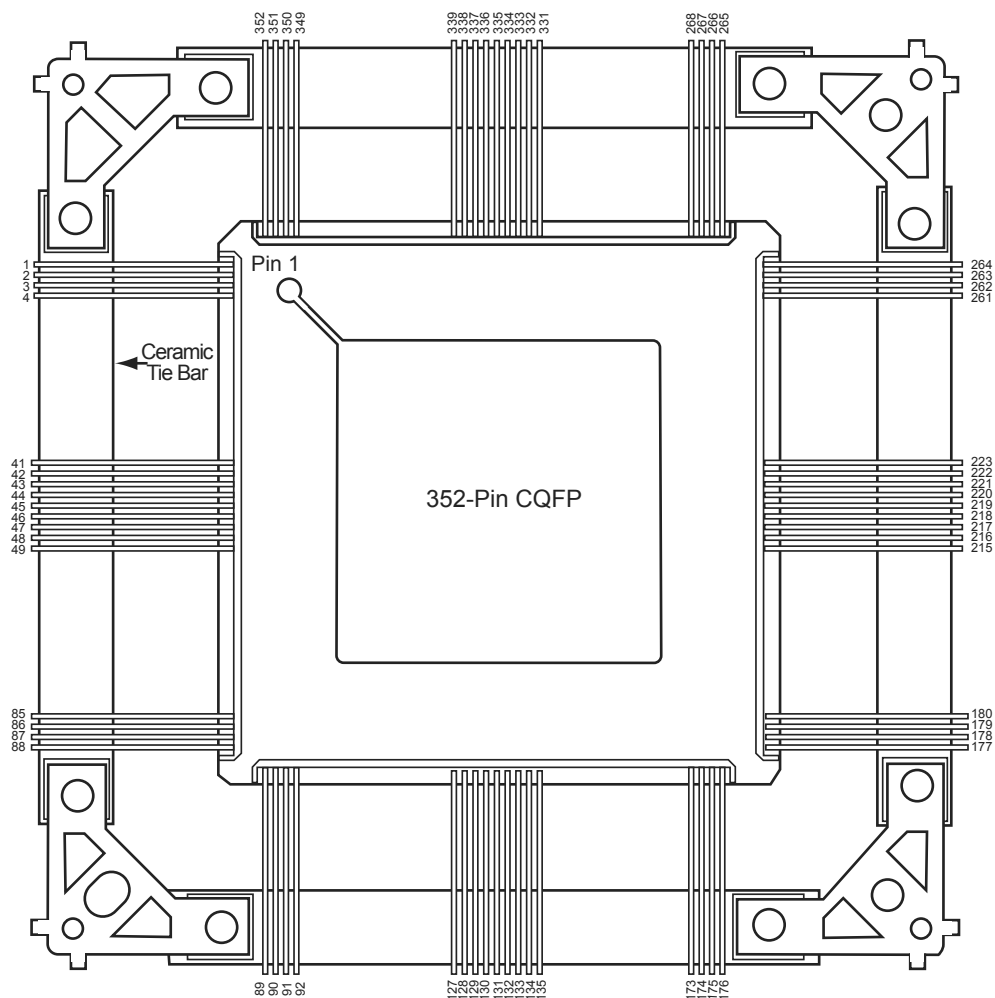
FG896	
AX2000 Function	Pin Number
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20

FG896		FG896		FG896	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	W19	VCCA	U11	VCCDA	G16
GND	Y11	VCCA	U20	VCCDA	T25
GND	Y20	VCCA	V11	VCCDA	T4
GND/LP	E4	VCCA	V20	VCCIB0	A3
PRA	G15	VCCA	W11	VCCIB0	B3
PRB	D16	VCCA	W20	VCCIB0	J10
PRC	AB16	VCCA	Y12	VCCIB0	J11
PRD	AF16	VCCA	Y13	VCCIB0	J12
TCK	G7	VCCA	Y14	VCCIB0	K11
TDI	D5	VCCA	Y15	VCCIB0	K12
TDO	J8	VCCA	Y16	VCCIB0	K13
TMS	F6	VCCA	Y17	VCCIB0	K14
TRST	C4	VCCA	Y18	VCCIB0	K15
VCCA	AD6	VCCA	Y19	VCCIB1	A28
VCCA	AH26	VCCDA	AD24	VCCIB1	B28
VCCA	E28	VCCDA	AD7	VCCIB1	J19
VCCA	E3	VCCDA	AE15	VCCIB1	J20
VCCA	L12	VCCDA	AE16	VCCIB1	J21
VCCA	L13	VCCDA	AF12	VCCIB1	K16
VCCA	L14	VCCDA	AF13	VCCIB1	K17
VCCA	L15	VCCDA	AF15	VCCIB1	K18
VCCA	L16	VCCDA	AF18	VCCIB1	K19
VCCA	L17	VCCDA	AF19	VCCIB1	K20
VCCA	L18	VCCDA	AH27	VCCIB2	C29
VCCA	L19	VCCDA	AH4	VCCIB2	C30
VCCA	M11	VCCDA	C13	VCCIB2	K22
VCCA	M20	VCCDA	C27	VCCIB2	L21
VCCA	N11	VCCDA	C5	VCCIB2	L22
VCCA	N20	VCCDA	D13	VCCIB2	M21
VCCA	P11	VCCDA	D19	VCCIB2	M22
VCCA	P20	VCCDA	D3	VCCIB2	N21
VCCA	R11	VCCDA	E18	VCCIB2	P21
VCCA	R20	VCCDA	F15	VCCIB2	R21
VCCA	T11	VCCDA	F16	VCCIB3	AA22
VCCA	T20	VCCDA	F26	VCCIB3	AH29

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO51PB1F4	J20	IO69NB1F6	C27	IO86NB2F8	J28
IO52NB1F4	B20	IO69PB1F6	C26	IO86PB2F8	J27
IO52PB1F4	A20	IO70NB1F6	H24	IO87NB2F8	M25
IO53NB1F4	F20	IO70PB1F6	G24	IO87PB2F8	L25
IO53PB1F4	E20	IO71NB1F6	H23	IO88NB2F8	L26
IO54NB1F5	B21	IO71PB1F6	G23	IO88PB2F8	K26
IO54PB1F5	A21	IO72NB1F6	B28	IO89NB2F8	G31
IO55NB1F5	K21	IO72PB1F6	A28	IO89PB2F8	F31
IO55PB1F5	J21	IO73NB1F6	E26	IO90NB2F8	H29
IO56NB1F5	D21	IO73PB1F6	E25	IO90PB2F8	G29
IO56PB1F5	C21	IO74NB1F6	F26	IO91NB2F8	K28
IO57NB1F5	G22	IO74PB1F6	F25	IO91PB2F8	K27
IO57PB1F5	G21	IO75NB1F6	K25	IO92NB2F8	J30
IO58NB1F5	E22	IO75PB1F6	K24	IO92PB2F8	H30
IO58PB1F5	E21	IO76NB1F7	D27	IO93NB2F8	L28
IO59NB1F5	D22	IO76PB1F7	D26	IO93PB2F8	L27
IO59PB1F5	C22	IO77NB1F7	B29	IO94NB2F8	K29
IO60NB1F5	B23	IO77PB1F7	A29	IO94PB2F8	J29
IO60PB1F5	A23	IO78NB1F7	D28	IO95NB2F8	K31
IO61NB1F5	H22	IO78PB1F7	C28	IO95PB2F8	J31
IO61PB1F5	H21	IO79NB1F7	H25	IO96NB2F9	J32
IO62NB1F5	C24	IO79PB1F7	G25	IO96PB2F9	H32
IO62PB1F5	C23	IO80NB1F7	F27	IO97NB2F9	M27
IO63NB1F5	F23	IO80PB1F7	E27	IO97PB2F9	M26
IO63PB1F5	F22	IO81NB1F7	J25	IO98NB2F9	L30
IO64NB1F6	B24	IO81PB1F7	J24	IO98PB2F9	K30
IO64PB1F6	A24	IO82NB1F7	D29	IO99NB2F9	N25
IO65NB1F6	J22	IO82PB1F7	C29	IO99PB2F9	N26
IO65PB1F6	K22	IO83NB1F7	H26	IO100NB2F9	M29
IO66NB1F6	B25	IO83PB1F7	G26	IO100PB2F9	L29
IO66PB1F6	A25	IO84NB1F7	F28	IO101NB2F9	L33
IO67NB1F6	K23	IO84PB1F7	E28	IO101PB2F9	L32
IO67PB1F6	J23	IO85NB1F7	H27	IO102NB2F9	K34
IO68NB1F6	F24	IO85PB1F7	G27	IO102PB2F9	K33
IO68PB1F6	E24	Bank 2		IO103NB2F9	N28

CQ352



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CQ352	
AX250 Function	Pin Number
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282

CQ352	
AX250 Function	Pin Number
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224

CQ352	
AX250 Function	Pin Number
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0		IO60NB1F5	275	Bank 3	
IO02NB0F0	341	IO60PB1F5	276	IO96NB3F9	217
IO02PB0F0	342	IO61NB1F5	271	IO96PB3F9	218
IO03PB0F0	343	IO61PB1F5	272	IO97NB3F9	219
IO04NB0F0	337	IO63NB1F5	269	IO97PB3F9	220
IO04PB0F0	338	IO63PB1F5	270	IO99NB3F9	213
IO08NB0F0	331	Bank 2		IO99PB3F9	214
IO08PB0F0	332	IO64NB2F6	259	IO108NB3F10	211
IO09NB0F0	335	IO64PB2F6	260	IO108PB3F10	212
IO09PB0F0	336	IO67NB2F6	261	IO109NB3F10	207
IO24NB0F2	325	IO67PB2F6	262	IO109PB3F10	208
IO24PB0F2	326	IO68NB2F6	255	IO111NB3F10	205
IO25NB0F2	323	IO68PB2F6	256	IO111PB3F10	206
IO25PB0F2	324	IO69NB2F6	253	IO112NB3F10	199
IO30NB0F2/HCLKAN	319	IO69PB2F6	254	IO112PB3F10	200
IO30PB0F2/HCLKAP	320	IO74NB2F7	249	IO113NB3F10	201
IO31NB0F2/HCLKBN	313	IO74PB2F7	250	IO113PB3F10	202
IO31PB0F2/HCLKBP	314	IO75NB2F7	247	IO115NB3F10	195
Bank 1		IO75PB2F7	248	IO115PB3F10	196
IO32NB1F3/HCLKCN	305	IO76NB2F7	243	IO116NB3F10	193
IO32PB1F3/HCLKCP	306	IO76PB2F7	244	IO116PB3F10	194
IO33NB1F3/HCLKDN	299	IO77NB2F7	241	IO117NB3F10	189
IO33PB1F3/HCLKDP	300	IO77PB2F7	242	IO117PB3F10	190
IO38NB1F3	295	IO78NB2F7	237	IO124NB3F11	183
IO38PB1F3	296	IO78PB2F7	238	IO124PB3F11	184
IO54NB1F5	287	IO79NB2F7	235	IO125NB3F11	187
IO54PB1F5	288	IO79PB2F7	236	IO125PB3F11	188
IO55NB1F5	289	IO82NB2F7	231	IO127NB3F11	181
IO55PB1F5	290	IO82PB2F7	232	IO127PB3F11	182
IO56NB1F5	281	IO83NB2F7	229	IO128NB3F11	179
IO56PB1F5	282	IO83PB2F7	230	IO128PB3F11	180
IO57NB1F5	283	IO94NB2F8	225	Bank 4	
IO57PB1F5	284	IO94PB2F8	226	IO130NB4F12	172
IO59NB1F5	277	IO95NB2F8	223	IO130PB4F12	173
IO59PB1F5	278	IO95PB2F8	224	IO131NB4F12	170

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
VCCA	U17	VCCIB2	D23	VCCIB7	E4
VCCA	U9	VCCIB2	E22	VCCIB7	K9
VCCA	Y4	VCCIB2	K17	VCCIB7	L9
VCCDA	A12	VCCIB2	L17	VCCIB7	M10
VCCDA	AA13	VCCIB2	M16	VCCPLA	E12
VCCDA	AA15	VCCIB3	AA22	VCCPLB	J12
VCCDA	AA7	VCCIB3	AB23	VCCPLC	E14
VCCDA	AC11	VCCIB3	AC24	VCCPLD	H14
VCCDA	AD11	VCCIB3	AC25	VCCPLE	Y14
VCCDA	AE17	VCCIB3	P16	VCCPLF	U14
VCCDA	B15	VCCIB3	R17	VCCPLG	Y12
VCCDA	C15	VCCIB3	T17	VCCPLH	U12
VCCDA	C6	VCCIB4	AB21	VCOMPLA	F12
VCCDA	D13	VCCIB4	AC22	VCOMPLB	H12
VCCDA	E13	VCCIB4	AD23	VCOMPLC	F14
VCCDA	E19	VCCIB4	AE23	VCOMPLD	J14
VCCDA	G5	VCCIB4	T14	VCOMPLE	AA14
VCCDA	N21	VCCIB4	U15	VCOMPLF	V14
VCCDA	N5	VCCIB4	U16	VCOMPLG	AA12
VCCDA	W21	VCCIB5	AB5	VCOMPLH	V12
VCCIB0	A3	VCCIB5	AC4	VPUMP	E20
VCCIB0	B3	VCCIB5	AD3		
VCCIB0	C4	VCCIB5	AE3		
VCCIB0	D5	VCCIB5	T12		
VCCIB0	J10	VCCIB5	U10		
VCCIB0	J11	VCCIB5	U11		
VCCIB0	K12	VCCIB6	AA4		
VCCIB1	A23	VCCIB6	AB3		
VCCIB1	B23	VCCIB6	AC1		
VCCIB1	C22	VCCIB6	AC2		
VCCIB1	D21	VCCIB6	P10		
VCCIB1	J15	VCCIB6	R9		
VCCIB1	J16	VCCIB6	T9		
VCCIB1	K14	VCCIB7	C1		
VCCIB2	C24	VCCIB7	C2		
VCCIB2	C25	VCCIB7	D3		