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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	684
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	1152-BGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-1fgg1152m

1 – General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microsemi AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

Device Architecture

AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

The very nature of Microsemi's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-108).

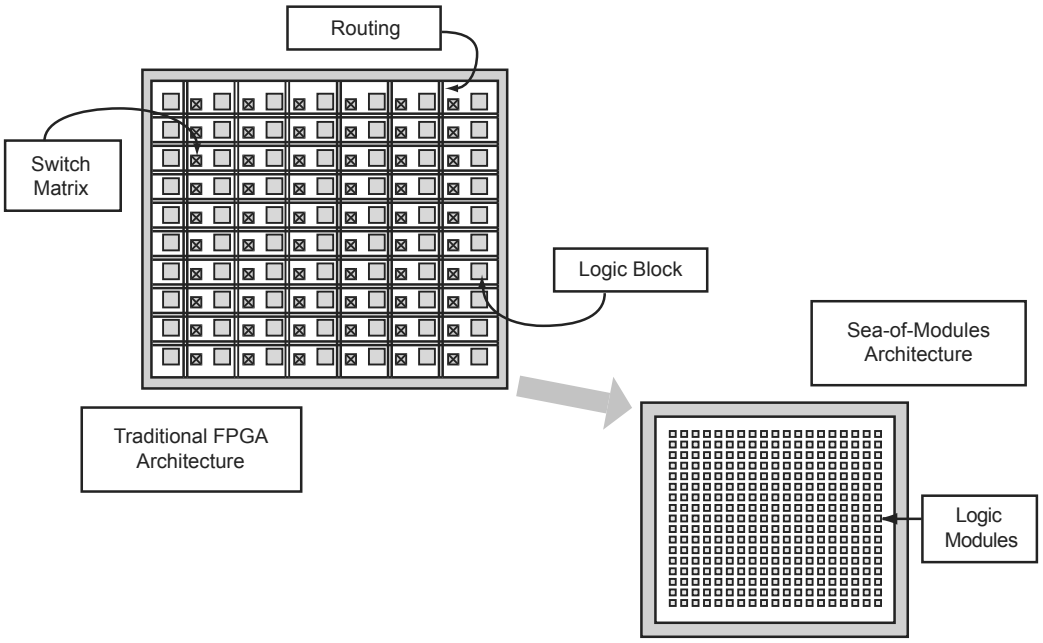


Figure 1-1 • **Sea-of-Modules Comparison**

2 – Detailed Specifications

Operating Conditions

Table 2-1 lists the absolute maximum ratings of Axcelerator devices. Stresses beyond the ratings may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommendations in Table 2-2.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCCA	DC Core Supply Voltage	–0.3 to 1.7	V
VCCI	DC I/O Supply Voltage	–0.3 to 3.75	V
VREF	DC I/O Reference Voltage	–0.3 to 3.75	V
VI	Input Voltage	–0.5 to 4.1	V
VO	Output Voltage	–0.5 to 3.75	V
TSTG	Storage Temperature	–60 to +150	°C
VCCDA*	Supply Voltage for Differential I/Os	–0.3 to 3.75	V

*Note: * Should be the maximum of all VCCI.*

Table 2-2 • **Recommended Operating Conditions**

Parameter Range	Commercial	Industrial	Military	Units
Ambient Temperature (T_A)[1]	0 to +70	–40 to +85	–55 to +125	°C
1.5 V Core Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.5 V I/O Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.8 V I/O Supply Voltage	1.71 to 1.89	1.71 to 1.89	1.71 to 1.89	V
2.5 V I/O Supply Voltage	2.375 to 2.625	2.375 to 2.625	2.375 to 2.625	V
3.3 V I/O Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCDA Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VPUMP Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*
2. *T_J max = 125°C*

Power-Up/Down Sequence

All Axcelerator I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. VCCDA should be powered up before (or coincidentally with) VCCA and VCCI to ensure the behavior of user I/Os at system start-up. Conversely, VCCDA should be powered down after (or coincidentally with) VCCA and VCCI. Note that VCCI and VCCA can be powered up in any sequence with respect to each other, provided the requirement with respect to VCCDA is satisfied.

Table 2-5 • **Different Components Contributing to the Total Power Consumption in Axcelerator Devices**

Component	Definition	Device Specific Value (in µW/MHz)				
		AX125	AX250	AX500	AX1000	AX2000
P1	Core tile HCLK power component	33	49	71	130	216
P2	R-cell power component	0.2	0.2	0.2	0.2	0.2
P3	HCLK signal power dissipation	4.5	4.5	9	13.5	18
P4	Core tile RCLK power component	33	49	71	130	216
P5	R-cell power component	0.3	0.3	0.3	0.3	0.3
P6	RCLK signal power dissipation	6.5	6.5	13	19.5	26
P7	Power dissipation due to the switching activity on the R-cell	1.6	1.6	1.6	1.6	1.6
P8	Power dissipation due to the switching activity on the C-cell	1.4	1.4	1.4	1.4	1.4
P9	Power component associated with the input voltage	10	10	10	10	10
P10	Power component associated with the output voltage	See table Per pin contribution				
P11	Power component associated with the read operation in the RAM block	25	25	25	25	25
P12	Power component associated with the write operation in the RAM block	30	30	30	30	30
P13	Core PLL power component	1.5	1.5	1.5	1.5	1.5

Ptotal = Pdc + Pac

P_{dc} = ICCA * VCCA

P_{ac} = $P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$

P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs

s = the number of R-cells clocked by this clock

Fs = the clock frequency

PCLK = (P4 + P5 * s + P6 * sqrt[s]) * Fs

s = the number of R-cells clocked by this clock

Fs = the clock frequency

PR-cells = P7 * ms * Fs

ms = the number of R-cells switching at each Fs cycle

Fs = the clock frequency

PC-cells = P8 * mc * Fs

mc = the number of C-cells switching at each Fs cycle

Fs = the clock frequency

Pinputs = P9 * pi * Fpi

pi = the number of inputs

F_{pi} = the average input frequency

5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

EQ 3

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

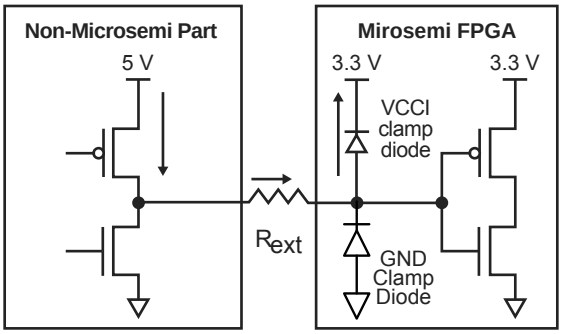


Figure 2-3 • **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

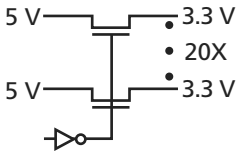


Figure 2-4 • **Bus Switch IDTQS32X2384**

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

3. The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.

I/O Clusters

Each I/O cluster incorporates two I/O modules, four RX modules, two TX modules, and a buffer module. In turn, each I/O module contains one Input Register (InReg), one Output Register (OutReg), and one Enable Register (EnReg) (Figure 2-5).

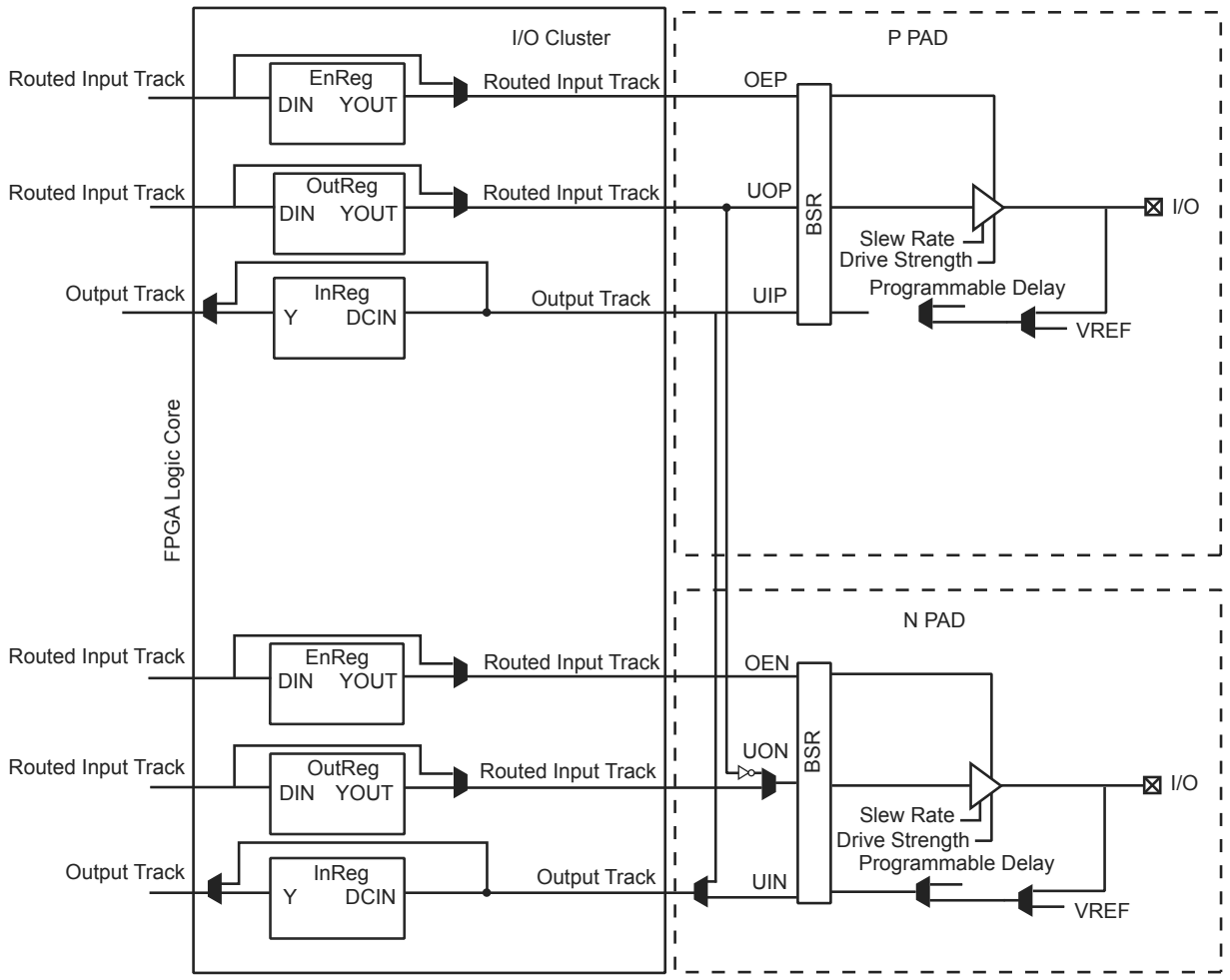


Figure 2-5 • **I/O Cluster Interface**

Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. Usage of each I/O register (register combining) is individually controlled and can be selected/deselected using the PinEditor tool in the Designer software. I/O register combining can also be controlled at the device level, affecting all I/Os. Please note, the I/O register option is deselected by default in any given design.[4]

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design-specific. The setting for each individual I/O overrides this global option. Furthermore, the *global set fuse* option in the Designer software, when checked, causes all I/O registers to output logic High at device power-up.

4. Please note that register combining for multi fanout nets is not supported.

Table 2-15, Table 2-16, and Table 2-17 list all the available macro names differentiated by I/O standard, type, slew rate, and drive strength.

***Table 2-15* • Macros for Single-Ended I/O Standards**

Standard	VCCI	Macro Names
LVTTL	3.3 V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_H_8, OUTBUF_H_12, OUTBUF_H_16, OUTBUF_H_24, TRIBUF, TRIBUF_S_8, TRIBUF_S_12, TRIBUF_S_16, TRIBUF_S_24, TRIBUF_H_8, TRIBUF_H_12, TRIBUF_H_16, TRIBUF_H_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_H_8, BIBUF_H_12, BIBUF_H_16, BIBUF_H_24
3.3 V PCI	3.3 V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUF_PCI, BIBUF_PCI
3.3 V PCI-X	3.3 V	CLKBUF_PCI-X, HCLKBUF_PCI-X, INBUF_PCI-X, OUTBUF_PCI-X, TRIBUF_PCI-X, BIBUF_PCI-X
LVCMOS25	2.5 V	CLKBUF_LVCMOS25, HCLKBUF_LVCMOS25, INBUF_LVCMOS25, OUTBUF_LVCMOS25, TRIBUF_LVCMOS25, BIBUF_LVCMOS25
LVCMOS18	1.8 V	CLKBUF_LVCMOS18, HCLKBUF_LVCMOS18, INBUF_LVCMOS18, OUTBUF_LVCMOS18, TRIBUF_LVCMOS18, BIBUF_LVCMOS18
LVCMOS15 (JESD8-11)	1.5 V	CLKBUF_LVCMOS15, HCLKBUF_LVCMOS15, INBUF_LVCMOS15, OUTBUF_LVCMOS15, TRIBUF_LVCMOS15, BIBUF_LVCMOS15

***Table 2-16* • I/O Macros for Differential I/O Standards**

Standard	VCCI	Macro Names
LVPECL	3.3 V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL
LVDS	2.5 V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS

***Table 2-17* • I/O Macros for Voltage-Referenced I/O Standards**

Standard	VCCI	VREF	Macro Names
GTL+	3.3 V	1.0 V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUF_GTP33, BIBUF_GTP33
GTL+	2.5 V	1.0 V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUF_GTP25, BIBUF_GTP25
SSTL2 Class I	2.5 V	1.25 V	CLKBUF_SSTL2_I, HCLKBUF_SSTL2_I, INBUF_SSTL2_I, OUTBUF_SSTL2_I, TRIBUF_SSTL2_I, BIBUF_SSTL2_I
SSTL2 Class II	2.5 V	1.25 V	CLKBUF_SSTL2_II, HCLKBUF_SSTL2_II, INBUF_SSTL2_II, OUTBUF_SSTL2_II, TRIBUF_SSTL2_II, BIBUF_SSTL2_II
SSTL3 Class I	3.3 V	1.5 V	CLKBUF_SSTL3_I, HCLKBUF_SSTL3_I, INBUF_SSTL3_I, OUTBUF_SSTL3_I, TRIBUF_SSTL3_I, BIBUF_SSTL3_I
SSTL3 Class II	3.3 V	1.5 V	CLKBUF_SSTL3_II, HCLKBUF_SSTL3_II, INBUF_SSTL3_II, OUTBUF_SSTL3_II, TRIBUF_SSTL3_II, BIBUF_SSTL3_II
HSTL Class I	1.5 V	0.75 V	CLKBUF_HSTL_I, HCLKBUF_HSTL_I, INBUF_HSTL_I, OUTBUF_HSTL_I, TRIBUF_HSTL_I, BIBUF_HSTL_I

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		12.14		13.83		16.26	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

***Table 2-28* • 1.8V LVCMOS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.7 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVCMOS18 Output Module Timing								
t_{DP}	Input Buffer		3.26		3.71		4.37	ns
t_{PY}	Output Buffer		4.55		5.18		6.09	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.82		2.83		2.84	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.43		3.45		3.46	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.01		6.85		8.05	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.73		7.67		9.01	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

***Table 2-70* • AX125 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-71* • AX250 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

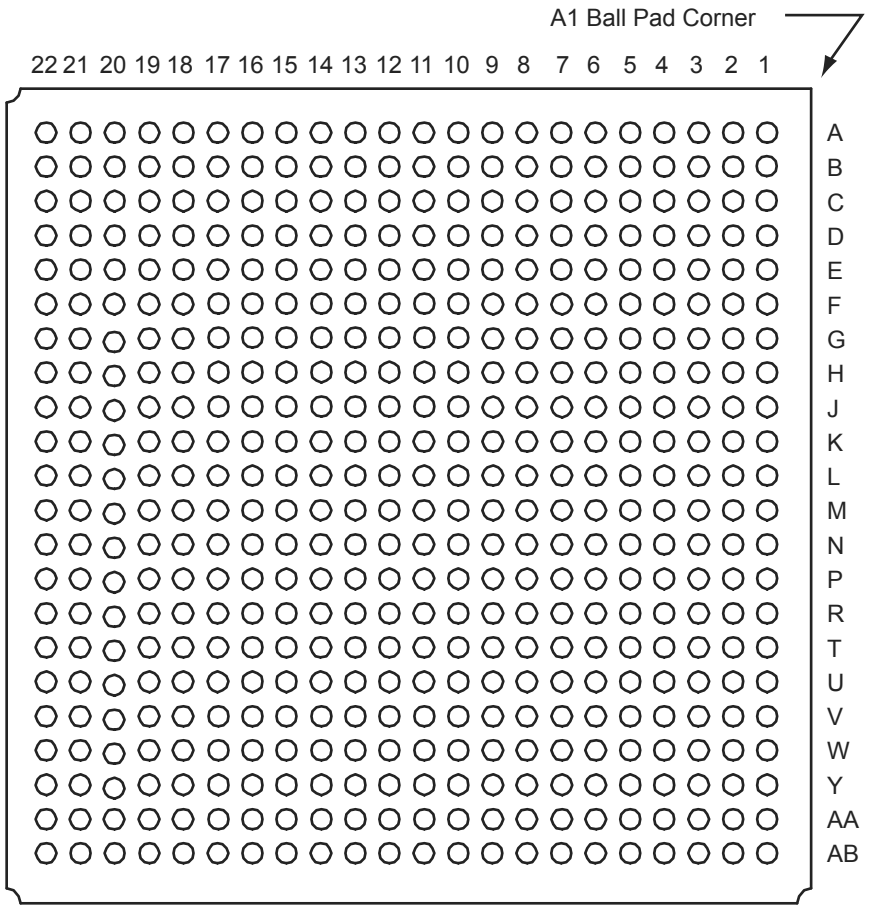
		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t_{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-83* • South PLL Connections**

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).

FG484



Note

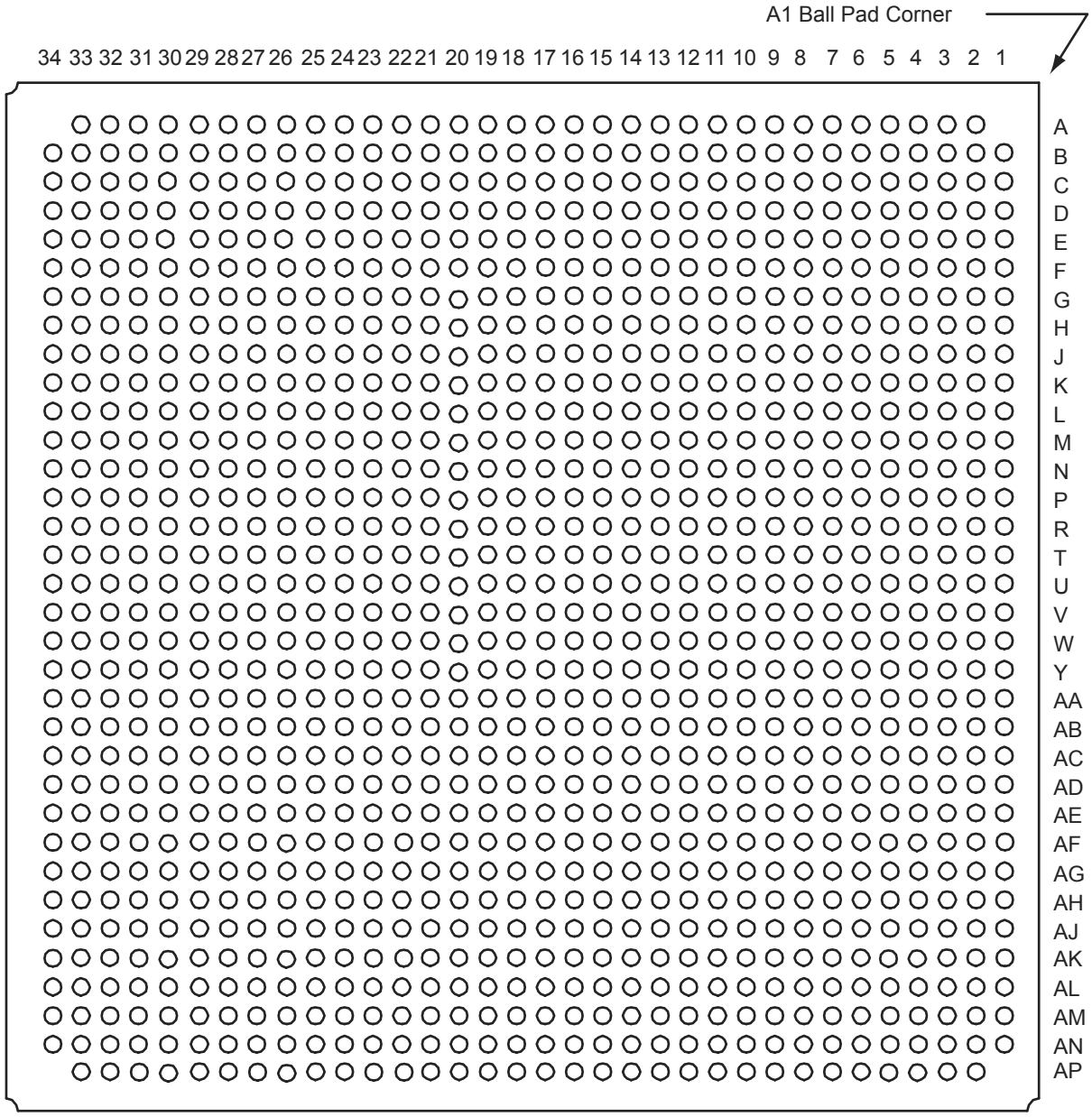
For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG676	
AX1000 Function	**Pin Number**
IO129PB4F12	AA21
IO131NB4F12	AD22
IO131PB4F12	AD23
IO132NB4F12	AE23
IO132PB4F12	AE24
IO133NB4F12	AB20
IO133PB4F12	AA20
IO134NB4F12	AC21
IO134PB4F12	AC22
IO135NB4F12	AF22
IO135PB4F12	AF23
IO137NB4F12	AB19
IO137PB4F12	AA19
IO139NB4F13	AC19
IO139PB4F13	AC20
IO140NB4F13	AE21
IO140PB4F13	AE22
IO141NB4F13	AD20
IO141PB4F13	AD21
IO143NB4F13	AB17
IO143PB4F13	AB18
IO144NB4F13	AE19
IO144PB4F13	AE20
IO145NB4F13	AC17
IO145PB4F13	AC18
IO146NB4F13	AD18
IO146PB4F13	AD19
IO147NB4F13	AA17
IO147PB4F13	AA18
IO148NB4F13	AF20
IO148PB4F13	AF21
IO149NB4F13	AA16
IO149PB4F13	Y16
IO151NB4F13	AC16
IO151PB4F13	AB16
IO153NB4F14	AE17

FG676	
AX1000 Function	**Pin Number**
IO153PB4F14	AE18
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AA15
IO155PB4F14	Y15
IO157NB4F14	AC15
IO157PB4F14	AB15
IO159NB4F14/CLKEN	AE16
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AE14
IO160PB4F14/CLKFP	AE15
Bank 5	
IO161NB5F15/CLKGN	AE12
IO161PB5F15/CLKGP	AE13
IO162NB5F15/CLKHN	AE11
IO162PB5F15/CLKHP	AF11
IO163NB5F15	AC12
IO163PB5F15	AB12
IO165NB5F15	Y12
IO165PB5F15	AA13
IO167NB5F15	Y11
IO167PB5F15	AA12
IO168NB5F15	AF9
IO168PB5F15	AF10
IO169NB5F15	AB11
IO169PB5F15	AA11
IO171NB5F16	AE9
IO171PB5F16	AE10
IO173NB5F16	AC10
IO173PB5F16	AC11
IO174NB5F16	AE7
IO174PB5F16	AE8
IO175NB5F16	AC9
IO175PB5F16	AD9
IO176NB5F16	AF6
IO176PB5F16	AF7

FG676	
AX1000 Function	**Pin Number**
IO177NB5F16	AA10
IO177PB5F16	AB10
IO179NB5F16	AD7
IO179PB5F16	AD8
IO180NB5F16	AC7
IO180PB5F16	AC8
IO181NB5F17	AA9
IO181PB5F17	AB9
IO183NB5F17	AD6
IO183PB5F17	AE6
IO184NB5F17	AE5
IO184PB5F17	AF5
IO185NB5F17	AA8
IO185PB5F17	AB8
IO187NB5F17	AC5
IO187PB5F17	AC6
IO188NB5F17	AD4
IO188PB5F17	AD5
IO189NB5F17	AB6
IO189PB5F17	AB7
IO190NB5F17	AF4
IO190PB5F17	AE4
IO191NB5F17	AE3
IO191PB5F17	AF3
IO192NB5F17	AA6
IO192PB5F17	AA7
Bank 6	
IO193NB6F18	Y5
IO193PB6F18	AA5
IO194NB6F18	AB3
IO194PB6F18	AC3
IO195NB6F18	Y4
IO195PB6F18	AA4
IO196NB6F18	AC2
IO196PB6F18	AD2
IO197NB6F18	W6

FG1152



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

PQ208	
AX500 Function	**Pin Number**
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
V_{CCDA}	1
V_{CCDA}	26
V_{CCDA}	53
V_{CCDA}	63
V_{CCDA}	78
V_{CCDA}	95
V_{CCDA}	105
V_{CCDA}	130
V_{CCDA}	157
V_{CCDA}	167
V_{CCDA}	182
V_{CCDA}	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX500 Function	**Pin Number**
GND	94
GND	99
GND	113
GND	119
GND	125
GND	143
GND	136
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX500 Function	**Pin Number**
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	200
VCCIB0	193
VCCIB1	172
VCCIB1	163
VCCIB2	149
VCCIB2	135
VCCIB3	124
VCCIB3	112
VCCIB4	98
VCCIB4	89
VCCIB5	68
VCCIB5	58
VCCIB6	45
VCCIB6	31
VCCIB7	20
VCCIB7	8
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ256	
AX2000 Function	**Pin Number**
VCCA	4
VCCA	22
VCCA	42
VCCA	61
VCCA	63
VCCA	84
VCCA	108
VCCA	127
VCCA	131
VCCA	150
VCCA	170
VCCA	189
VCCA	191
VCCA	212
VCCA	238
VCCDA	2
VCCDA	32
VCCDA	66
VCCDA	67
VCCDA	86
VCCDA	87
VCCDA	94
VCCDA	95
VCCDA	96
VCCDA	106
VCCDA	107
VCCDA	126
VCCDA	130
VCCDA	160
VCCDA	194
VCCDA	196
VCCDA	214
VCCDA	215
VCCDA	222
VCCDA	223

CQ256	
AX2000 Function	**Pin Number**
VCCDA	224
VCCDA	236
VCCDA	237
VCCDA	251
VCCIB0	230
VCCIB0	244
VCCIB1	200
VCCIB1	206
VCCIB1	218
VCCIB2	164
VCCIB2	176
VCCIB2	182
VCCIB3	138
VCCIB3	144
VCCIB3	156
VCCIB4	102
VCCIB4	114
VCCIB4	120
VCCIB5	72
VCCIB5	78
VCCIB5	90
VCCIB6	36
VCCIB6	48
VCCIB6	54
VCCIB7	10
VCCIB7	16
VCCIB7	28
VPUMP	195

CQ352	
AX500 Function	Pin Number
Bank 0	
IO00PB0F0	343
IO03NB0F0	341
IO03PB0F0	342
IO05NB0F0	337
IO05PB0F0	338
IO07NB0F0	335
IO07PB0F0	336
IO09NB0F0	331
IO09PB0F0	332
IO15NB0F1	325
IO15PB0F1	326
IO17NB0F1	323
IO17PB0F1	324
IO19NB0F1/HCLKAN	319
IO19PB0F1/HCLKAP	320
IO20NB0F1/HCLKBN	313
IO20PB0F1/HCLKBP	314
Bank 1	
IO21NB1F2/HCLKCN	305
IO21PB1F2/HCLKCP	306
IO22NB1F2/HCLKDN	299
IO22PB1F2/HCLKDP	300
IO23NB1F2	289
IO23PB1F2	290
IO24NB1F2	295
IO24PB1F2	296
IO25NB1F2	287
IO25PB1F2	288
IO27NB1F2	283
IO27PB1F2	284
IO29NB1F2	281
IO29PB1F2	282
IO31NB1F2	277
IO31PB1F2	278

CQ352	
AX500 Function	Pin Number
IO35NB1F3	275
IO35PB1F3	276
IO37NB1F3	271
IO37PB1F3	272
IO41NB1F3	269
IO41PB1F3	270
Bank 2	
IO43NB2F4	261
IO43PB2F4	262
IO45NB2F4	259
IO45PB2F4	260
IO47NB2F4	255
IO47PB2F4	256
IO49NB2F4	253
IO49PB2F4	254
IO50NB2F4	247
IO50PB2F4	248
IO51NB2F4	249
IO51PB2F4	250
IO53NB2F5	243
IO53PB2F5	244
IO54NB2F5	241
IO54PB2F5	242
IO55NB2F5	237
IO55PB2F5	238
IO57NB2F5	235
IO57PB2F5	236
IO58NB2F5	231
IO58PB2F5	232
IO59NB2F5	229
IO59PB2F5	230
IO61NB2F5	225
IO61PB2F5	226
IO62NB2F5	223
IO62PB2F5	224

CQ352	
AX500 Function	Pin Number
Bank 3	
IO63NB3F6	217
IO63PB3F6	218
IO64NB3F6	219
IO64PB3F6	220
IO65NB3F6	213
IO65PB3F6	214
IO67NB3F6	207
IO67PB3F6	208
IO68NB3F6	211
IO68PB3F6	212
IO69NB3F6	205
IO69PB3F6	206
IO71NB3F6	201
IO71PB3F6	202
IO73NB3F6	199
IO73PB3F6	200
IO75NB3F7	193
IO75PB3F7	194
IO76NB3F7	195
IO76PB3F7	196
IO77NB3F7	189
IO77PB3F7	190
IO79NB3F7	187
IO79PB3F7	188
IO80NB3F7	183
IO80PB3F7	184
IO81NB3F7	181
IO81PB3F7	182
IO83NB3F7	179
IO83PB3F7	180
Bank 4	
IO85NB4F8	172
IO85PB4F8	173
IO87NB4F8	170

CQ352	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282

CQ352	
AX2000 Function	Pin Number
IO71NB1F6	277
IO71PB1F6	278
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224

CQ352	
AX2000 Function	Pin Number
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170

CG624	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	F7
IO02NB0F0	G7
IO02PB0F0	G6
IO04NB0F0	E9
IO04PB0F0	D8
IO06NB0F0	G9
IO06PB0F0	G8
IO07PB0F0	B6
IO08NB0F0	F10
IO08PB0F0	F9
IO09PB0F0	C7
IO10NB0F0	H8
IO10PB0F0	H7
IO11NB0F0	D10
IO11PB0F0	D9
IO12NB0F1	B5
IO12PB0F1	B4
IO13NB0F1	A7
IO13PB0F1	A6
IO14NB0F1	C9
IO14PB0F1	C8
IO15PB0F1	B7
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	A9
IO17PB0F1	B9
IO18NB0F1	D12
IO18PB0F1	D11
IO20NB0F1	B11
IO20PB0F1	B10
IO21NB0F1	A11
IO21PB0F1	A10
IO22NB0F2	H10
IO22PB0F2	H9

CG624	
AX1000 Function	Pin Number
IO23NB0F2	E11
IO23PB0F2	F11
IO24NB0F2	D7
IO24PB0F2	E7
IO25PB0F2	B12
IO26NB0F2	H11
IO26PB0F2	G11
IO27NB0F2	C11
IO27PB0F2	B8
IO28NB0F2	J13
IO28PB0F2	K13
IO29NB0F2	J8
IO29PB0F2	J7
IO30NB0F2/HCLKAN	G13
IO30PB0F2/HCLKAP	G12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	C12
Bank 1	
IO32NB1F3/HCLKCN	G15
IO32PB1F3/HCLKCP	G14
IO33NB1F3/HCLKDN	B14
IO33PB1F3/HCLKDP	B13
IO34NB1F3	G16
IO34PB1F3	H16
IO35NB1F3	C17
IO35PB1F3	B18
IO36NB1F3	H18
IO36PB1F3	H15
IO37NB1F3	H13
IO38NB1F3	E15
IO38PB1F3	F15
IO39NB1F3	D14
IO39PB1F3	C14
IO40NB1F3	D16
IO40PB1F3	D15
IO41NB1F4	F16

CG624	
AX1000 Function	Pin Number
IO42NB1F4	G21
IO42PB1F4	G20
IO43NB1F4	A16
IO43PB1F4	A15
IO44NB1F4	A20
IO44PB1F4	A19
IO45NB1F4	B17
IO45PB1F4	B16
IO46NB1F4	G17
IO46PB1F4	H17
IO47NB1F4	A17
IO48NB1F4	C19
IO48PB1F4	C18
IO49NB1F4	B20
IO49PB1F4	B19
IO50NB1F4	H20
IO50PB1F4	H19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	C21
IO52PB1F4	C20
IO53NB1F4	B22
IO53PB1F4	B21
IO54NB1F5	J18
IO54PB1F5	J19
IO55NB1F5	D18
IO55PB1F5	D17
IO56NB1F5	F20
IO56PB1F5	F19
IO58NB1F5	E17
IO58PB1F5	F17
IO60NB1F5	D20
IO60PB1F5	D19
IO62NB1F5	E18
IO62PB1F5	F18
IO63NB1F5	G19

Revision	Changes	Page
Revision 10 (continued)	The "TRST" section was updated.	2-107
	The "Global Set Fuse" section was added.	2-109
	A footnote was added to "FG896" for the AX2000 regarding pins AB1, AE2, G1, and K2.	3-52
	Pinouts for the AX250, AX500, and AX1000 were added for "CQ352".	3-98
	Pinout for the AX1000 was added for "CG624".	3-115
Revision 9 (v2.1)	Table 2-79 was updated.	2-69
	The "Low Power Mode" section was updated.	2-106
Revision 8 (v2.0)	Table 1 has been updated.	i
	The "Ordering Information" section has been updated.	ii
	The "Device Resources" section has been updated.	ii
	The "Temperature Grade Offerings" section is new.	iii
	The "Speed Grade and Temperature Grade Matrix" section has been updated.	iii
	Table 2-9 has been updated.	2-12
	Table 2-10 has been updated.	2-12
	Table 2-1 has been updated.	2-1
	Table 2-2 has been updated.	2-1
	Table 2-3 has been updated.	2-2
	Table 2-4 has been updated.	2-3
	Table 2-5 has been updated.	2-4
	The "Power Estimation Example" section has been updated.	2-5
	The "Thermal Characteristics" section has been updated.	2-6
	The "Package Thermal Characteristics" section has been updated.	2-6
	The "Timing Characteristics" section has been updated.	2-7
	The "Pin Descriptions" section has been updated.	2-9
	Timing numbers have been updated from the "3.3 V LVTTL" section to the "Timing Characteristics" section. Many AC Loads were updated as well.	2-25 to 2-59
	Timing characteristics for the "Hardwired Clocks" and "Routed Clocks" sections were updated.	2-66, 2-68
	Table 2-89 to Table 2-92 and Table 2-98 to Table 2-99 were updated.	2-90 to 2-93, 2-102 to 2-103
	The following sections were updated: "Low Power Mode", "Interface", "Data Registers (DRs)", "Security", "Silicon Explorer II Probe Interface", and "Programming"	2-106 to 2-110
	In the "PQ208" (AX500) section, pins 2, 52, and 156 changed from V_{CCDA} to V_{CCA}. For pins 170 and 171, the I/O names refer to pair 23 instead of 24.	3-84