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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	684
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	1152-BGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax2000-2fgg1152i

Figure 1-2 • **Axcelerator Family Interconnect Elements**

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

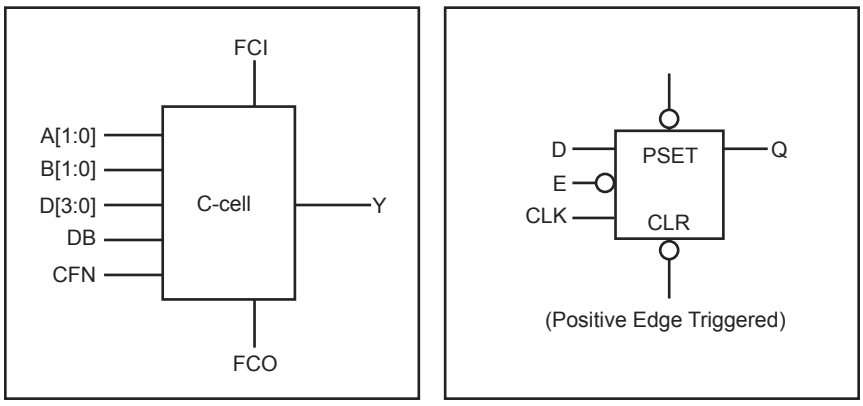
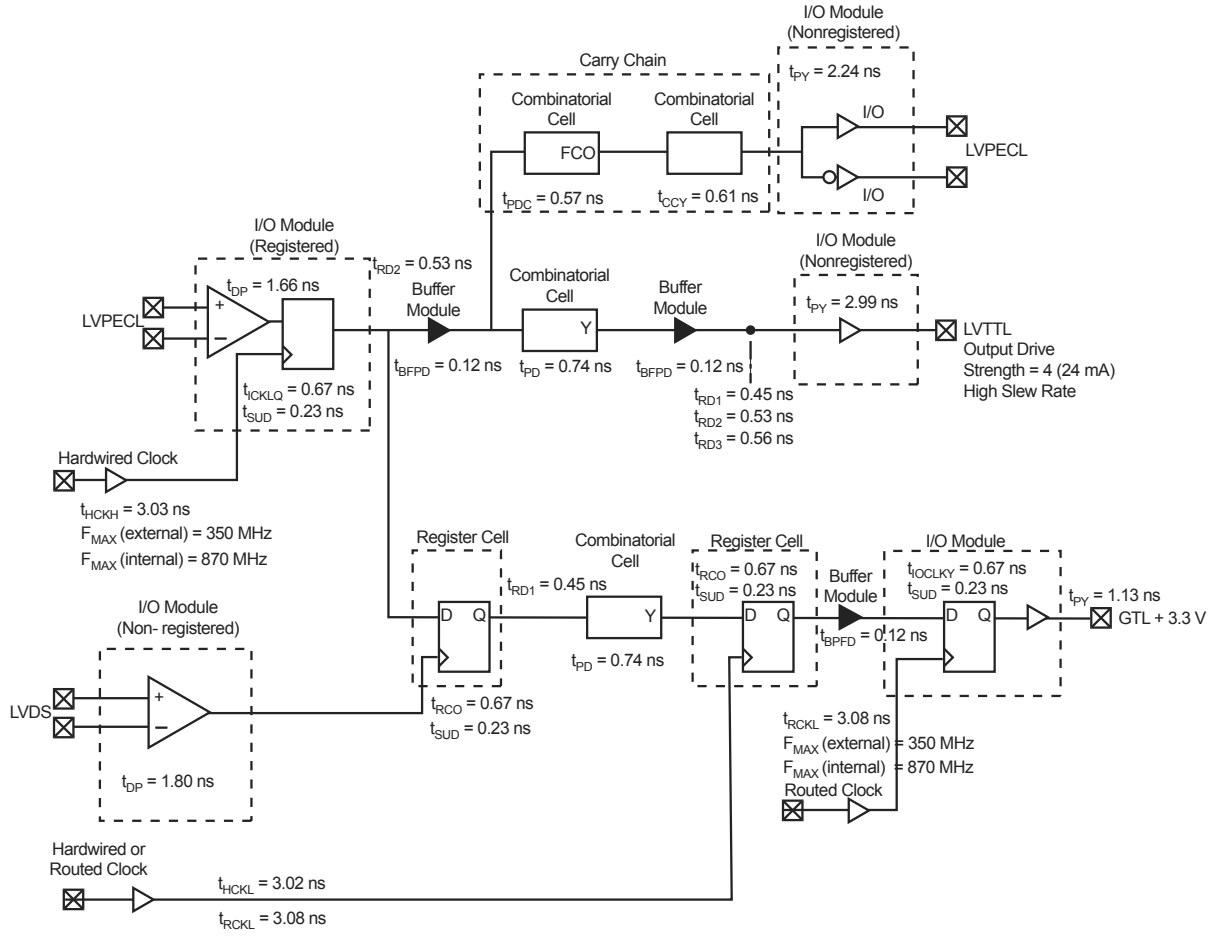


Figure 1-3 • **AX C-Cell and R-Cell**

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

Timing Model



Note: Worst case timing data for the AX1000, –2 speed grade

Figure 2-1 • **Worst Case Timing Data**

Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$= (t_{DP} + t_{RD2} + t_{SUD}) – t_{HCKL}$

$= (1.72 + 0.53 + 0.23) – 3.02 = –0.54$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{HCKL} + t_{RCO} + t_{RD1} + t_{PY}$

$= 3.02 + 0.67 + 0.45 + 2.99 = 7.13$ ns

Routed Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$= (t_{DP} + t_{RD2} + t_{SUD}) – t_{RCKH}$

$= (1.72 + 0.53 + 0.23) – 3.13 = –0.65$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$

$= 3.13 + 0.67 + 0.45 + 3.03 = 7.24$ ns

I/O Specifications

Pin Descriptions

Supply Pins

GND **Ground**

Low supply voltage.

VCCA **Supply Voltage**

Supply voltage for array (1.5V). See "Operating Conditions" on page 2-1 for more information.

VCCIBx **Supply Voltage**

Supply voltage for I/Os. Bx is the I/O Bank ID – 0 to 7. See "Operating Conditions" on page 2-1 for more information.

VCCDA **Supply Voltage**

Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. See "Operating Conditions" on page 2-1 for more information. VCCDA should be tied to 3.3V.

VCCPLA/B/C/D/E/F/G/H **Supply Voltage**

PLL analog power supply (1.5V) for internal PLL. There are eight in each device. VCCPLA supports the PLL associated with global resource HCLKA, VCCPLB supports the PLL associated with global resource HCLKB, etc. The PLL analog power supply pins should be connected to 1.5V whether PLL is used or not.

VCOMPLA/B/C/D/E/F/G/H **Supply Voltage**

Compensation reference signals for internal PLL. There are eight in each device. **VCOMPLA** supports the PLL associated with global resource HCLKA, VCOMPLE supports the PLL associated with global resource CLKE, etc. (see Figure 2-2 on page 2-9 for correct external connection to the supply). The VCOMPLX pins should be left floating if PLL is not used.

VPUMP **Supply Voltage (External Pump)**

In the low power mode, VPUMP will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on VPUMP reaches VIH[1]. In normal device operation, when using the internal charge pump, VPUMP should be tied to GND.

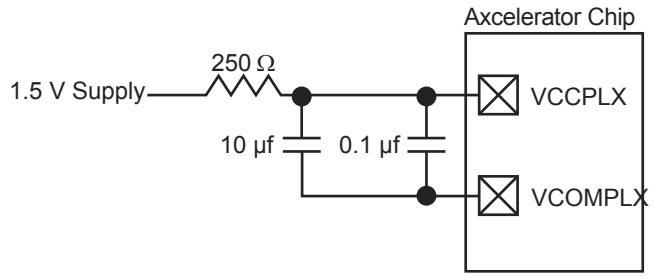


Figure 2-2 • **VCCPLX and VCOMPLX Power Supply Connect**

1. *When $V_{PUMP} = V_{IH}$, it shuts off the internal charge pump. See* ***"Low Power Mode" on page 2-106****.*

Table 2-8 • **I/O Standards Supported by the Axcelerator Family**

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVCMOS 2.5 V	2.5	N/A	N/A
LVCMOS 1.8 V	1.8	N/A	N/A
LVCMOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

*Note: *2.5 V GTL+ is not supported across the full military temperature range.*

Table 2-9 • **Supply Voltages**

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5 V	1.5 V	3.3 V	1.5 V
1.5 V	1.8 V	3.3 V	1.8 V
1.5 V	2.5 V	3.3 V	2.5 V
1.5 V	3.3 V	3.3 V	3.3 V

Table 2-10 • **I/O Features Comparison**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1, 2]	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled[3]
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled[4]

Notes:

1. *Can be implemented with an IDT bus switch.*
2. *Can be implemented with an external resistor.*
3. *The OE input of the output buffer must be deasserted permanently (handled by software).*
4. *The OE input of the output buffer must be asserted permanently (handled by software).*

Class II

Table 2-53 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16

AC Loadings

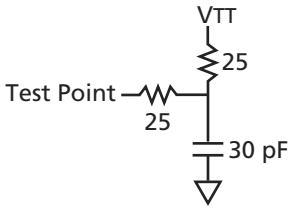


Figure 2-24 • AC Test Loads

Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

*Note: * Measuring Point = VTRIP*

Timing Characteristics

Table 2-55 • 3.3 V SSTL3 Class II I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V SSTL3 Class II I/O Module Timing								
t_{DP}	Input Buffer		1.85		2.10		2.47	ns
t_{PY}	Output Buffer		2.17		2.47		2.91	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Routing Specifications

Routing Resources

The routing structure found in Axcelerator devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the AX architecture: DirectConnect, CarryConnect, FastConnect, and Vertical and Horizontal Routing.

DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 2-35). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

Figure 2-35 • **DirectConnect and CarryConnect**

CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (Figure 2-35). The FCO output of the right C-cell of a two-C-cell Cluster drives the FCI input of the left C-cell in the two-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two-C-cell cluster to the FCI of the two-C-cell cluster immediately below it (see the "Carry-Chain Logic" section on page 2-56 for more information).

FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 2-36 on page 2-62). FastConnects provide a maximum delay of 0.3 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

***Table 2-67* • AX500 Predicted Routing Delays**
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

***Table 2-68* • AX1000 Predicted Routing Delays**
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.45	0.51	0.60	ns
t_{RD2}	Routing delay for FO2	0.53	0.60	0.71	ns
t_{RD3}	Routing delay for FO3	0.56	0.63	0.74	ns
t_{RD4}	Routing delay for FO4	0.63	0.71	0.84	ns
t_{RD5}	Routing delay for FO5	0.73	0.82	0.97	ns
t_{RD6}	Routing delay for FO6	0.99	1.13	1.32	ns
t_{RD7}	Routing delay for FO7	1.02	1.15	1.36	ns
t_{RD8}	Routing delay for FO8	1.48	1.68	1.97	ns
t_{RD16}	Routing delay for FO16	2.57	2.91	3.42	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

***Table 2-72* • AX500 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		2.35		2.68		3.15	ns
t_{HCKH}	Input High to Low		2.44		2.79		3.27	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-73* • AX1000 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-74* • AX2000 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

Implementation Example:

Figure 2-47 shows a complex clock distribution example. The reference clock (RefCLK) of PLLE is being sourced from non-clock signal pins (INBUF to PLLINT). The CLK1 output of PLLE is being fed to the RefCLK input of PLLF. The CLK2 output of PLLE is driving logic (via PLLOUT). In turn, this logic is driving the global resource CLKE. PLLF is driving both CLKF and CLKG global resources.

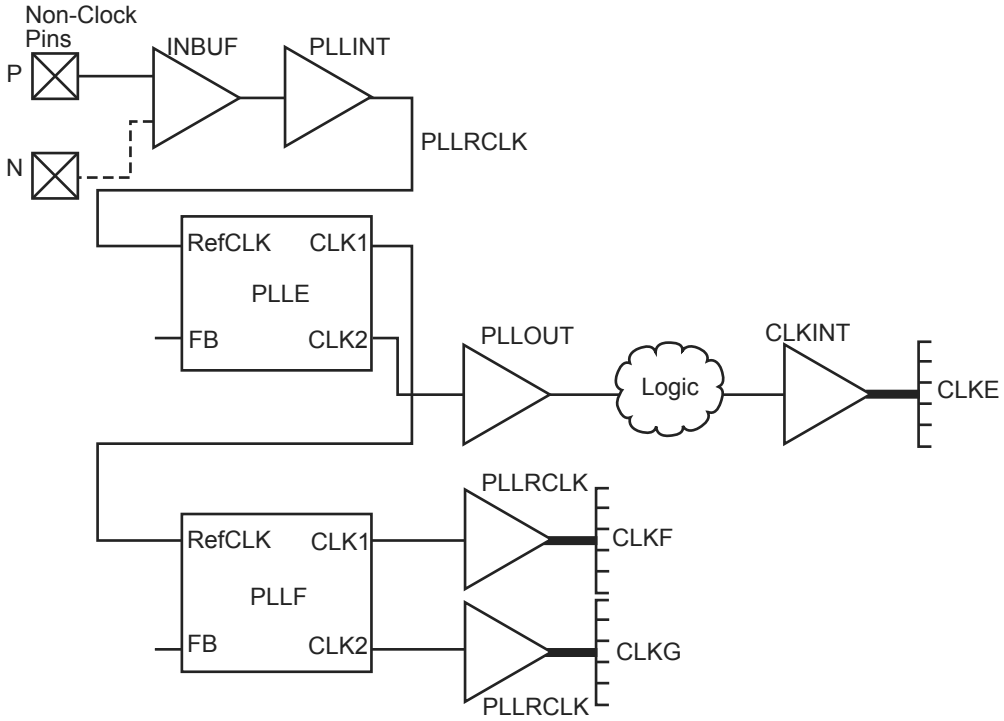


Figure 2-47 • **Complex Clock Distribution Example**

single-ended, or voltage-referenced standard. The [H]CLKxN pad can only be used as a differential pair with [H]CLKxP.

The block marked “/i Delay Match” is a fixed delay equal to that of the i divider. The “/j Delay Match” block has the same function as its j divider counterpart.

Functional Description

Figure 2-48 on page 2-75 illustrates a block diagram of the PLL. The PLL contains two dividers, i and j, that allow frequency scaling of the clock signal:

- The i divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64, and the resultant frequency is available at the output of the PLL block.
- The j divider divides the PLL output by integer factors ranging from 1 to 64, and the divided clock is available at CLK1.
- The two dividers together can implement any combination of multiplication and division up to a maximum frequency of 1 GHz on CLK1. Both the CLK1 and CLK2 outputs have a fixed 50/50 duty cycle.
- The output frequencies of the two clocks are given by the following formulas (f_{REF} is the reference clock frequency):

$$f_{CLK1} = f_{REF} * (DividerI) / (DividerJ)$$

EQ 4

$$f_{CLK2} = f_{REF} * (DividerI)$$

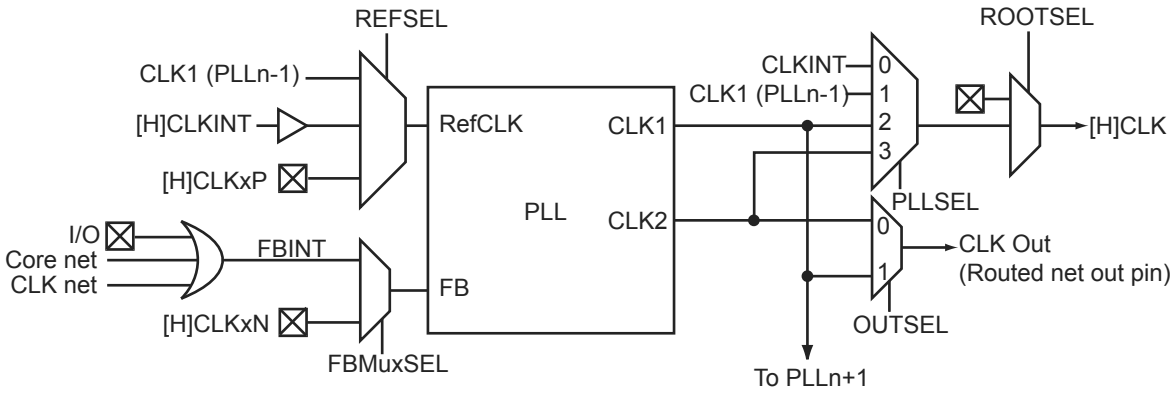
EQ 5

- CLK2 provides the PLL output directly—without division

The input and output frequency ranges are selected by LowFreq and Osc(2:0), respectively. These functions and their possible values are detailed in Table 2-80 on page 2-77.

The delay lines shown in Figure 2-48 on page 2-75 are programmable. The feedback clock path can be delayed (using the five DelayLine bits) relative to the reference clock (or vice versa) by up to 3.75 ns in increments of 250 ps. Table 2-80 on page 2-77 describes the usage of these bits. The delay increments are independent of frequency, so this results in phase changes that vary with frequency. The delay value is highly dependent on V_{CC} and the speed grade.

Figure 2-49 is a logical diagram of the various control signals to the PLL and shows how the PLL interfaces with the global and routing networks of the FPGA. Note that not all signals are user-accessible. These non-user-accessible signals are used by the place-and-route tool to control the configuration of the PLL. The user gains access to these control signals either based upon the connections built in the user's design or through the special macros (Table 2-84 on page 2-81) inserted into the design. For example, connecting the macro PLLOUT to CLK2 will control the OUTSEL signal.



Note: Not all signals are available to the user.

Figure 2-49 • **PLL Logical Interface**

Note that the RAM blocks employ little-endian byte order for read and write operations.

***Table 2-88* • RAM Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

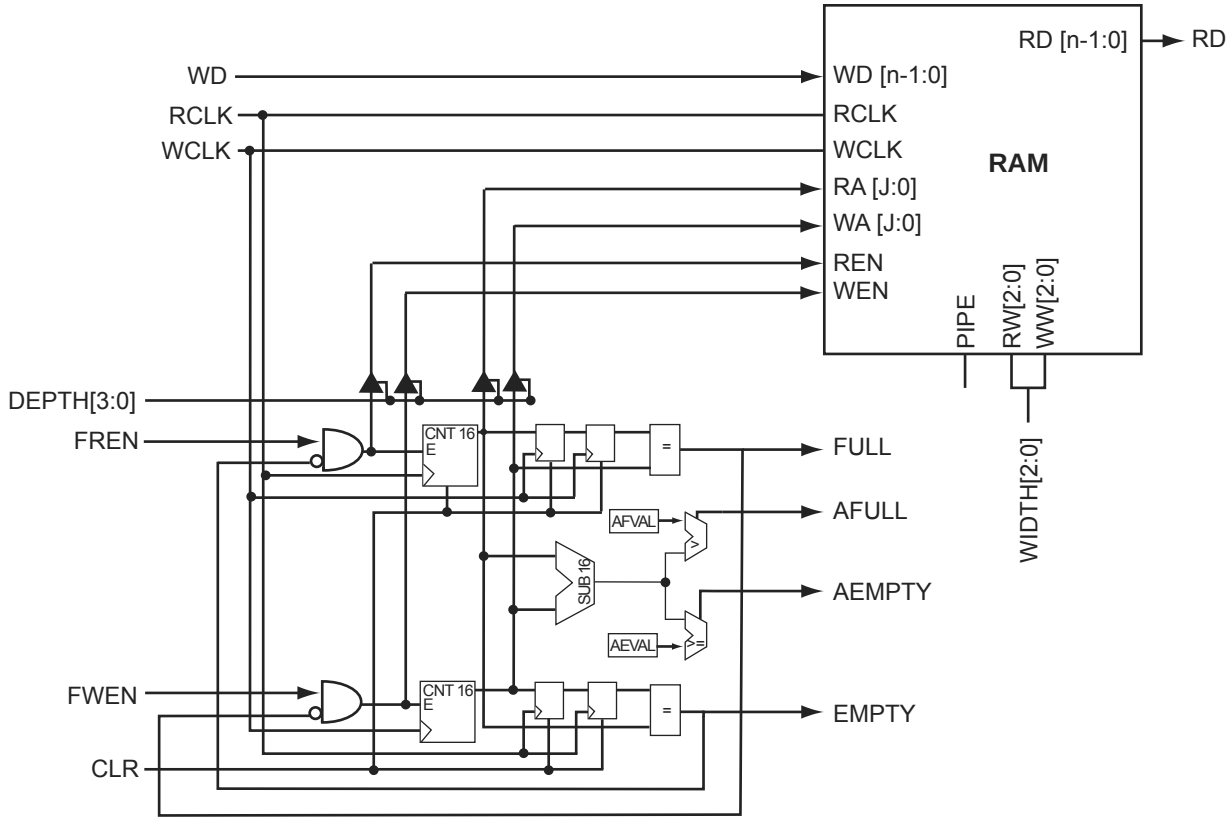


Figure 2-61 • **Axcelerator RAM with Embedded FIFO Controller**

FG484	
AX1000 Function	**Pin Number**
IO87PB2F8	H20
IO88NB2F8	L18
IO88PB2F8	K18
IO89NB2F8	K19
IO89PB2F8	J19
IO90NB2F8	J21
IO90PB2F8	H21
IO91NB2F8	J22
IO91PB2F8	H22
IO93NB2F8	K21
IO93PB2F8	K22
IO94NB2F8	L20
IO94PB2F8	K20
IO95NB2F8	M21
IO95PB2F8	L21
Bank 3	
IO96NB3F9	N16
IO96PB3F9	M16
IO97NB3F9	M19
IO97PB3F9	L19
IO98NB3F9	P22
IO98PB3F9	N22
IO99NB3F9	N20
IO99PB3F9	M20
IO100NB3F9	N17
IO100PB3F9	M17
IO101NB3F9	P21
IO101PB3F9	N21
IO103NB3F9	R20
IO103PB3F9	P20
IO104NB3F9	N18
IO104PB3F9	N19
IO105NB3F9	T22
IO105PB3F9	R22
IO106NB3F9	R17

FG484	
AX1000 Function	**Pin Number**
IO106PB3F9	P17
IO107NB3F10	T21
IO107PB3F10	R21
IO110NB3F10	V22
IO110PB3F10	U22
IO113NB3F10	V21
IO113PB3F10	U21
IO114NB3F10	P18
IO114PB3F10	P19
IO116PB3F10	R19
IO117NB3F10	U20
IO117PB3F10	T20
IO118NB3F11	T18
IO118PB3F11	R18
IO121NB3F11	U19
IO121PB3F11	T19
IO124NB3F11	R16
IO124PB3F11	P16
IO127NB3F11	W21
IO127PB3F11	W22
Bank 4	
IO129PB4F12	AB17
IO132NB4F12	Y19
IO132PB4F12	W18
IO133NB4F12	W17
IO133PB4F12	V17
IO135NB4F12	T15
IO135PB4F12	T16
IO138NB4F12	Y17
IO138PB4F12	Y18
IO139NB4F13	V15
IO139PB4F13	V16
IO140NB4F13	U18
IO140PB4F13	V19
IO142NB4F13	W20

FG484	
AX1000 Function	**Pin Number**
IO142PB4F13	V20
IO143NB4F13	W15
IO143PB4F13	W16
IO144NB4F13	AA18
IO144PB4F13	AA19
IO145NB4F13	U14
IO145PB4F13	U15
IO146NB4F13	Y15
IO146PB4F13	Y16
IO147NB4F13	AB18
IO147PB4F13	AB19
IO149NB4F13	Y14
IO149PB4F13	W14
IO150NB4F13	AA16
IO150PB4F13	AA17
IO152NB4F14	AA14
IO152PB4F14	AA15
IO154NB4F14	AB14
IO154PB4F14	AB15
IO155NB4F14	AA13
IO155PB4F14	AB13
IO158NB4F14	Y12
IO158PB4F14	Y13
IO159NB4F14/CLKEN	V12
IO159PB4F14/CLKEP	V13
IO160NB4F14/CLKFN	W11
IO160PB4F14/CLKFP	W12
Bank 5	
IO161NB5F15/CLKGN	U10
IO161PB5F15/CLKGP	U11
IO162NB5F15/CLKHN	V9
IO162PB5F15/CLKHP	V10
IO163NB5F15	Y10
IO163PB5F15	Y11
IO167NB5F15	AA11

FG676	
AX500 Function	Pin Number
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A11
NC	A21

FG676	
AX500 Function	Pin Number
NC	A22
NC	A24
NC	A25
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
NC	AC25
NC	AD1
NC	AD11
NC	AD16
NC	AD25
NC	AE1
NC	AF2
NC	AF25
NC	B11
NC	B24
NC	B4
NC	C16

FG676	
AX500 Function	Pin Number
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
NC	G21
NC	G22
NC	H21
NC	H22
NC	H23
NC	H5
NC	H6

FG676	
AX500 Function	**Pin Number**
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8

FG676	
AX500 Function	**Pin Number**
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

FG896	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8

FG896	
AX2000 Function	Pin Number
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15

FG896	
AX2000 Function	Pin Number
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20

PQ208	
AX500 Function	**Pin Number**
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
V_{CCDA}	1
V_{CCDA}	26
V_{CCDA}	53
V_{CCDA}	63
V_{CCDA}	78
V_{CCDA}	95
V_{CCDA}	105
V_{CCDA}	130
V_{CCDA}	157
V_{CCDA}	167
V_{CCDA}	182
V_{CCDA}	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX500 Function	**Pin Number**
GND	94
GND	99
GND	113
GND	119
GND	125
GND	143
GND	136
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX500 Function	**Pin Number**
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	200
VCCIB0	193
VCCIB1	172
VCCIB1	163
VCCIB2	149
VCCIB2	135
VCCIB3	124
VCCIB3	112
VCCIB4	98
VCCIB4	89
VCCIB5	68
VCCIB5	58
VCCIB6	45
VCCIB6	31
VCCIB7	20
VCCIB7	8
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CG624	
AX1000 Function	**Pin Number**
VCCA	U17
VCCA	U9
VCCA	Y4
VCCDA	A12
VCCDA	AA13
VCCDA	AA15
VCCDA	AA7
VCCDA	AC11
VCCDA	AD11
VCCDA	AE17
VCCDA	B15
VCCDA	C15
VCCDA	C6
VCCDA	D13
VCCDA	E13
VCCDA	E19
VCCDA	G5
VCCDA	N21
VCCDA	N5
VCCDA	W21
VCCIB0	A3
VCCIB0	B3
VCCIB0	C4
VCCIB0	D5
VCCIB0	J10
VCCIB0	J11
VCCIB0	K12
VCCIB1	A23
VCCIB1	B23
VCCIB1	C22
VCCIB1	D21
VCCIB1	J15
VCCIB1	J16
VCCIB1	K14
VCCIB2	C24
VCCIB2	C25

CG624	
AX1000 Function	**Pin Number**
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3

CG624	
AX1000 Function	**Pin Number**
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

CG624	
AX2000 Function	**Pin Number**
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20*
IO85PB1F7	D19*
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17*
IO89PB2F8	G22*
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23*
IO107PB2F10	N16*
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*