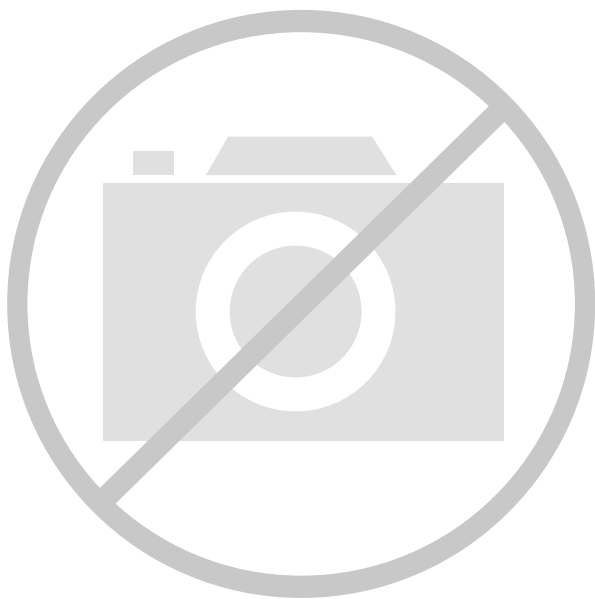




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	586
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-2fgg896

Two C-cells, a single R-cell, two Transmit (TX), and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

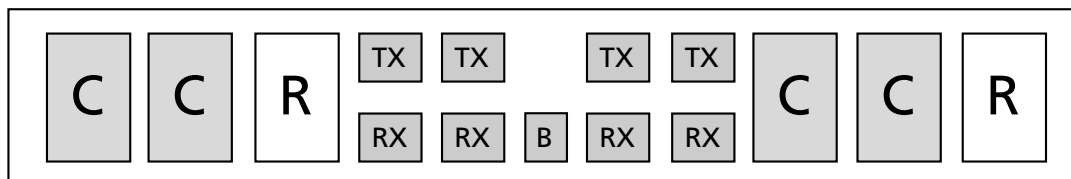


Figure 1-4 • AX SuperCluster

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

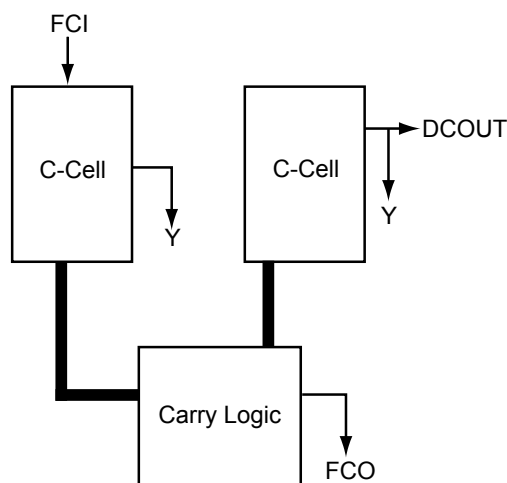


Figure 1-5 • AX 2-Bit Carry Logic

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the AX1000 is composed of a 3x3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1). Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the AX250).

Table 1-1 • Number of Core Tiles per Device

Device	Number of Core Tiles
AX125	1 regular tile
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II, Microsemi's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-109).

Summary

Microsemi's Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an Axcelerator design yet still achieve high performance and efficient device utilization.

Related Documents

Application Notes

Simultaneous Switching Noise and Signal Integrity

http://www.microsemi.com/soc/documents/SSN_AN.pdf

Axcelerator Family PLL and Clock Management

http://www.microsemi.com/soc/documents/AX_PLL_AN.pdf

Implementation of Security in Actel Antifuse FPGAs

http://www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

User's Guides and Manuals

Antifuse Macro Library Guide

http://www.microsemi.com/soc/documents/libguide_UG.pdf

SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder

http://www.microsemi.com/soc/documents/genguide_ug.pdf

Silicon Sculptor II User's Guide

http://www.microsemi.com/soc/documents/silisculptII_sculpt3_ug.pdf

White Paper

Design Security in Nonvolatile Flash and Antifuse FPGAs

http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

Understanding Actel Antifuse Device Security

http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

Miscellaneous

Libero IDE flow diagram

<http://www.microsemi.com/soc/products/tools/libero/flow.html>

I/O Module Timing Characteristics

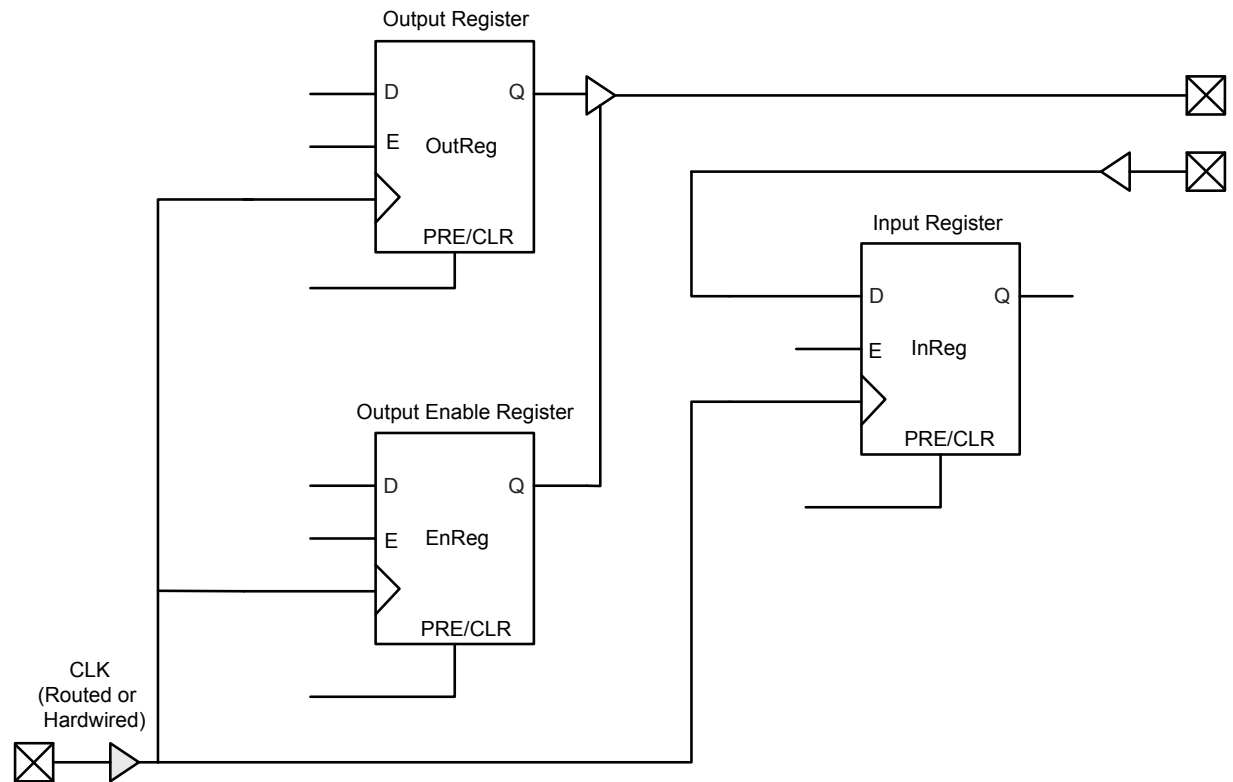


Figure 2-11 • Timing Model

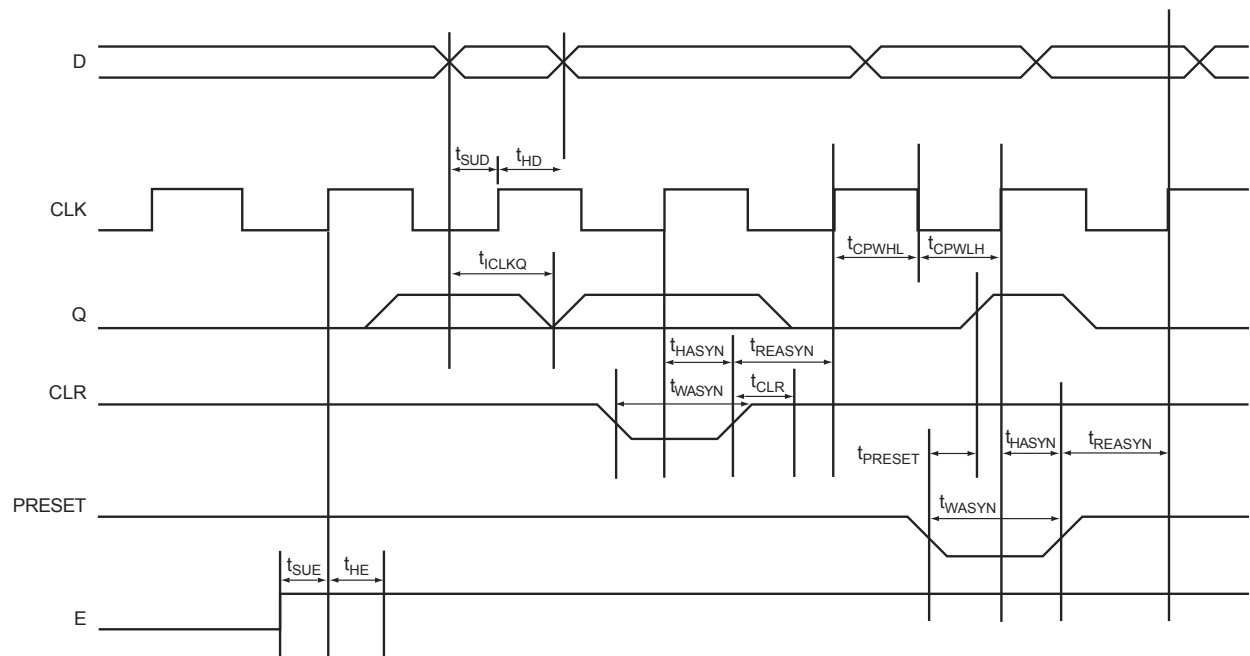


Figure 2-12 • Input Register Timing Characteristics

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		3.30		3.76		4.42	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.74		4.26		5.00	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.06		3.49		4.10	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.29		2.30		2.31	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 4 (24mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		2.99		3.41		4.01	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.49		2.51		2.51	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.59		2.95		3.46	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.56		4.06		4.77	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-28 • 1.8V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.7 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS18 Output Module Timing								
t _{DP}	Input Buffer		3.26		3.71		4.37	ns
t _{PY}	Output Buffer		4.55		5.18		6.09	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.82		2.83		2.84	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.43		3.45		3.46	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.01		6.85		8.05	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.73		7.67		9.01	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Special PLL Macros

Table 2-84 shows the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

Table 2-84 • PLL Special Macros

Macro Name	Usage
PLLINT	Connects RefCLK to a regular routed net or a pad.
PLLCLK	Connects CLK1 or CLK2 to the CLK network.
PLHCLK	Connects CLK1 or CLK2 to the HCLK network.
PLLOUT	Connects CLK1 or CLK2 to a regular routed net.

Table 2-85 • Electrical Specifications

Parameter	Value	Notes
Frequency Ranges		
Reference Frequency (min.)	14 MHz	Lowest input frequency
Reference Frequency (max.)	200 MHz	Highest input frequency
OSC Frequency (min.)	20 MHz	Lowest output frequency
OSC Frequency (max.)	1 GHz	Highest output frequency
Jitter		
Long-Term Jitter (max.)	1%	Percentage of period, low reference clock frequencies
Long-Term Jitter (max.)	100ps	High reference clock frequencies
Short-Term Jitter (max.)	50ps+1%	Percentage of output frequency
Acquisition Time (lock) from Cold Start		
Acquisition Time (max.)*	400 cycles	Period of low reference clock frequencies
Acquisition Time (max.)*	1.5 μ s	High reference clock frequencies
Power Consumption		
Analog Supply Current (low freq.)	200 μ A	Current at minimum oscillator frequency
Analog Supply Current (high freq.)	200 μ A	Frequency-dependent current
Digital Supply Current (low freq.)	0.5 μ A/MHz	Current at maximum oscillator frequency, unloaded
Digital Supply Current (high freq.)	1 μ A/MHz	Frequency-dependent current
Duty Cycle		
Minimum Output Duty Cycle	45%	
Maximum Output Duty Cycle	55%	

Note: *The lock bit remains Low until RefCLK reaches the minimum input frequency.

Table 2-91 • Four RAM Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t _{WDASU}	Write Data Setup vs. WCLK		2.37		2.70		3.17	ns
t _{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WADSU}	Write Address Setup vs. WCLK		2.37		2.70		3.17	ns
t _{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WENSU}	Write Enable Setup vs. WCLK		2.37		2.70		3.17	ns
t _{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t _{WCLK}	WCLK Minimum Low Pulse Width	2.51		2.51		2.51		ns
t _{WCKP}	WCLK Minimum Period	3.26		3.26		3.26		ns
Read Mode								
t _{RADSU}	Read Address Setup vs. RCLK		3.08		3.51		4.13	ns
t _{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RENSU}	Read Enable Setup vs. RCLK		3.08		3.51		4.13	ns
t _{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
t _{RCK2RD2}	RCLK-To-OUT (Non-Pipelined)		2.83		3.23		3.79	ns
t _{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t _{RCLKL}	RCLK Minimum Low Pulse Width	2.96		2.96		2.96		ns
t _{RCKP}	RCLK Minimum Period	3.69		3.69		3.69		ns

Note: Timing data for these four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111". If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:
The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microsemi identity, part number, and version number in a specific JTAG format.
2. USERCODE:
The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.
3. Boundary-Scan Register (BSR):
Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.
4. Bypass Register (BYR):
This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

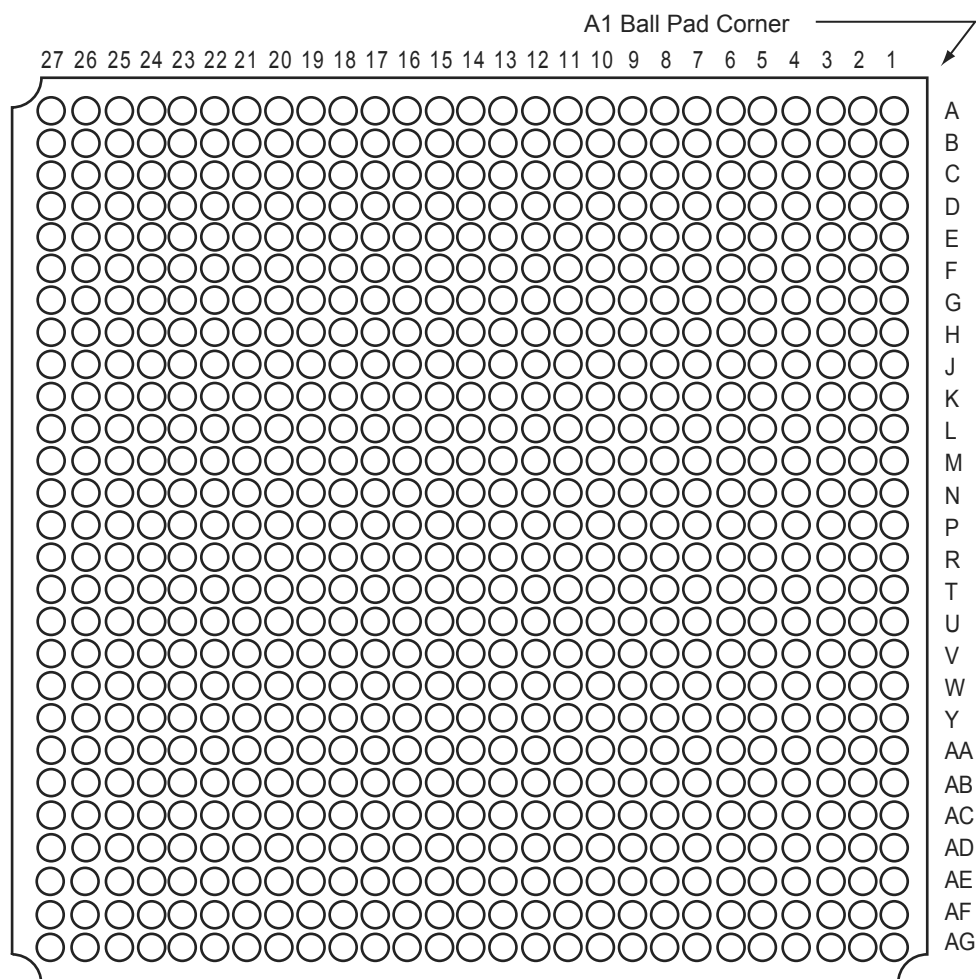
Special Fuses

Security

Microsemi antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden

3 – Package Pin Assignments

BG729



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG484	
AX500 Function	Pin Number
IO54PB2F5	H22
IO55NB2F5	L17
IO55PB2F5	K17
IO56NB2F5	K21
IO56PB2F5	K22
IO58NB2F5	L20
IO58PB2F5	K20
IO59NB2F5	L18
IO59PB2F5	K18
IO60NB2F5	M21
IO60PB2F5	L21
IO61NB2F5	L16
IO61PB2F5	K16
IO62NB2F5	M19
IO62PB2F5	L19
Bank 3	
IO63NB3F6	N16
IO63PB3F6	M16
IO64NB3F6	P22
IO64PB3F6	N22
IO65NB3F6	N20
IO65PB3F6	M20
IO66NB3F6	P21
IO66PB3F6	N21
IO67NB3F6	N18
IO67PB3F6	N19
IO68NB3F6	T22
IO68PB3F6	R22
IO69NB3F6	N17
IO69PB3F6	M17
IO70NB3F6	T21
IO70PB3F6	R21
IO71NB3F6	P18
IO71PB3F6	P19
IO72NB3F6	R20

FG484	
AX500 Function	Pin Number
IO72PB3F6	P20
IO73PB3F6	R19
IO74NB3F7	V21
IO74PB3F7	U21
IO75NB3F7	V22
IO75PB3F7	U22
IO76NB3F7	U20
IO76PB3F7	T20
IO77NB3F7	R17
IO77PB3F7	P17
IO78NB3F7	W21
IO78PB3F7	W22
IO79NB3F7	T18
IO79PB3F7	R18
IO80NB3F7	W20
IO80PB3F7	V20
IO81NB3F7	U19
IO81PB3F7	T19
IO82NB3F7	U18
IO82PB3F7	V19
IO83NB3F7	R16
IO83PB3F7	P16
Bank 4	
IO84NB4F8	AB18
IO84PB4F8	AB19
IO85NB4F8	T15
IO85PB4F8	T16
IO86NB4F8	AA18
IO86PB4F8	AA19
IO87NB4F8	W17
IO87PB4F8	V17
IO88NB4F8	Y19
IO88PB4F8	W18
IO89NB4F8	U14
IO89PB4F8	U15

FG484	
AX500 Function	Pin Number
IO90NB4F8	Y17
IO90PB4F8	Y18
IO91NB4F8	V15
IO91PB4F8	V16
IO92PB4F8	AB17
IO93NB4F8	Y15
IO93PB4F8	Y16
IO94NB4F9	AA16
IO94PB4F9	AA17
IO95NB4F9	AB14
IO95PB4F9	AB15
IO96NB4F9	W15
IO96PB4F9	W16
IO97NB4F9	AA13
IO97PB4F9	AB13
IO98NB4F9	AA14
IO98PB4F9	AA15
IO100NB4F9	Y14
IO100PB4F9	W14
IO101NB4F9	Y12
IO101PB4F9	Y13
IO102NB4F9	AA11
IO102PB4F9	AA12
IO103NB4F9/CLKEN	V12
IO103PB4F9/CLKEP	V13
IO104NB4F9/CLKFN	W11
IO104PB4F9/CLKFP	W12
Bank 5	
IO105NB5F10/CLKGN	U10
IO105PB5F10/CLKGP	U11
IO106NB5F10/CLKHN	V9
IO106PB5F10/CLKHP	V10
IO107NB5F10	Y10
IO107PB5F10	Y11
IO108NB5F10	AA9

FG676	
AX1000 Function	Pin Number
IO129PB4F12	AA21
IO131NB4F12	AD22
IO131PB4F12	AD23
IO132NB4F12	AE23
IO132PB4F12	AE24
IO133NB4F12	AB20
IO133PB4F12	AA20
IO134NB4F12	AC21
IO134PB4F12	AC22
IO135NB4F12	AF22
IO135PB4F12	AF23
IO137NB4F12	AB19
IO137PB4F12	AA19
IO139NB4F13	AC19
IO139PB4F13	AC20
IO140NB4F13	AE21
IO140PB4F13	AE22
IO141NB4F13	AD20
IO141PB4F13	AD21
IO143NB4F13	AB17
IO143PB4F13	AB18
IO144NB4F13	AE19
IO144PB4F13	AE20
IO145NB4F13	AC17
IO145PB4F13	AC18
IO146NB4F13	AD18
IO146PB4F13	AD19
IO147NB4F13	AA17
IO147PB4F13	AA18
IO148NB4F13	AF20
IO148PB4F13	AF21
IO149NB4F13	AA16
IO149PB4F13	Y16
IO151NB4F13	AC16
IO151PB4F13	AB16
IO153NB4F14	AE17

FG676	
AX1000 Function	Pin Number
IO153PB4F14	AE18
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AA15
IO155PB4F14	Y15
IO157NB4F14	AC15
IO157PB4F14	AB15
IO159NB4F14/CLKEN	AE16
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AE14
IO160PB4F14/CLKFP	AE15
Bank 5	
IO161NB5F15/CLKGN	AE12
IO161PB5F15/CLKGP	AE13
IO162NB5F15/CLKHN	AE11
IO162PB5F15/CLKHP	AF11
IO163NB5F15	AC12
IO163PB5F15	AB12
IO165NB5F15	Y12
IO165PB5F15	AA13
IO167NB5F15	Y11
IO167PB5F15	AA12
IO168NB5F15	AF9
IO168PB5F15	AF10
IO169NB5F15	AB11
IO169PB5F15	AA11
IO171NB5F16	AE9
IO171PB5F16	AE10
IO173NB5F16	AC10
IO173PB5F16	AC11
IO174NB5F16	AE7
IO174PB5F16	AE8
IO175NB5F16	AC9
IO175PB5F16	AD9
IO176NB5F16	AF6
IO176PB5F16	AF7

FG676	
AX1000 Function	Pin Number
IO177NB5F16	AA10
IO177PB5F16	AB10
IO179NB5F16	AD7
IO179PB5F16	AD8
IO180NB5F16	AC7
IO180PB5F16	AC8
IO181NB5F17	AA9
IO181PB5F17	AB9
IO183NB5F17	AD6
IO183PB5F17	AE6
IO184NB5F17	AE5
IO184PB5F17	AF5
IO185NB5F17	AA8
IO185PB5F17	AB8
IO187NB5F17	AC5
IO187PB5F17	AC6
IO188NB5F17	AD4
IO188PB5F17	AD5
IO189NB5F17	AB6
IO189PB5F17	AB7
IO190NB5F17	AF4
IO190PB5F17	AE4
IO191NB5F17	AE3
IO191PB5F17	AF3
IO192NB5F17	AA6
IO192PB5F17	AA7
Bank 6	
IO193NB6F18	Y5
IO193PB6F18	AA5
IO194NB6F18	AB3
IO194PB6F18	AC3
IO195NB6F18	Y4
IO195PB6F18	AA4
IO196NB6F18	AC2
IO196PB6F18	AD2
IO197NB6F18	W6

FG676	
AX1000 Function	Pin Number
IO197PB6F18	Y6
IO198NB6F18	AD1
IO198PB6F18	AE1
IO199NB6F18	AA2
IO199PB6F18	AB2
IO200NB6F18	Y3
IO200PB6F18	AA3
IO201NB6F18	V5
IO201PB6F18	W5
IO202NB6F18	AB1
IO202PB6F18	AC1
IO203NB6F19	V4
IO203PB6F19	W4
IO204NB6F19	V3
IO204PB6F19	W3
IO205NB6F19	U6
IO205PB6F19	V6
IO206NB6F19	W2
IO206PB6F19	Y2
IO207NB6F19	U4
IO207PB6F19	U5
IO208NB6F19	Y1
IO208PB6F19	AA1
IO209NB6F19	T6
IO209PB6F19	T7
IO211NB6F19	T3
IO211PB6F19	U3
IO212NB6F19	V1
IO212PB6F19	V2
IO213NB6F19	T5
IO213PB6F19	T4
IO214NB6F20	U1
IO214PB6F20	U2
IO215NB6F20	R6
IO215PB6F20	R7
IO217NB6F20	R5

FG676	
AX1000 Function	Pin Number
IO217PB6F20	R4
IO218NB6F20	R2
IO218PB6F20	T2
IO219NB6F20	P3
IO219PB6F20	R3
IO220NB6F20	R1
IO220PB6F20	T1
IO221NB6F20	P6
IO221PB6F20	P7
IO223NB6F20	P5
IO223PB6F20	P4
Bank 7	
IO225NB7F21	N5
IO225PB7F21	N4
IO226NB7F21	N2
IO226PB7F21	N3
IO227NB7F21	N6
IO227PB7F21	N7
IO229NB7F21	M7
IO229PB7F21	M6
IO231NB7F21	M5
IO231PB7F21	M4
IO232NB7F21	L1
IO232PB7F21	M1
IO233NB7F21	M2
IO233PB7F21	M3
IO235NB7F21	K2
IO235PB7F21	L2
IO236NB7F22	L5
IO236PB7F22	L4
IO237NB7F22	L6
IO237PB7F22	L7
IO238NB7F22	K3
IO238PB7F22	L3
IO240NB7F22	J1
IO240PB7F22	K1

FG676	
AX1000 Function	Pin Number
IO241NB7F22	K6
IO241PB7F22	K5
IO242NB7F22	H2
IO242PB7F22	J2
IO243NB7F22	J4
IO243PB7F22	K4
IO244NB7F22	H3
IO244PB7F22	J3
IO245NB7F22	G2
IO245PB7F22	G1
IO247NB7F23	J6
IO247PB7F23	J5
IO248NB7F23	E1
IO248PB7F23	F1
IO249NB7F23	E2
IO249PB7F23	F2
IO250NB7F23	G4
IO250PB7F23	H4
IO251NB7F23	F3
IO251PB7F23	G3
IO253NB7F23	H6
IO253PB7F23	H5
IO254NB7F23	D2
IO254PB7F23	D1
IO255NB7F23	E4
IO255PB7F23	F4
IO256NB7F23	D3
IO256PB7F23	E3
IO257NB7F23	F5
IO257PB7F23	G5
Dedicated I/O	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26

FG676	
AX1000 Function	Pin Number
NC	D13
NC	D14
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18

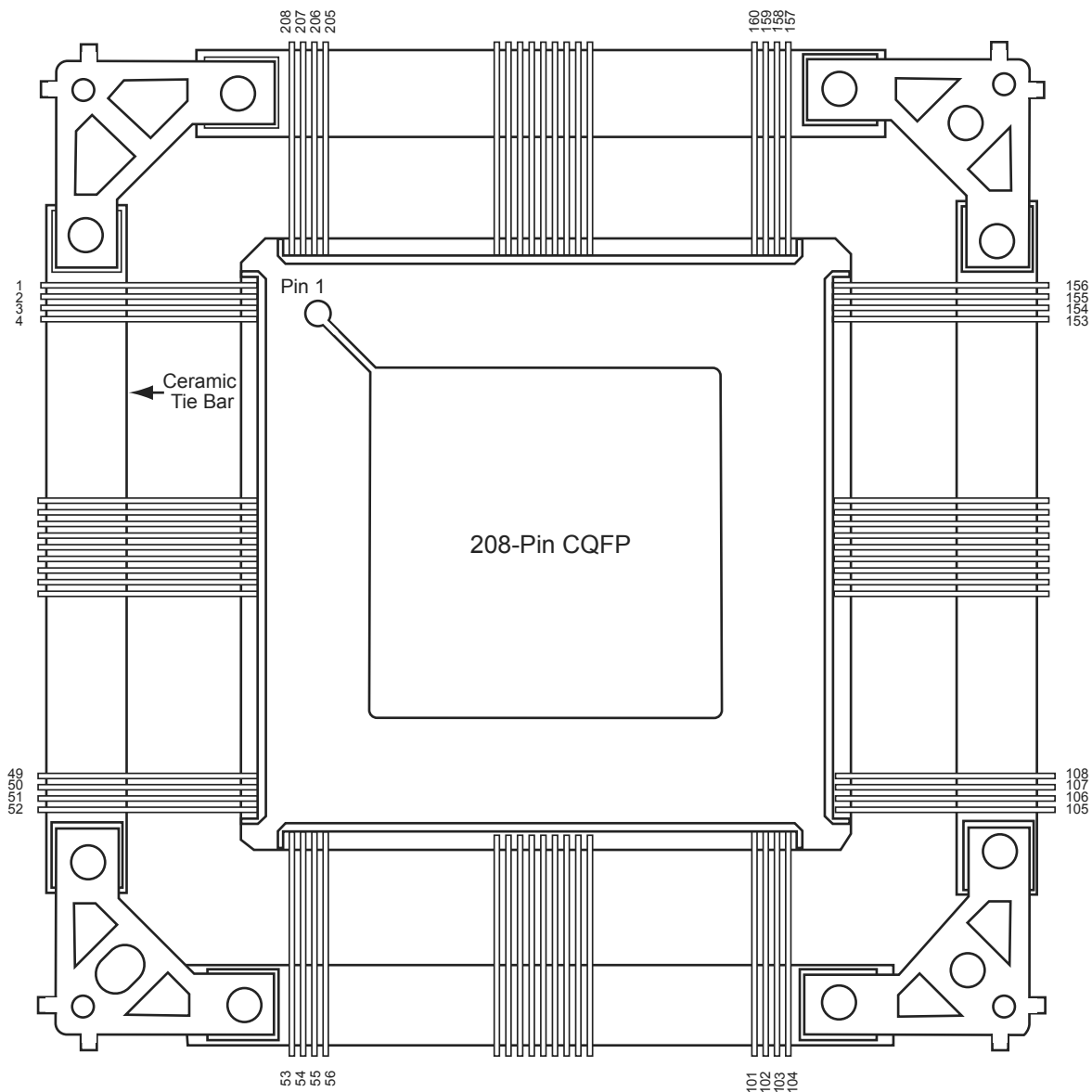
FG676	
AX1000 Function	Pin Number
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14
VCCA	V15
VCCA	V16
VCCA	V17
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCCDA	A11
VCCDA	A3
VCCDA	AB22
VCCDA	AB5
VCCDA	AD10
VCCDA	AD11
VCCDA	AD13
VCCDA	AD16
VCCDA	AD17
VCCDA	B1
VCCDA	B11
VCCDA	B17
VCCDA	C16
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23

FG676	
AX1000 Function	Pin Number
VCCIB0	G10
VCCIB0	G8
VCCIB0	G9
VCCIB0	H10
VCCIB0	H11
VCCIB0	H12
VCCIB0	H13
VCCIB0	H9
VCCIB1	G17
VCCIB1	G18
VCCIB1	G19
VCCIB1	H14
VCCIB1	H15
VCCIB1	H16
VCCIB1	H17
VCCIB1	H18
VCCIB2	H20
VCCIB2	J19
VCCIB2	J20
VCCIB2	K19
VCCIB2	K20
VCCIB2	L19
VCCIB2	M19
VCCIB2	N19
VCCIB3	P19
VCCIB3	R19
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
NC	K1	VCCA	N20	VCCDA	AF19
NC	K2	VCCA	P11	VCCDA	C13
NC	L30	VCCA	P20	VCCDA	C5
NC	M30	VCCA	R11	VCCDA	D13
NC	N29	VCCA	R20	VCCDA	D19
NC	T1	VCCA	T11	VCCDA	D3
NC	U1	VCCA	T20	VCCDA	E18
NC	W30	VCCA	U11	VCCDA	F26
NC	Y1	VCCA	U20	VCCDA	G16
NC	Y2	VCCA	V11	VCCDA	T25
NC	Y30	VCCA	V20	VCCDA	T4
PRA	G15	VCCA	W11	VCCIB0	A3
PRB	D16	VCCA	W20	VCCIB0	B3
PRC	AB16	VCCA	Y12	VCCIB0	J10
PRD	AF16	VCCA	Y13	VCCIB0	J11
TCK	G7	VCCA	Y14	VCCIB0	J12
TDI	D5	VCCA	Y15	VCCIB0	K11
TDO	J8	VCCA	Y16	VCCIB0	K12
TMS	F6	VCCA	Y17	VCCIB0	K13
TRST	C4	VCCA	Y18	VCCIB0	K14
VCCA	AD6	VCCA	Y19	VCCIB0	K15
VCCA	AH26	VCCPLA	G14	VCCIB1	A28
VCCA	E28	VCCPLB	H15	VCCIB1	B28
VCCA	E3	VCCPLC	G17	VCCIB1	J19
VCCA	L12	VCCPLD	J16	VCCIB1	J20
VCCA	L13	VCCPLE	AH17	VCCIB1	J21
VCCA	L14	VCCPLF	AC16	VCCIB1	K16
VCCA	L15	VCCPLG	AH14	VCCIB1	K17
VCCA	L16	VCCPLH	AD15	VCCIB1	K18
VCCA	L17	VCCDA	AD24	VCCIB1	K19
VCCA	L18	VCCDA	AD7	VCCIB1	K20
VCCA	L19	VCCDA	AF12	VCCIB2	C29
VCCA	M11	VCCDA	AF13	VCCIB2	C30
VCCA	M20	VCCDA	AF15	VCCIB2	K22
VCCA	N11	VCCDA	AF18	VCCIB2	L21

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	AK12	GND	AN34	GND	D1
GND	AK17	GND	AN4	GND	D11
GND	AK18	GND	AN9	GND	D2
GND	AK23	GND	AP13	GND	D24
GND	AK30	GND	AP2	GND	D3
GND	AK5	GND	AP22	GND	D31
GND	AL1	GND	AP27	GND	D32
GND	AL11	GND	AP3	GND	D33
GND	AL2	GND	AP31	GND	D34
GND	AL24	GND	AP32	GND	D4
GND	AL3	GND	AP33	GND	E12
GND	AL31	GND	AP4	GND	E17
GND	AL32	GND	AP8	GND	E18
GND	AL33	GND	B1	GND	E23
GND	AL34	GND	B2	GND	E30
GND	AL4	GND	B26	GND	E5
GND	AM1	GND	B3	GND	F29
GND	AM10	GND	B31	GND	F30
GND	AM15	GND	B32	GND	F6
GND	AM2	GND	B33	GND	G28
GND	AM20	GND	B34	GND	G7
GND	AM25	GND	B4	GND	H1
GND	AM3	GND	B9	GND	H34
GND	AM31	GND	C1	GND	J2
GND	AM32	GND	C10	GND	J33
GND	AM33	GND	C15	GND	K3
GND	AM34	GND	C2	GND	K32
GND	AM4	GND	C20	GND	L11
GND	AN1	GND	C25	GND	L24
GND	AN2	GND	C3	GND	L31
GND	AN26	GND	C31	GND	L4
GND	AN3	GND	C32	GND	M12
GND	AN31	GND	C33	GND	M23
GND	AN32	GND	C34	GND	M30
GND	AN33	GND	C4	GND	M5

CQ208



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CQ352	
AX250 Function	Pin Number
IO64PB4F4	167
IO65NB4F4	170
IO65PB4F4	171
IO66NB4F4	164
IO66PB4F4	165
IO67NB4F4	160
IO67PB4F4	161
IO68NB4F4	158
IO68PB4F4	159
IO70NB4F4	154
IO70PB4F4	155
IO72NB4F4	152
IO72PB4F4	153
IO73NB4F4	146
IO73PB4F4	147
IO74NB4F4/CLKEN	142
IO74PB4F4/CLKEP	143
IO75NB4F4/CLKFN	136
IO75PB4F4/CLKFP	137
Bank 5	
IO76NB5F5/CLKGN	128
IO76PB5F5/CLKGP	129
IO77NB5F5/CLKHN	122
IO77PB5F5/CLKHP	123
IO78NB5F5	112
IO78PB5F5	113
IO79NB5F5	118
IO79PB5F5	119
IO80NB5F5	110
IO80PB5F5	111
IO82NB5F5	106
IO82PB5F5	107
IO84NB5F5	100
IO84PB5F5	101
IO85NB5F5	104

CQ352	
AX250 Function	Pin Number
IO85PB5F5	105
IO86NB5F5	98
IO86PB5F5	99
IO87NB5F5	94
IO87PB5F5	95
IO89NB5F5	92
IO89PB5F5	93
Bank 6	
IO90PB6F6	86
IO91NB6F6	84
IO91PB6F6	85
IO92NB6F6	78
IO92PB6F6	79
IO93NB6F6	82
IO93PB6F6	83
IO95NB6F6	76
IO95PB6F6	77
IO96NB6F6	72
IO96PB6F6	73
IO97NB6F6	70
IO97PB6F6	71
IO98NB6F6	66
IO98PB6F6	67
IO99NB6F6	64
IO99PB6F6	65
IO100NB6F6	60
IO100PB6F6	61
IO101NB6F6	58
IO101PB6F6	59
IO103NB6F6	54
IO103PB6F6	55
IO104NB6F6	52
IO104PB6F6	53
IO105NB6F6	48
IO105PB6F6	49

CQ352	
AX250 Function	Pin Number
IO106NB6F6	46
IO106PB6F6	47
Bank 7	
IO107NB7F7	40
IO107PB7F7	41
IO108NB7F7	42
IO108PB7F7	43
IO109NB7F7	36
IO109PB7F7	37
IO110NB7F7	34
IO110PB7F7	35
IO111NB7F7	30
IO111PB7F7	31
IO113NB7F7	28
IO113PB7F7	29
IO114NB7F7	24
IO114PB7F7	25
IO115NB7F7	22
IO115PB7F7	23
IO116NB7F7	18
IO116PB7F7	19
IO117NB7F7	16
IO117PB7F7	17
IO118NB7F7	12
IO118PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121NB7F7	6
IO121PB7F7	7
IO123NB7F7	4
IO123PB7F7	5
Dedicated I/O	
GND	1
GND	9
GND	15

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO131NB4F12	V19	IO153NB4F14	Y15	IO173PB5F16	Y11
IO131PB4F12	W19	IO153PB4F14	Y16	IO174NB5F16	AB10
IO133NB4F12	Y18	IO155NB4F14	V15	IO174PB5F16	AB11
IO133PB4F12	Y19	IO155PB4F14	V16	IO175NB5F16	AC9
IO135NB4F12	W18	IO156NB4F14	AB14	IO175PB5F16	AE9
IO135PB4F12	V18	IO156PB4F14	AB15	IO177NB5F16	AA8
IO137NB4F12	Y17	IO157NB4F14	AE14	IO177PB5F16	Y8
IO137PB4F12	AA17	IO157PB4F14	AC18	IO178NB5F16	Y6
IO138NB4F12	AB19	IO158NB4F14	AC15	IO178PB5F16	W6
IO138PB4F12	AB18	IO158PB4F14	AC19	IO179NB5F16	Y10
IO139NB4F13	AA19	IO159NB4F14/CLKEN	W14	IO179PB5F16	W10
IO139PB4F13	U18	IO159PB4F14/CLKEP	W15	IO180NB5F16	Y7
IO140NB4F13	AC20	IO160NB4F14/CLKFN	AC13	IO180PB5F16	W7
IO140PB4F13	AC21	IO160PB4F14/CLKFP	AD13	IO181NB5F17	AD9
IO141NB4F13	AD17	Bank 5		IO181PB5F17	AD10
IO141PB4F13	AD18	IO161NB5F15/CLKGN	W13	IO182NB5F17	AE10
IO142NB4F13	AD21	IO161PB5F15/CLKGP	Y13	IO182PB5F17	AE11
IO142PB4F13	AD22	IO162NB5F15/CLKHN	AC12	IO183NB5F17	AD7
IO143NB4F13	AB17	IO162PB5F15/CLKHP	AD12	IO183PB5F17	AD8
IO143PB4F13	AC17	IO163NB5F15	V9	IO184NB5F17	AB9
IO144PB4F13	AE22	IO163PB5F15	V10	IO185NB5F17	AE6
IO145NB4F13	AE15	IO164NB5F15	V11	IO185PB5F17	AE7
IO145PB4F13	AE16	IO164PB5F15	T13	IO186NB5F17	AE4
IO146NB4F13	AD19	IO165NB5F15	U13	IO186PB5F17	AE5
IO146PB4F13	AD20	IO165PB5F15	V13	IO187NB5F17	AA9
IO147NB4F13	AD15	IO167NB5F15	W11	IO187PB5F17	Y9
IO147PB4F13	AD16	IO167PB5F15	W12	IO188NB5F17	U8
IO148PB4F13	AE21	IO168NB5F15	AB6	IO189NB5F17	AD5
IO149NB4F13	AD14	IO168PB5F15	AA6	IO189PB5F17	AD6
IO149PB4F13	AC14	IO169NB5F15	V8	IO191NB5F17	AC5
IO150NB4F13	AE19	IO169PB5F15	V7	IO191PB5F17	AC6
IO150PB4F13	AE20	IO171NB5F16	W8	IO192NB5F17	AB7
IO151NB4F13	V17	IO171PB5F16	W9	IO192PB5F17	AC7
IO151PB4F13	W17	IO172NB5F16	AB8	Bank 6	
IO152NB4F14	AB16	IO172PB5F16	AC8	IO193NB6F18	U6
IO152PB4F14	W16	IO173NB5F16	AA11	IO193PB6F18	U5