



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	198
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	352-BFCQFP with Tie Bar
Supplier Device Package	352-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-cq352m

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

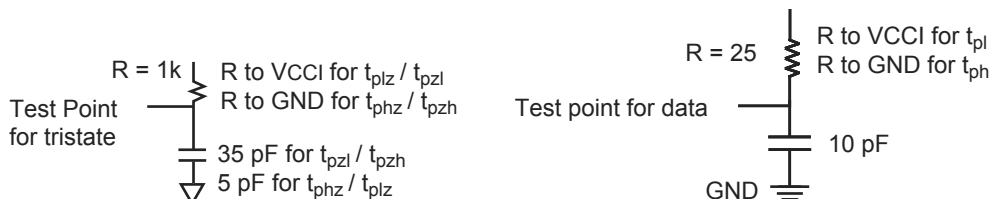


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

Timing Model and Waveforms

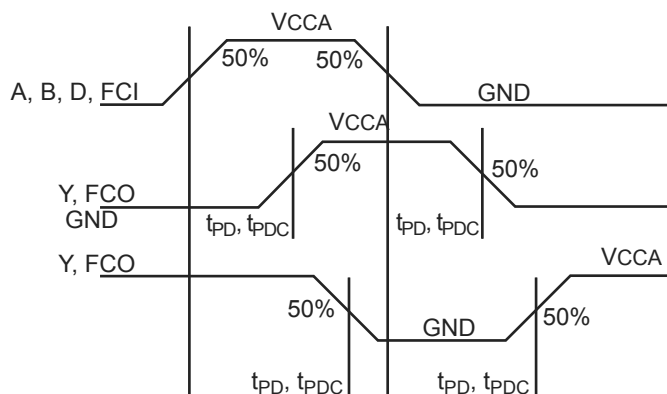


Figure 2-28 • C-Cell Timing Model and Waveforms

Timing Characteristics

Table 2-62 • C-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t _{PD}	Any input to output Y	0.74		0.84		0.99		ns
t _{PDC}	Any input to carry chain output (FCO)	0.57		0.64		0.76		ns
t _{PDB}	Any input through DB when one input is used	0.95		1.09		1.28		ns
t _{CCY}	Input to carry chain (FCI) to Y	0.61		0.69		0.82		ns
t _{CC}	Input to carry chain (FCI) to carry chain output (FCO)	0.08		0.09		0.11		ns

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-37 on page 2-62). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 2-37). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

Figure 2-36 • FastConnect Routing

Figure 2-37 • Horizontal and Vertical Tracks

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t _{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t _{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t _{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t _{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t _{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t _{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t _{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t _{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t _{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t _{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t _{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t _{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t _{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t _{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t _{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t _{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t _{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t _{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-77 • AX500 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		2.31		2.63		3.09	ns
t _{RCKH}	Input High to Low		2.44		2.78		3.27	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-78 • AX1000 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-79 • AX2000 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

single-ended, or voltage-referenced standard. The [H]CLKxN pad can only be used as a differential pair with [H]CLKxP.

The block marked “i Delay Match” is a fixed delay equal to that of the i divider. The “j Delay Match” block has the same function as its j divider counterpart.

Functional Description

Figure 2-48 on page 2-75 illustrates a block diagram of the PLL. The PLL contains two dividers, i and j, that allow frequency scaling of the clock signal:

- The i divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64, and the resultant frequency is available at the output of the PLL block.
- The j divider divides the PLL output by integer factors ranging from 1 to 64, and the divided clock is available at CLK1.
- The two dividers together can implement any combination of multiplication and division up to a maximum frequency of 1 GHz on CLK1. Both the CLK1 and CLK2 outputs have a fixed 50/50 duty cycle.
- The output frequencies of the two clocks are given by the following formulas (f_{REF} is the reference clock frequency):

$$f_{CLK1} = f_{REF} * (DividerI) / (DividerJ)$$

EQ 4

$$f_{CLK2} = f_{REF} * (DividerI)$$

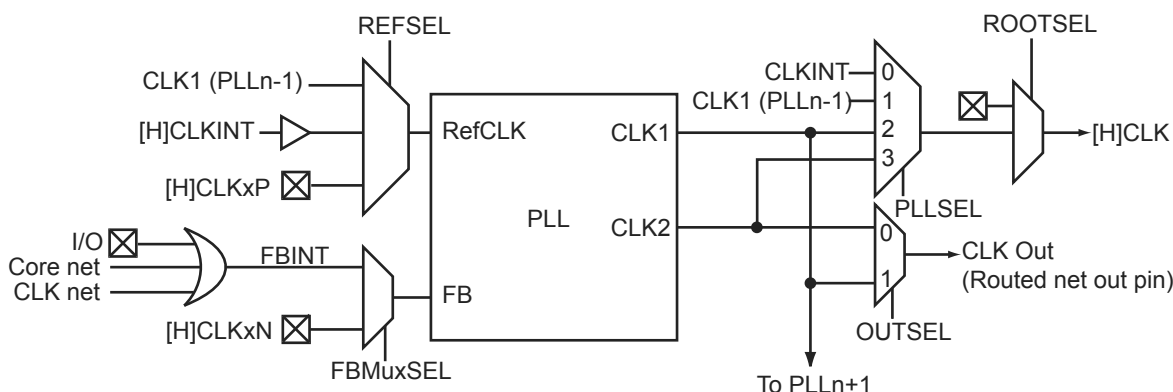
EQ 5

- CLK2 provides the PLL output directly—without division

The input and output frequency ranges are selected by LowFreq and Osc(2:0), respectively. These functions and their possible values are detailed in Table 2-80 on page 2-77.

The delay lines shown in Figure 2-48 on page 2-75 are programmable. The feedback clock path can be delayed (using the five DelayLine bits) relative to the reference clock (or vice versa) by up to 3.75 ns in increments of 250 ps. Table 2-80 on page 2-77 describes the usage of these bits. The delay increments are independent of frequency, so this results in phase changes that vary with frequency. The delay value is highly dependent on V_{CC} and the speed grade.

Figure 2-49 is a logical diagram of the various control signals to the PLL and shows how the PLL interfaces with the global and routing networks of the FPGA. Note that not all signals are user-accessible. These non-user-accessible signals are used by the place-and-route tool to control the configuration of the PLL. The user gains access to these control signals either based upon the connections built in the user's design or through the special macros (Table 2-84 on page 2-81) inserted into the design. For example, connecting the macro PLLOUT to CLK2 will control the OUTSEL signal.



Note: Not all signals are available to the user.

Figure 2-49 • PLL Logical Interface

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-86). Each block has independent read and write ports which enable simultaneous read and write operations.

Table 2-86 • Memory Block WxD Options

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in Table 2-87.

Table 2-87 • Allowable RW and WW Values

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

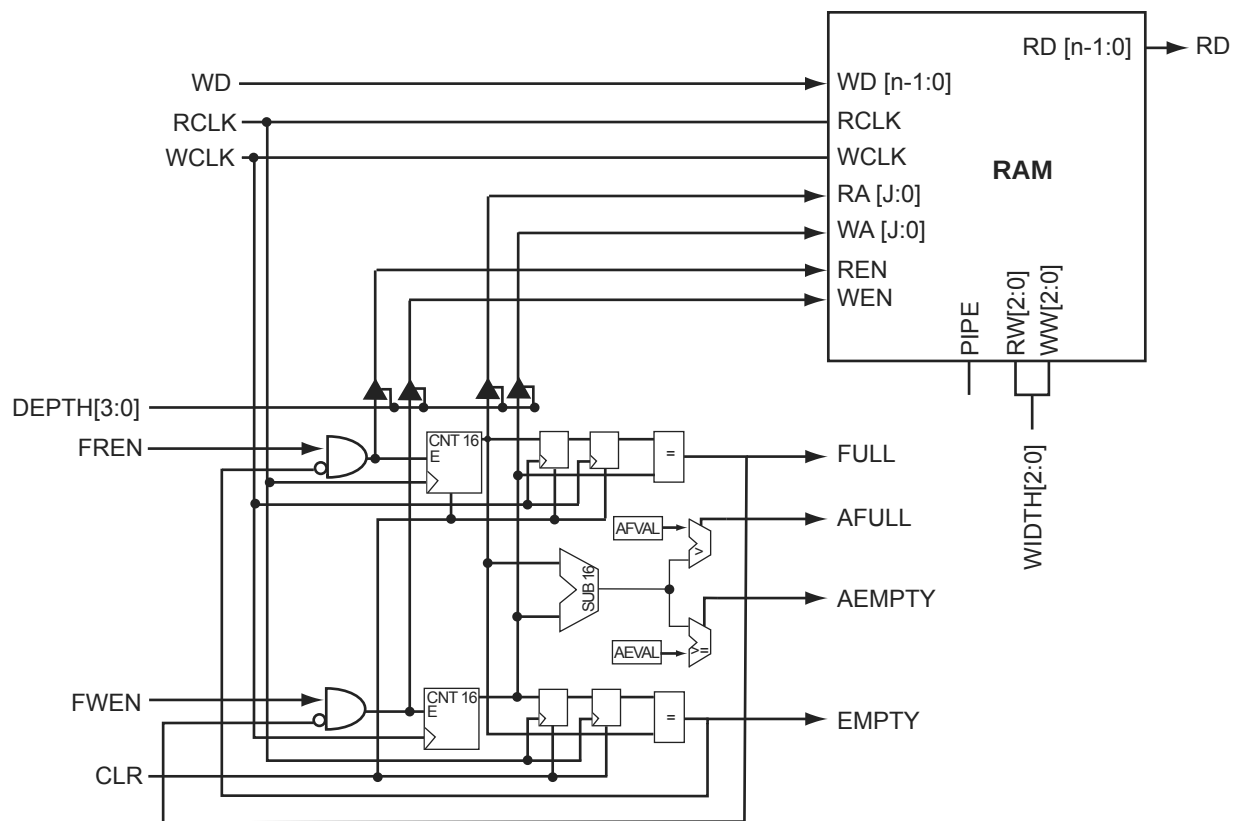


Figure 2-61 • Axcelerator RAM with Embedded FIFO Controller

mode if desired. Please note, if the I/O bank is not disabled, differential I/Os belonging to the I/O bank will still consume normal power, even when operating in the low power mode.

The Axcelerator device will resume normal operation 10 μ s after the LP pin is pulled Low.

To further reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e. high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

In addition, any PLL in use can be powered down to further reduce power consumption. This can be done with the PowerDown pin driven Low. Driving this pin High restarts the PLL with the output clock(s) being stable once lock is restored.

JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the Table 2-103.

Table 2-103 • JTAG Instruction Code

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload / Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
Reserved	All others
Bypass	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low, asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1 k Ω resistor.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a VCCA and/or VCCDA voltage drop.

BG729	
AX1000 Function	Pin Number
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16

BG729	
AX1000 Function	Pin Number
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

FG484		FG484		FG484	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO87PB2F8	H20	IO106PB3F9	P17	IO142PB4F13	V20
IO88NB2F8	L18	IO107NB3F10	T21	IO143NB4F13	W15
IO88PB2F8	K18	IO107PB3F10	R21	IO143PB4F13	W16
IO89NB2F8	K19	IO110NB3F10	V22	IO144NB4F13	AA18
IO89PB2F8	J19	IO110PB3F10	U22	IO144PB4F13	AA19
IO90NB2F8	J21	IO113NB3F10	V21	IO145NB4F13	U14
IO90PB2F8	H21	IO113PB3F10	U21	IO145PB4F13	U15
IO91NB2F8	J22	IO114NB3F10	P18	IO146NB4F13	Y15
IO91PB2F8	H22	IO114PB3F10	P19	IO146PB4F13	Y16
IO93NB2F8	K21	IO116PB3F10	R19	IO147NB4F13	AB18
IO93PB2F8	K22	IO117NB3F10	U20	IO147PB4F13	AB19
IO94NB2F8	L20	IO117PB3F10	T20	IO149NB4F13	Y14
IO94PB2F8	K20	IO118NB3F11	T18	IO149PB4F13	W14
IO95NB2F8	M21	IO118PB3F11	R18	IO150NB4F13	AA16
IO95PB2F8	L21	IO121NB3F11	U19	IO150PB4F13	AA17
Bank 3		IO121PB3F11	T19	IO152NB4F14	AA14
IO96NB3F9	N16	IO124NB3F11	R16	IO152PB4F14	AA15
IO96PB3F9	M16	IO124PB3F11	P16	IO154NB4F14	AB14
IO97NB3F9	M19	IO127NB3F11	W21	IO154PB4F14	AB15
IO97PB3F9	L19	IO127PB3F11	W22	IO155NB4F14	AA13
IO98NB3F9	P22	Bank 4		IO155PB4F14	AB13
IO98PB3F9	N22	IO129PB4F12	AB17	IO158NB4F14	Y12
IO99NB3F9	N20	IO132NB4F12	Y19	IO158PB4F14	Y13
IO99PB3F9	M20	IO132PB4F12	W18	IO159NB4F14/CLKEN	V12
IO100NB3F9	N17	IO133NB4F12	W17	IO159PB4F14/CLKEP	V13
IO100PB3F9	M17	IO133PB4F12	V17	IO160NB4F14/CLKFN	W11
IO101NB3F9	P21	IO135NB4F12	T15	IO160PB4F14/CLKFP	W12
IO101PB3F9	N21	IO135PB4F12	T16	Bank 5	
IO103NB3F9	R20	IO138NB4F12	Y17	IO161NB5F15/CLKGN	U10
IO103PB3F9	P20	IO138PB4F12	Y18	IO161PB5F15/CLKGP	U11
IO104NB3F9	N18	IO139NB4F13	V15	IO162NB5F15/CLKHN	V9
IO104PB3F9	N19	IO139PB4F13	V16	IO162PB5F15/CLKHP	V10
IO105NB3F9	T22	IO140NB4F13	U18	IO163NB5F15	Y10
IO105PB3F9	R22	IO140PB4F13	V19	IO163PB5F15	Y11
IO106NB3F9	R17	IO142NB4F13	W20	IO167NB5F15	AA11

FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO153PB7F14	M6	GND	A8	GND	L11
IO154NB7F14	K2	GND	AC23	GND	L12
IO154PB7F14	L2	GND	AC4	GND	L13
IO155NB7F14	K3	GND	AD24	GND	L14
IO155PB7F14	L3	GND	AD3	GND	L15
IO156NB7F14	L5	GND	AE2	GND	L16
IO156PB7F14	L4	GND	AE25	GND	L17
IO157NB7F14	L6	GND	AF1	GND	M10
IO157PB7F14	L7	GND	AF13	GND	M11
IO158NB7F15	J1	GND	AF14	GND	M12
IO158PB7F15	K1	GND	AF19	GND	M13
IO159NB7F15	J4	GND	AF26	GND	M14
IO159PB7F15	K4	GND	AF8	GND	M15
IO160NB7F15	H2	GND	B2	GND	M16
IO160PB7F15	J2	GND	B25	GND	M17
IO161NB7F15	K6	GND	B26	GND	N1
IO161PB7F15	K5	GND	C24	GND	N10
IO162NB7F15	H3	GND	C3	GND	N11
IO162PB7F15	J3	GND	G20	GND	N12
IO163NB7F15	G2	GND	G7	GND	N13
IO163PB7F15	G1	GND	H1	GND	N14
IO164NB7F15	G4	GND	H19	GND	N15
IO164PB7F15	H4	GND	H26	GND	N16
IO165NB7F15	F3	GND	H8	GND	N17
IO165PB7F15	G3	GND	J18	GND	N26
IO166NB7F15	E2	GND	J9	GND	P1
IO166PB7F15	F2	GND	K10	GND	P10
IO167NB7F15	F5	GND	K11	GND	P11
IO167PB7F15	G5	GND	K12	GND	P12
Dedicated I/O		GND	K13	GND	P13
GND	A1	GND	K14	GND	P14
GND	A13	GND	K15	GND	P15
GND	A14	GND	K16	GND	P16
GND	A19	GND	K17	GND	P17
GND	A26	GND	L10	GND	P26

FG676	
AX500 Function	Pin Number
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8

FG676	
AX500 Function	Pin Number
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
NC	AP9	PRB	F18	VCCA	T22
NC	B17	PRC	AD18	VCCA	U13
NC	B22	PRD	AH18	VCCA	U22
NC	B27	TCK	J9	VCCA	V13
NC	B8	TDI	F7	VCCA	V22
NC	D10	TDO	L10	VCCA	W13
NC	D20	TMS	H8	VCCA	W22
NC	D23	TRST	E6	VCCA	Y13
NC	D25	VCCA	AA13	VCCA	Y22
NC	F3	VCCA	AA22	VCCDA	AF26
NC	F32	VCCA	AB14	VCCDA	AF9
NC	F33	VCCA	AB15	VCCDA	AG17
NC	F34	VCCA	AB16	VCCDA	AG18
NC	F4	VCCA	AB17	VCCDA	AH14
NC	G1	VCCA	AB18	VCCDA	AH15
NC	G32	VCCA	AB19	VCCDA	AH17
NC	G33	VCCA	AB20	VCCDA	AH20
NC	G34	VCCA	AB21	VCCDA	AH21
NC	H31	VCCA	AF8	VCCDA	AK29
NC	H33	VCCA	AK28	VCCDA	AK6
NC	J1	VCCA	G30	VCCDA	E15
NC	J3	VCCA	G5	VCCDA	E29
NC	J34	VCCA	N14	VCCDA	E7
NC	M1	VCCA	N15	VCCDA	F15
NC	M4	VCCA	N16	VCCDA	F21
NC	P1	VCCA	N17	VCCDA	F5
NC	P2	VCCA	N18	VCCDA	G20
NC	R31	VCCA	N19	VCCDA	H17
NC	T1	VCCA	N20	VCCDA	H18
NC	T2	VCCA	N21	VCCDA	H28
NC	V3	VCCA	P13	VCCDA	J18
NC	V34	VCCA	P22	VCCDA	V27
NC	W3	VCCA	R13	VCCDA	V6
NC	W34	VCCA	R22	VCCIB0	A5
PRA	J17	VCCA	T13	VCCIB0	B5

CQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

CQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

CQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132

CQ208	
AX500 Function	Pin Number
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
Bank 4	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76

CQ208	
AX500 Function	Pin Number
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18

CQ352	
AX250 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CQ352	
AX2000 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX2000 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 18 (March 2012)	Table 2-1 • Absolute Maximum Ratings was updated to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419).	2-1
	Values for tristate leakage current IOZ, and I _{IH} and I _{IL} were added to Table 2-3 • Standby Current (SARs 35774, 32021).	2-2
	Figure 2-2 • VCCPLX and VCOMPLX Power Supply Connect was updated to correct the units for the resistance from "W" to Ω (SAR 36415).	2-9
	In the Introduction to the "User I/Os" section, the following sentence was added to clarify the slew rate setting (SAR 34943): The slew rate setting is effective for both rising and falling edges.	2-11
	Figure 2-3 • Use of an External Resistor for 5 V Tolerance was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942).	2-13
	EQ 3 for 5 V tolerance was corrected to change V _{diode} from 0.6 V to 0.7 V (SAR 36786).	2-13
	Additional information was added to the "Using the Weak Pull-Up and Pull-Down Circuits" section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945).	2-17
	The description for the C _{INCLK} parameter in Table 2-18 • Input Capacitance was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944).	2-21
	Table 2-19 • I/O Input Rise Time and Fall Time* is new (SAR 34942).	2-21
	The minimum V _{IL} for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-29 • DC Input and Output Levels and Table 2-33 • DC Input and Output Levels (SAR 34358).	2-38, 2-40
	Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the <i>Antifuse Macro Library Guide</i> was added to the "R-Cell" section (SAR 26413).	2-58
Revision 17 (September 2011)	The enable signal in Figure 2-32 • R-Cell Delays was corrected to show it is active low rather than active high (SAR 34946).	2-59
	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Axcelerator Family Device Status" table indicates the status for each device in the device family.	iii
	The "Features" section, "Programmable Interconnect Element" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865).	i, 1-1, 2-108