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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	586
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-fgg896

Table of Contents

1 – General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microsemi AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

Device Architecture

AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

The very nature of Microsemi's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-108).

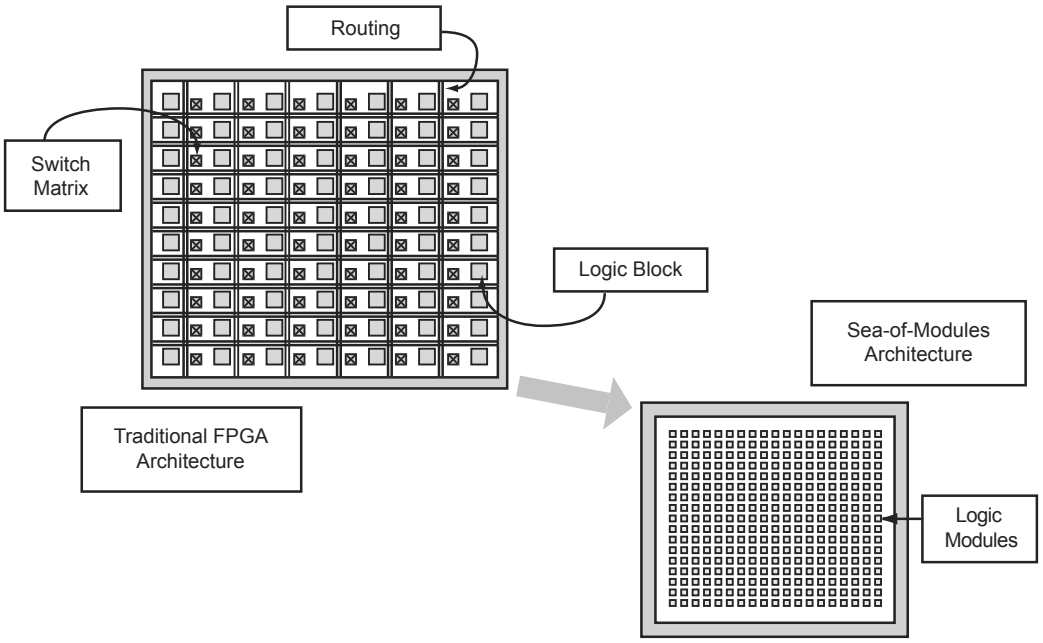


Figure 1-1 • **Sea-of-Modules Comparison**

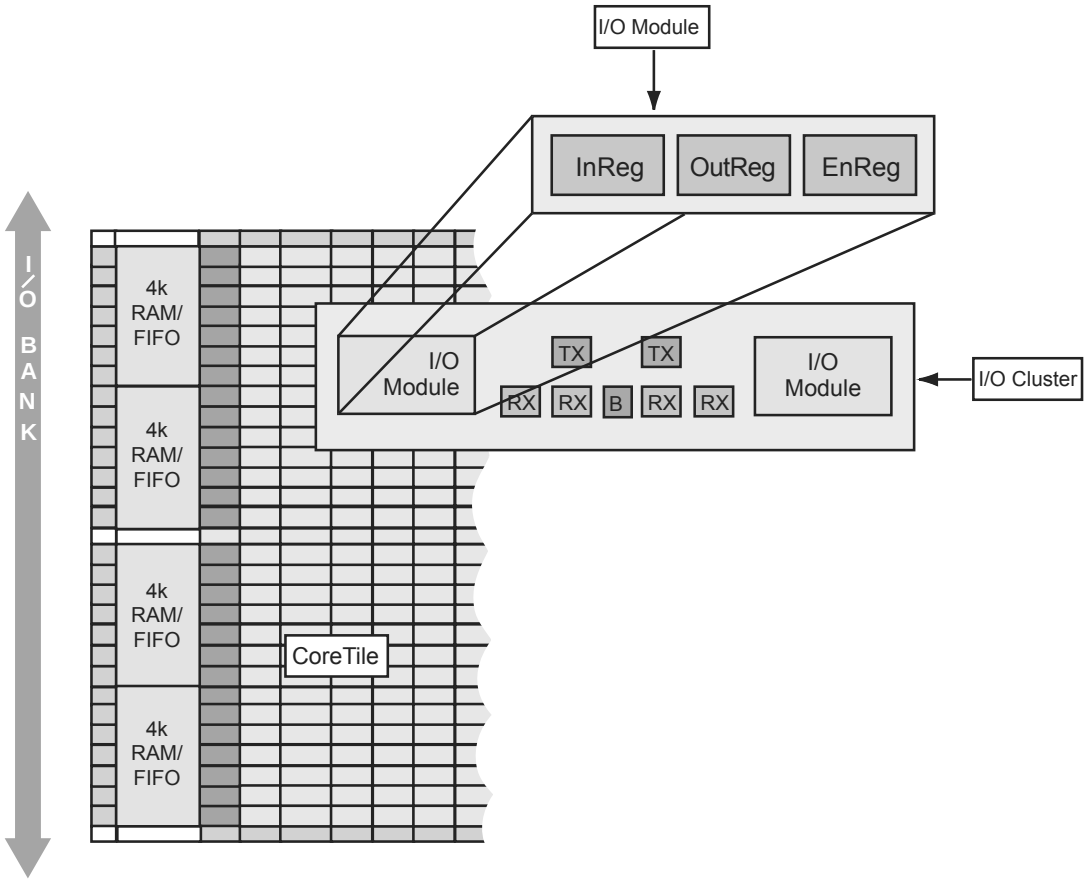


Figure 1-7 • **I/O Cluster Arrangement**

Routing

The AX hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together (Figure 1-8 on page 1-6). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

FastConnects provide high-performance, horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the FCO output of one two-bit, C-cell carry logic to the FCI input of the two-bit, C-cell carry logic of the SuperCluster below it. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. Over the SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns, respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north-to-south and east-to-west. These tracks are composed of highway routing that extend the entire length of the device (segmented at core tile boundaries) as well as segmented routing of varying lengths.

5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

EQ 3

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

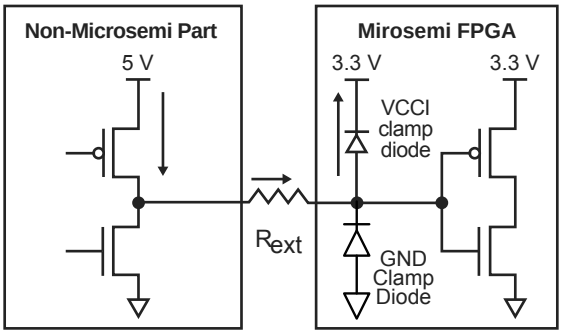


Figure 2-3 • **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

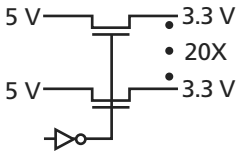


Figure 2-4 • **Bus Switch IDTQS32X2384**

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

3. The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.

Timing Characteristics

***Table 2-25* • 2.5V LVCMOS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVCMOS25 I/O Module Timing								
t_{DP}	Input Buffer		1.95		2.22		2.61	ns
t_{PY}	Output Buffer		3.29		3.74		4.40	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.48		2.50		2.51	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.48		2.50		2.51	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		5.74		6.54		7.69	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.60		7.51		8.83	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

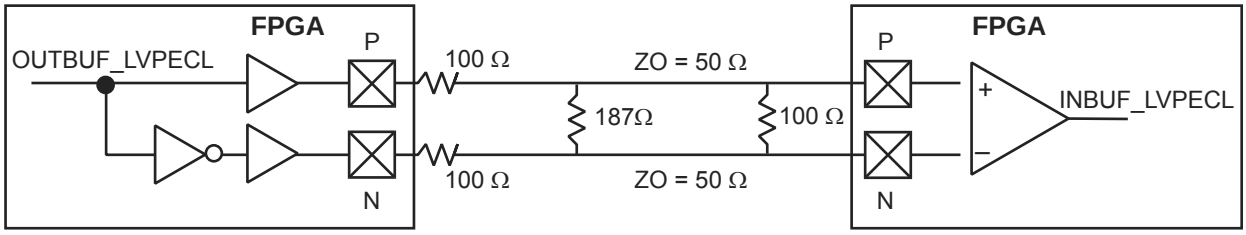


Figure 2-26 • **LVPECL Board-Level Implementation**

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS since the output voltage levels are different. Please note that the VOH levels are 200 mV below the standard LVPECL levels.

Table 2-59 • **DC Input and Output Levels**

	Min.		Typ.		Max.		
DC Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
VCCI	3		3.3		3.6		V
VOH	1.8	2.11	1.92	2.28	2.13	2.41	V
VOL	0.96	1.27	1.06	1.43	1.3	1.57	V
VIH	1.49	2.72	1.49	2.72	1.49	2.72	V
VIL	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3		0.3		0.3		V

Table 2-60 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.6 – 0.3	1.6 + 0.3	1.6

*Note: * Measuring Point = VTRIP*

Timing Model and Waveforms

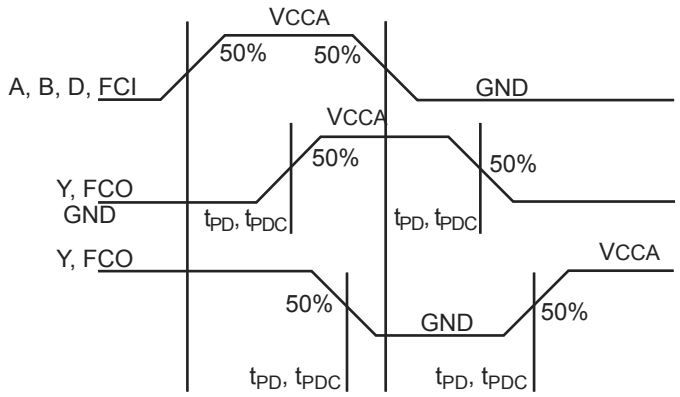


Figure 2-28 • **C-Cell Timing Model and Waveforms**

Timing Characteristics

Table 2-62 • **C-Cell**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays								
t_{PD}	Any input to output Y		0.74		0.84		0.99	ns
t_{PDC}	Any input to carry chain output (FCO)		0.57		0.64		0.76	ns
t_{PDB}	Any input through DB when one input is used		0.95		1.09		1.28	ns
t_{CCY}	Input to carry chain (FCI) to Y		0.61		0.69		0.82	ns
t_{CC}	Input to carry chain (FCI) to carry chain output (FCO)		0.08		0.09		0.11	ns

Buffer Module

Introduction

An additional resource inside each SuperCluster is the Buffer (B) module (Figure 1-4 on page 1-3). When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the AX architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium-to-high-fanout nets.

Timing Models and Waveforms

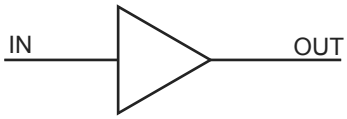


Figure 2-33 • **Buffer Module Timing Model**

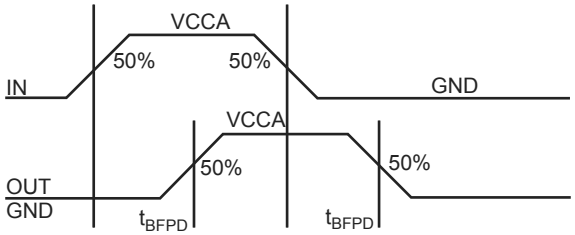


Figure 2-34 • **Buffer Module Waveform**

Timing Characteristics

Table 2-64 • **Buffer Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Buffer Module Propagation Delays								
t_{BFPD}	Any input to output Y		0.12		0.14		0.16	ns

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

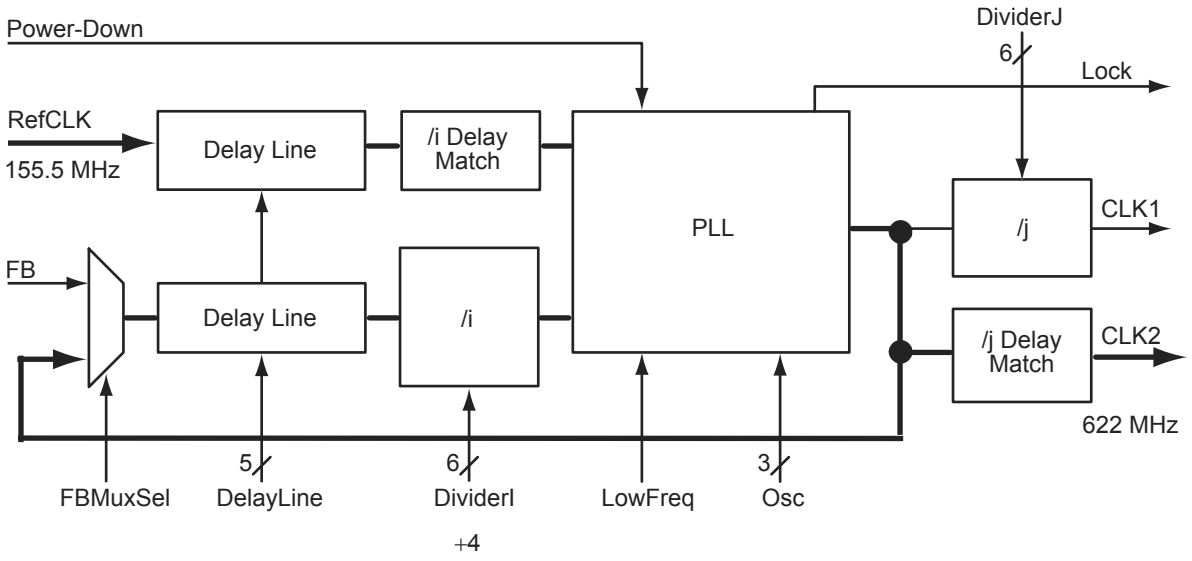


Figure 2-53 • **Using the PLL 155.5 MHz In, 622 MHz Out**

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

BG729	
AX1000 Function	Pin Number
IO163PB5F15	AA14
IO164NB5F15	AE13
IO164PB5F15	AF13
IO165NB5F15	AF12
IO165PB5F15	AG12
IO166NB5F15	AD12
IO166PB5F15	AE12
IO167NB5F15	Y13
IO167PB5F15	AA13
IO168NB5F15	AD11
IO168PB5F15	AE11
IO169NB5F15	AG11
IO169PB5F15	AF11
IO170NB5F15	AB11
IO170PB5F15	AC11
IO171NB5F16	AF10
IO171PB5F16	AG10
IO172NB5F16	AD10
IO172PB5F16	AE10
IO173NB5F16	Y12
IO173PB5F16	AA12
IO174NB5F16	AB10
IO174PB5F16	AC10
IO175NB5F16	AF9
IO175PB5F16	AG9
IO176NB5F16	AD9
IO176PB5F16	AE9
IO177NB5F16	Y11
IO177PB5F16	AA11
IO178NB5F16	AF8
IO178PB5F16	AG8
IO179NB5F16	AD8
IO179PB5F16	AE8
IO180NB5F16	AB9
IO180PB5F16	AC9
IO181NB5F17	Y10
IO181PB5F17	AA10

BG729	
AX1000 Function	Pin Number
IO182NB5F17	AF7
IO182PB5F17	AG7
IO183NB5F17	AD7
IO183PB5F17	AE7
IO184NB5F17	AC7
IO184PB5F17	AC8
IO185NB5F17	AF6
IO185PB5F17	AG6
IO186NB5F17	AB7
IO186PB5F17	AB8
IO187NB5F17	Y9
IO187PB5F17	AA9
IO188NB5F17	AD6
IO188PB5F17	AE6
IO189NB5F17	AB6
IO189PB5F17	AC6
IO190NB5F17	AF5
IO190PB5F17	AG5
IO191NB5F17	AA6
IO191PB5F17	AA7
IO192NB5F17	Y8
IO192PB5F17	AA8
Bank 6	
IO193NB6F18	W8
IO193PB6F18	Y7
IO194NB6F18	AB5
IO194PB6F18	AC5
IO195NB6F18	AC2
IO195PB6F18	AC3
IO196NB6F18	AC4
IO196PB6F18	AD4
IO197NB6F18	Y5
IO197PB6F18	Y6
IO198NB6F18	AB3
IO198PB6F18	AB4
IO199NB6F18	V7
IO199PB6F18	W7

BG729	
AX1000 Function	Pin Number
IO200NB6F18	AA4
IO200PB6F18	AA5
IO201NB6F18	W5
IO201PB6F18	W6
IO202NB6F18	AB1
IO202PB6F18	AC1
IO203NB6F19	Y3
IO203PB6F19	AA3
IO204NB6F19	AA2
IO204PB6F19	AB2
IO205NB6F19	U8
IO205PB6F19	V8
IO206NB6F19	V5
IO206PB6F19	V6
IO207NB6F19	Y1
IO207PB6F19	AA1
IO208NB6F19	W4
IO208PB6F19	Y4
IO209NB6F19	T7
IO209PB6F19	U7
IO210NB6F19	W2
IO210PB6F19	Y2
IO211NB6F19	U5
IO211PB6F19	U6
IO212NB6F19	V3
IO212PB6F19	W3
IO213NB6F19	R9
IO213PB6F19	T8
IO214NB6F20	U4
IO214PB6F20	V4
IO215NB6F20	T5
IO215PB6F20	T6
IO216NB6F20	V1
IO216PB6F20	W1
IO217NB6F20	R7
IO217PB6F20	R8
IO218NB6F20	U2

FG484	
AX500 Function	**Pin Number**
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
Bank 6	
IO126NB6F12	V2
IO126PB6F12	W2

FG484	
AX500 Function	**Pin Number**
IO127NB6F12	P7
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7

FG484	
AX500 Function	**Pin Number**
IO146NB6F13	M3
IO146PB6F13	N3
Bank 7	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3

FG676	
AX1000 Function	**Pin Number**
NC	D13
NC	D14
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18

FG676	
AX1000 Function	**Pin Number**
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14
VCCA	V15
VCCA	V16
VCCA	V17
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCCDA	A11
VCCDA	A3
VCCDA	AB22
VCCDA	AB5
VCCDA	AD10
VCCDA	AD11
VCCDA	AD13
VCCDA	AD16
VCCDA	AD17
VCCDA	B1
VCCDA	B11
VCCDA	B17
VCCDA	C16
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23

FG676	
AX1000 Function	**Pin Number**
VCCIB0	G10
VCCIB0	G8
VCCIB0	G9
VCCIB0	H10
VCCIB0	H11
VCCIB0	H12
VCCIB0	H13
VCCIB0	H9
VCCIB1	G17
VCCIB1	G18
VCCIB1	G19
VCCIB1	H14
VCCIB1	H15
VCCIB1	H16
VCCIB1	H17
VCCIB1	H18
VCCIB2	H20
VCCIB2	J19
VCCIB2	J20
VCCIB2	K19
VCCIB2	K20
VCCIB2	L19
VCCIB2	M19
VCCIB2	N19
VCCIB3	P19
VCCIB3	R19
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17

FG896	
AX1000 Function	Pin Number
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

FG896	
AX1000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

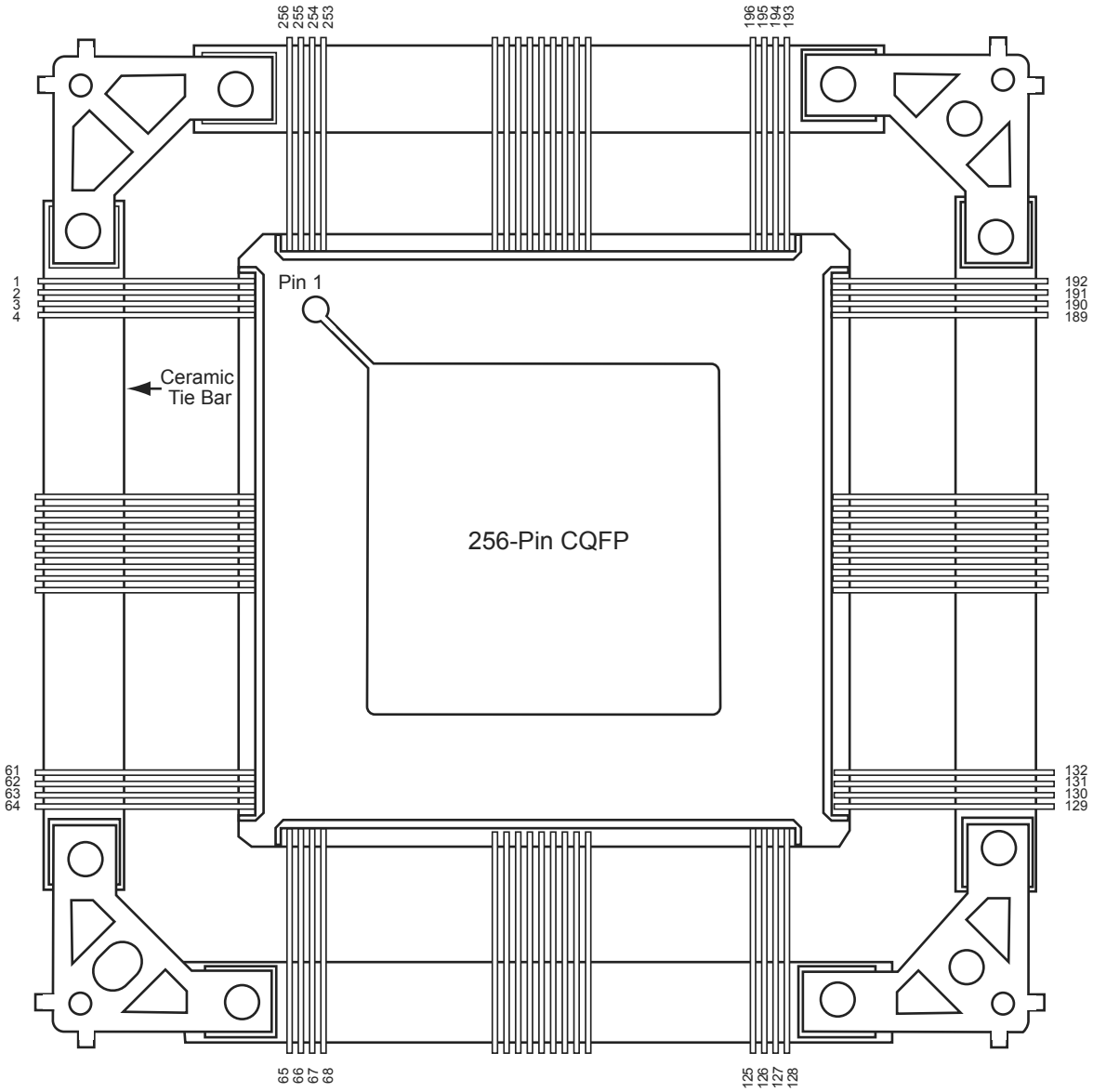
FG896	
AX1000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ256



Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CQ352	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282

CQ352	
AX2000 Function	Pin Number
IO71NB1F6	277
IO71PB1F6	278
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224

CQ352	
AX2000 Function	Pin Number
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170

CG624	
AX1000 Function	**Pin Number**
IO63PB1F5	G18
Bank 2	
IO64NB2F6	M17
IO64PB2F6	G22
IO65NB2F6	J21
IO65PB2F6	J20
IO66NB2F6	L23
IO66PB2F6	K20
IO67NB2F6	F23
IO67PB2F6	E23
IO68NB2F6	L18
IO68PB2F6	K18
IO70NB2F6	E24
IO70PB2F6	D24
IO71NB2F6	H23
IO71PB2F6	G23
IO72NB2F6	L19
IO72PB2F6	K19
IO74NB2F7	J22
IO74PB2F7	H22
IO75NB2F7	N23
IO75PB2F7	M23
IO76NB2F7	N17
IO76PB2F7	N16
IO77NB2F7	L22
IO77PB2F7	K22
IO78NB2F7	M19
IO78PB2F7	M18
IO79NB2F7	N19
IO79PB2F7	N18
IO80NB2F7	L21
IO80PB2F7	L20
IO82NB2F7	P18
IO82PB2F7	P17
IO83NB2F7	N22
IO83PB2F7	M22

CG624	
AX1000 Function	**Pin Number**
IO84NB2F7	M20
IO84PB2F7	M21
IO86NB2F8	E25
IO86PB2F8	D25
IO87NB2F8	L24
IO87PB2F8	K24
IO88NB2F8	G24
IO88PB2F8	F24
IO89NB2F8	J25
IO90NB2F8	G25
IO90PB2F8	F25
IO91NB2F8	L25
IO91PB2F8	K25
IO92NB2F8	J24
IO92PB2F8	H24
IO93PB2F8	J23
IO94NB2F8	N24
IO94PB2F8	M24
IO95NB2F8	N25
IO95PB2F8	M25
Bank 3	
IO96NB3F9	T18
IO96PB3F9	R18
IO97NB3F9	N20
IO97PB3F9	P24
IO98NB3F9	P20
IO98PB3F9	P19
IO99NB3F9	P21
IO100NB3F9	T22
IO100PB3F9	W24
IO101NB3F9	R22
IO101PB3F9	P22
IO102NB3F9	U19
IO102PB3F9	T19
IO104NB3F9	V20
IO104PB3F9	U20

CG624	
AX1000 Function	**Pin Number**
IO105NB3F9	R23
IO105PB3F9	P23
IO106NB3F9	R19
IO106PB3F9	R20
IO107NB3F10	AB24
IO108NB3F10	R25
IO108PB3F10	P25
IO109NB3F10	U25
IO109PB3F10	T25
IO110NB3F10	U24
IO110PB3F10	U23
IO112NB3F10	T24
IO112PB3F10	R24
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V23
IO114PB3F10	V24
IO116NB3F10	AA24
IO116PB3F10	Y24
IO117NB3F10	AB25
IO117PB3F10	AA25
IO118NB3F11	T20
IO118PB3F11	R21
IO120NB3F11	W22
IO120PB3F11	W23
IO122NB3F11	V22
IO122PB3F11	U22
IO124NB3F11	Y23
IO124PB3F11	AA23
IO126NB3F11	V21
IO126PB3F11	U21
IO128NB3F11	Y22
IO128PB3F11	Y21
Bank 4	
IO129NB4F12	W20
IO129PB4F12	Y20

CG624	
AX1000 Function	Pin Number
IO194NB6F18	Y3
IO194PB6F18	AA3
IO195NB6F18	V6
IO195PB6F18	W4
IO197NB6F18	R5
IO197PB6F18	U3
IO198NB6F18	P6
IO199NB6F18	Y5
IO199PB6F18	W5
IO200NB6F18	V3
IO200PB6F18	W3
IO201NB6F18	T7
IO201PB6F18	U7
IO202NB6F18	V2
IO203NB6F19	W2
IO203PB6F19	Y2
IO204NB6F19	AA1
IO204PB6F19	AB1
IO205NB6F19	R6
IO205PB6F19	T6
IO206NB6F19	W1
IO206PB6F19	Y1
IO207NB6F19	T2
IO207PB6F19	U2
IO208NB6F19	T1
IO208PB6F19	U1
IO209NB6F19	AA2
IO209PB6F19	AB2
IO210NB6F19	P5
IO211NB6F19	M1
IO211PB6F19	N1
IO212NB6F19	P1
IO212PB6F19	R1
IO213NB6F19	R8
IO213PB6F19	T8
IO215NB6F20	U4

CG624	
AX1000 Function	Pin Number
IO215PB6F20	V4
IO216NB6F20	P8
IO216PB6F20	R3
IO217NB6F20	P7
IO217PB6F20	R7
IO219NB6F20	R4
IO219PB6F20	T4
IO220NB6F20	P2
IO220PB6F20	R2
IO221NB6F20	N4
IO221PB6F20	P4
IO223NB6F20	M2
IO223PB6F20	N2
IO224NB6F20	N3
IO224PB6F20	P3
Bank 7	
IO225NB7F21	J2
IO225PB7F21	J1
IO226PB7F21	G2
IO227NB7F21	H3
IO227PB7F21	H2
IO229NB7F21	K2
IO229PB7F21	L2
IO230NB7F21	K1
IO230PB7F21	L1
IO231NB7F21	E2
IO231PB7F21	F2
IO232NB7F21	F1
IO232PB7F21	G1
IO233NB7F21	L3
IO233PB7F21	M3
IO234NB7F21	D1
IO234PB7F21	E1
IO235NB7F21	K4
IO235PB7F21	L4
IO236NB7F22	M6

CG624	
AX1000 Function	Pin Number
IO237NB7F22	N8
IO237PB7F22	N7
IO238NB7F22	M5
IO239NB7F22	L6
IO239PB7F22	L5
IO240NB7F22	M4
IO241NB7F22	L7
IO241PB7F22	M7
IO242NB7F22	J3
IO243NB7F22	M9
IO243PB7F22	M8
IO244NB7F22	P9
IO244PB7F22	N6
IO245NB7F22	K8
IO245PB7F22	L8
IO246NB7F22	F3
IO246PB7F22	E3
IO247NB7F23	K7
IO247PB7F23	K6
IO248NB7F23	D2
IO249NB7F23	G4
IO249PB7F23	G3
IO251NB7F23	N10
IO251PB7F23	N9
IO253NB7F23	H4
IO253PB7F23	J4
IO255NB7F23	J6
IO255PB7F23	J5
IO257NB7F23	H5
IO257PB7F23	H6
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25

Revision	Changes	Page
Revision 3 (continued)	The timing characteristics tables from pages 2-26 to 2-60 were updated.	2-26 to 2-60
	The "Global Resources" section was updated.	2-66
	The timing characteristics tables from pages 2-102 to 2-103 were updated.	2-102 to 2-103
	The "PQ208", "FG256", and "FG324" tables are new.	3-9,3-16, 3-84

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