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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	586
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-fgg896i

Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II, Microsemi's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-109).

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Microsemi’s Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an Axcelerator design yet still achieve high performance and efficient device utilization.

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Simultaneous Switching Noise and Signal Integrity
http://www.microsemi.com/soc/documents/SSN_AN.pdf
Axcelerator Family PLL and Clock Management
http://www.microsemi.com/soc/documents/AX_PLL_AN.pdf
Implementation of Security in Actel Antifuse FPGAs
http://www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

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Antifuse Macro Library Guide
http://www.microsemi.com/soc/documents/libguide_UG.pdf
SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder
http://www.microsemi.com/soc/documents/genguide_ug.pdf
Silicon Sculptor II User’s Guide
http://www.microsemi.com/soc/documents/silisculptII_sculpt3_ug.pdf

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Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf
Understanding Actel Antifuse Device Security
http://www.microsemi.com/soc/documents/DesignSecurity_WP.pdf

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Libero IDE flow diagram
http://www.microsemi.com/soc/products/tools/libero/flow.html

The maximum power dissipation allowed for Military temperature and Mil-Std 883B devices is specified as a function of θ_{jc}.

Table 2-6 [illegible]

[illegible]	[illegible]	T [illegible]	T [illegible]	T [illegible]	T [illegible]	[illegible]
Chip Scale Package (CSP)	180	N/A	57.8	51.0	50	°C/W
Plastic Quad Flat Pack (PQFP)	208	8.0	26	23.5	20.9	°C/W
Plastic Ball Grid Array (PBGA)	729	2.2	13.7	10.6	9.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.0	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	324	3.0	25.8	22.1	20.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	208	2.0	22	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA)[2]	624	6.5	8.9	8.5	8	°C/W

Notes:

1. θ_{jc} for the 208-pin and 352-pin CQFP refers to the thermal resistance between the junction and the bottom of the package.
2. θ_{jc} for the 624-pin CCGA refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board (θ_{jb}) for CCGA 624 package is 3.4 °C/W.

[illegible]

Axcelerator devices are manufactured in a CMOS process, therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-7 should be applied to all timing data contained within this datasheet.

Table 2-7 [illegible]

[illegible]	[illegible]						
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
1.4 V	0.83	0.86	0.91	0.96	1.02	1.05	1.15
1.425 V	0.82	0.84	0.90	0.94	1.00	1.04	1.13
1.5 V	0.78	0.80	0.85	0.89	0.95	0.98	1.07
1.575 V	0.74	0.76	0.81	0.85	0.90	0.94	1.02
1.6 V	0.73	0.75	0.80	0.84	0.89	0.92	1.01

Notes:

1. The user can set the junction temperature in Designer software to be any integer value in the range of –55 °C to 175 °C.
2. The user can set the core voltage in Designer software to be any value between 1.4V and 1.6V.

All timing numbers listed in this datasheet represent sample timing characteristics of Axcelerator devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Microsemi's Designer software after place-and-route.