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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32256
Number of Logic Elements/Cells	-
Total RAM Bits	294912
Number of I/O	418
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	624-BCLGA
Supplier Device Package	624-CLGA (32.5x32.5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax2000-lg624m

Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Note that there are no tristated or bidirectional I/O buffers for differential standards.

Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users need to:

1. Instantiate an input buffer (with the required I/O standard)
2. Instantiate the DDR_REG macro (Figure 2-6)
3. Connect the output from the Input buffer to the input of the DDR macro

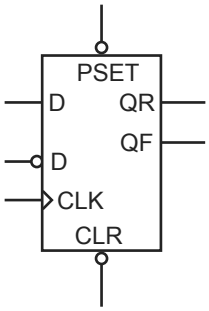


Figure 2-6 • **DDR Register**

Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required VCCI and VREF voltages for an I/O. The generic buffer macros require the LVTTL standard with slow slew rate and 24 mA-drive strength. LVTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (e.g. INBUF_LVDS) or a pair of differential outputs (e.g. OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (i.e. INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

Timing Characteristics

***Table 2-35* • 3.3 V PCI I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V PCI Output Module Timing								
t_{DP}	Input Buffer		1.57		1.79		2.10	ns
t_{PY}	Output Buffer		1.91		2.18		2.56	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

***Table 2-41* • DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCC – 0.4	8	-8

AC Loadings

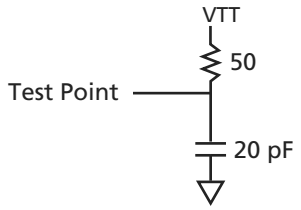


***Figure 2-20 •* AC Test Loads**

***Table 2-42* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
VREF –0.5	VREF + 0.5	VREF	0.75	20

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-43* • 1.5 V HSTL Class I I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.425 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
1.5 V HSTL Class I I/O Module Timing								
t_{DP}	Input Buffer		1.80		2.05		2.41	ns
t_{PY}	Output Buffer		4.90		5.58		6.56	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-57* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.2 – 0.125	1.2 + 0.125	1.2

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-58* • LVDS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVDS Output Module Timing								
t_{DP}	Input Buffer		1.80		2.05		2.41	ns
t_{PY}	Output Buffer		2.32		2.64		3.11	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Models and Waveforms

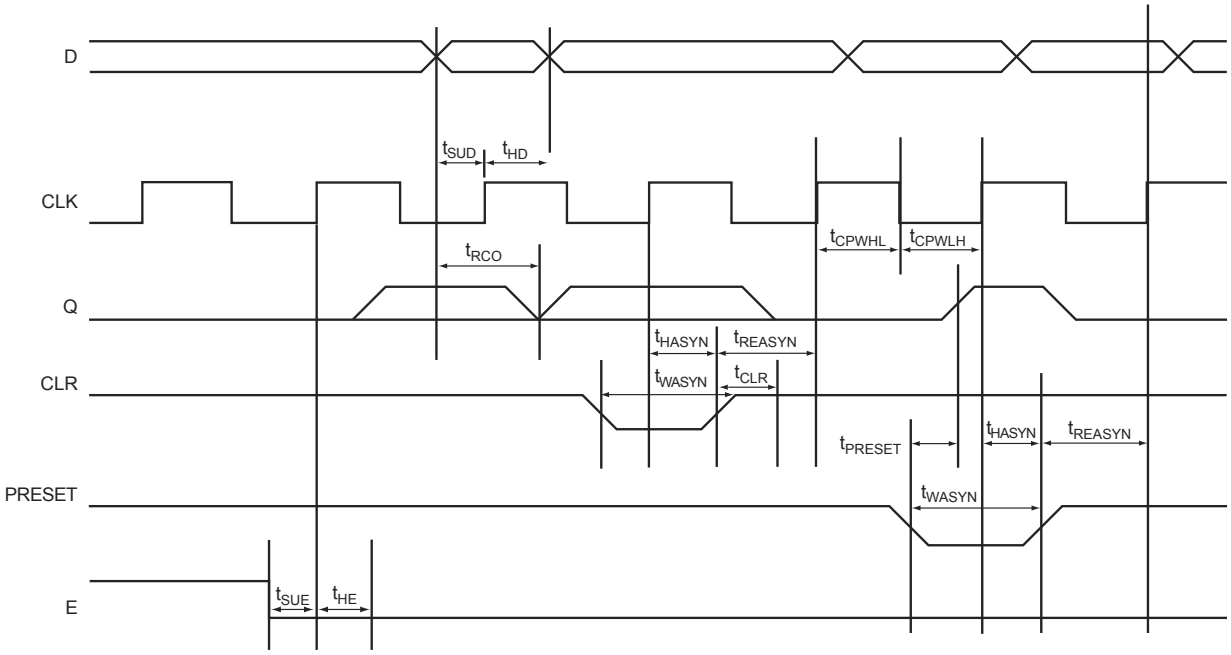


Figure 2-32 • **R-Cell Delays**

Timing Characteristics

Table 2-63 • **R-Cell**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
R-Cell Propagation Delays								
t_{RCO}	Sequential Clock-to-Q		0.67		0.77		0.90	ns
t_{CLR}	Asynchronous Clear-to-Q		0.67		0.77		0.90	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.36		0.36		0.36	ns
t_{SUD}	Flip-Flop Data Input Set-Up		0.34		0.34		0.34	ns
t_{SUE}	Flip-Flop Enable Input Set-Up		0.00		0.00		0.00	ns
t_{HD}	Flip-Flop Data Input Hold		0.67		0.77		0.90	ns
t_{HE}	Flip-Flop Enable Input Hold		0.67		0.77		0.90	ns
t_{WASYN}	Asynchronous Pulse Width	0.48		0.48		0.48		ns
t_{REASYN}	Asynchronous Recovery Time		0.23		0.27		0.31	ns
t_{HASYN}	Asynchronous Removal Time		0.36		0.36		0.36	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.36		0.36		0.36		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.36		0.36		0.36		ns

Buffer Module

Introduction

An additional resource inside each SuperCluster is the Buffer (B) module (Figure 1-4 on page 1-3). When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the AX architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium-to-high-fanout nets.

Timing Models and Waveforms

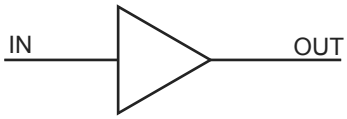


Figure 2-33 • **Buffer Module Timing Model**

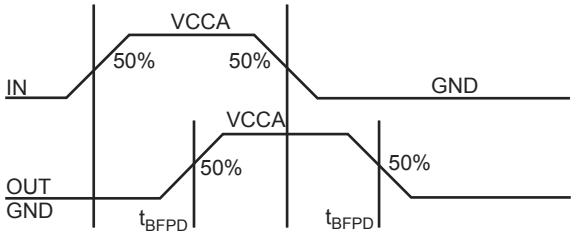


Figure 2-34 • **Buffer Module Waveform**

Timing Characteristics

Table 2-64 • **Buffer Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Buffer Module Propagation Delays								
t_{BFPD}	Any input to output Y		0.12		0.14		0.16	ns

Axcelerator Clock Management System

Introduction

Each member of the Axcelerator family[6] contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20µs

Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 µF and 10 µF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

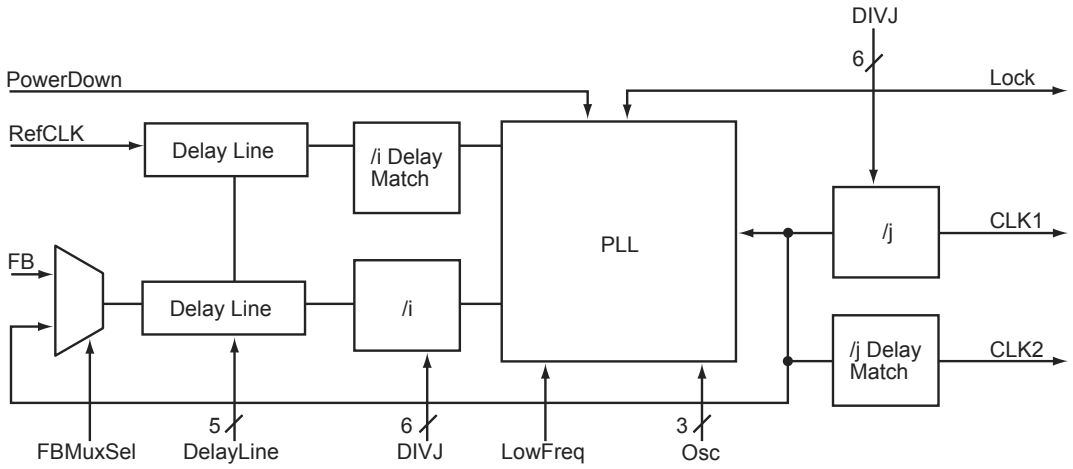


Figure 2-48 • **PLL Block Diagram**

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

6. *AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.*

***Table 2-100* • Four FIFO Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
FIFO Module Timing								
t_{WSU}	Write Setup		14.60		16.63		19.55	ns
t_{WHD}	Write Hold		0.00		0.00		0.00	ns
t_{WCKH}	WCLK High		0.75		0.75		0.75	ns
t_{WCKL}	WCLK Low		2.51		2.51		2.51	ns
t_{WCKP}	Minimum WCLK Period	3.26		3.26		3.26		ns
t_{RSU}	Read Setup		15.27		17.39		20.44	ns
t_{RHD}	Read Hold		0.00		0.00		0.00	ns
t_{RCKH}	RCLK High		0.73		0.73		0.73	ns
t_{RCKL}	RCLK Low		2.96		2.96		2.96	ns
t_{RCKP}	Minimum RCLK period	3.69		3.69		3.69		ns
t_{CLRHF}	Clear High		0.00		0.00		0.00	ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Nonpipelined)		2.83		3.23		3.79	ns

Note: Timing data for these four cascaded FIFO blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

***Table 2-102* • Sixteen FIFO Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
FIFO Module Timing								
t_{WSU}	Write Setup		16.32		18.60		21.86	ns
t_{WHD}	Write Hold		0.00		0.00		0.00	ns
t_{WCKH}	WCLK High		0.75		0.75		0.75	ns
t_{WCKL}	WCLK Low		13.40		13.40		13.40	ns
t_{WCKP}	Minimum WCLK Period	14.15		14.15		14.15		ns
t_{RSU}	Read Setup		17.16		19.54		22.97	ns
t_{RHD}	Read Hold		0.00		0.00		0.00	ns
t_{RCKH}	RCLK High		0.73		0.73		0.73	ns
t_{RCKL}	RCLK Low		14.41		14.41		14.41	ns
t_{RCKP}	Minimum RCLK period	15.14		15.14		15.14		ns
t_{CLRHF}	Clear High		0.00		0.00		0.00	ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Nonpipelined)		12.83		14.62		17.18	ns

Note: Timing data for these sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen Core Generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (refer to the *SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder* User's Guide for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Low Power Mode

Although designed for high performance, the AX architecture also allows the user to place the device into a low power mode. Each I/O bank in an Axcelerator device can be configured individually, when in low power mode, to tristate all outputs, disable inputs, or both. The low power mode is activated by asserting the LP pin, which is grounded in normal operation.

While in the low power mode, the device is still fully functional and all internal logic states are preserved. This allows a user to disable all but a few signals and operate the part in a low-frequency, watchdog

FG484	
AX1000 Function	**Pin Number**
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	AB16
VCCDA	AB8
VCCDA	C10
VCCDA	C11
VCCDA	C14
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX1000 Function	**Pin Number**
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX1000 Function	**Pin Number**
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG676	
AX500 Function	Pin Number
NC	J5
NC	J6
NC	P22
NC	R20
NC	R21
NC	R22
NC	R4
NC	R5
NC	T22
NC	T24
NC	U22
NC	U24
NC	V22
NC	V5
NC	W21
NC	W22
NC	W5
NC	W6
NC	Y21
NC	Y4
NC	Y5
NC	Y6
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26

FG676	
AX500 Function	Pin Number
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14
VCCA	V15
VCCA	V16
VCCA	V17
VCCDA	A3
VCCDA	AB22
VCCDA	AB5

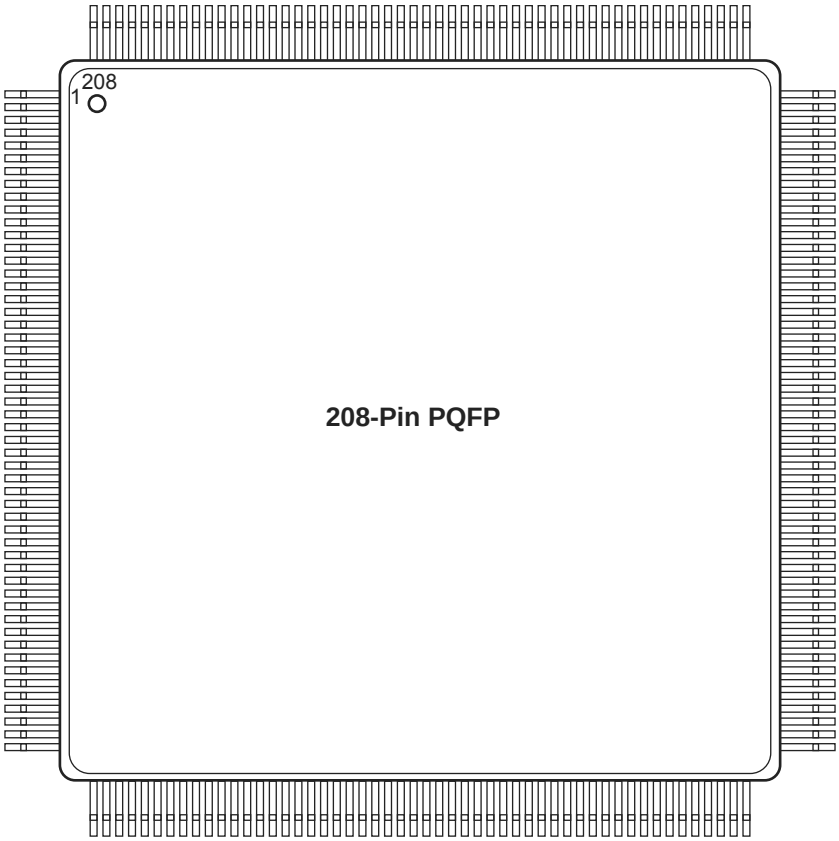
FG676	
AX500 Function	Pin Number
VCCDA	AD10
VCCDA	AD13
VCCDA	AD17
VCCDA	B1
VCCDA	B17
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23
VCCIB0	G10
VCCIB0	G8
VCCIB0	G9
VCCIB0	H10
VCCIB0	H11
VCCIB0	H12
VCCIB0	H13
VCCIB0	H9
VCCIB1	G17
VCCIB1	G18
VCCIB1	G19
VCCIB1	H14
VCCIB1	H15
VCCIB1	H16
VCCIB1	H17
VCCIB1	H18
VCCIB2	H20
VCCIB2	J19
VCCIB2	J20
VCCIB2	K19
VCCIB2	K20
VCCIB2	L19
VCCIB2	M19
VCCIB2	N19
VCCIB3	P19
VCCIB3	R19

FG676	
AX1000 Function	**Pin Number**
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26
IO73PB2F6	D26
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23

FG676	
AX1000 Function	**Pin Number**
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
Bank 3	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24
IO100NB3F9	R22
IO100PB3F9	P22
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25

FG676	
AX1000 Function	**Pin Number**
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
Bank 4	
IO129NB4F12	AB21

PQ208



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

PQ208	
AX250 Function	**Pin Number**
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	**Pin Number**
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX250 Function	**Pin Number**
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ256	
AX2000 Function	**Pin Number**
VCCA	4
VCCA	22
VCCA	42
VCCA	61
VCCA	63
VCCA	84
VCCA	108
VCCA	127
VCCA	131
VCCA	150
VCCA	170
VCCA	189
VCCA	191
VCCA	212
VCCA	238
VCCDA	2
VCCDA	32
VCCDA	66
VCCDA	67
VCCDA	86
VCCDA	87
VCCDA	94
VCCDA	95
VCCDA	96
VCCDA	106
VCCDA	107
VCCDA	126
VCCDA	130
VCCDA	160
VCCDA	194
VCCDA	196
VCCDA	214
VCCDA	215
VCCDA	222
VCCDA	223

CQ256	
AX2000 Function	**Pin Number**
VCCDA	224
VCCDA	236
VCCDA	237
VCCDA	251
VCCIB0	230
VCCIB0	244
VCCIB1	200
VCCIB1	206
VCCIB1	218
VCCIB2	164
VCCIB2	176
VCCIB2	182
VCCIB3	138
VCCIB3	144
VCCIB3	156
VCCIB4	102
VCCIB4	114
VCCIB4	120
VCCIB5	72
VCCIB5	78
VCCIB5	90
VCCIB6	36
VCCIB6	48
VCCIB6	54
VCCIB7	10
VCCIB7	16
VCCIB7	28
VPUMP	195

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15

CQ352	
AX2000 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX2000 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114

CQ352	
AX2000 Function	Pin Number
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	91
VCCDA	116
VCCDA	117
VCCDA	130
VCCDA	131
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	174
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	268
VCCDA	293
VCCDA	294
VCCDA	307
VCCDA	308
VCCDA	309
VCCDA	327
VCCDA	328

CG624	
AX1000 Function	Pin Number
IO194NB6F18	Y3
IO194PB6F18	AA3
IO195NB6F18	V6
IO195PB6F18	W4
IO197NB6F18	R5
IO197PB6F18	U3
IO198NB6F18	P6
IO199NB6F18	Y5
IO199PB6F18	W5
IO200NB6F18	V3
IO200PB6F18	W3
IO201NB6F18	T7
IO201PB6F18	U7
IO202NB6F18	V2
IO203NB6F19	W2
IO203PB6F19	Y2
IO204NB6F19	AA1
IO204PB6F19	AB1
IO205NB6F19	R6
IO205PB6F19	T6
IO206NB6F19	W1
IO206PB6F19	Y1
IO207NB6F19	T2
IO207PB6F19	U2
IO208NB6F19	T1
IO208PB6F19	U1
IO209NB6F19	AA2
IO209PB6F19	AB2
IO210NB6F19	P5
IO211NB6F19	M1
IO211PB6F19	N1
IO212NB6F19	P1
IO212PB6F19	R1
IO213NB6F19	R8
IO213PB6F19	T8
IO215NB6F20	U4

CG624	
AX1000 Function	Pin Number
IO215PB6F20	V4
IO216NB6F20	P8
IO216PB6F20	R3
IO217NB6F20	P7
IO217PB6F20	R7
IO219NB6F20	R4
IO219PB6F20	T4
IO220NB6F20	P2
IO220PB6F20	R2
IO221NB6F20	N4
IO221PB6F20	P4
IO223NB6F20	M2
IO223PB6F20	N2
IO224NB6F20	N3
IO224PB6F20	P3
Bank 7	
IO225NB7F21	J2
IO225PB7F21	J1
IO226PB7F21	G2
IO227NB7F21	H3
IO227PB7F21	H2
IO229NB7F21	K2
IO229PB7F21	L2
IO230NB7F21	K1
IO230PB7F21	L1
IO231NB7F21	E2
IO231PB7F21	F2
IO232NB7F21	F1
IO232PB7F21	G1
IO233NB7F21	L3
IO233PB7F21	M3
IO234NB7F21	D1
IO234PB7F21	E1
IO235NB7F21	K4
IO235PB7F21	L4
IO236NB7F22	M6

CG624	
AX1000 Function	Pin Number
IO237NB7F22	N8
IO237PB7F22	N7
IO238NB7F22	M5
IO239NB7F22	L6
IO239PB7F22	L5
IO240NB7F22	M4
IO241NB7F22	L7
IO241PB7F22	M7
IO242NB7F22	J3
IO243NB7F22	M9
IO243PB7F22	M8
IO244NB7F22	P9
IO244PB7F22	N6
IO245NB7F22	K8
IO245PB7F22	L8
IO246NB7F22	F3
IO246PB7F22	E3
IO247NB7F23	K7
IO247PB7F23	K6
IO248NB7F23	D2
IO249NB7F23	G4
IO249PB7F23	G3
IO251NB7F23	N10
IO251PB7F23	N9
IO253NB7F23	H4
IO253PB7F23	J4
IO255NB7F23	J6
IO255PB7F23	J5
IO257NB7F23	H5
IO257PB7F23	H6
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25

Revision	Changes	Page
Revision 3 (continued)	The timing characteristics tables from pages 2-26 to 2-60 were updated.	2-26 to 2-60
	The "Global Resources" section was updated.	2-66
	The timing characteristics tables from pages 2-102 to 2-103 were updated.	2-102 to 2-103
	The "PQ208", "FG256", and "FG324" tables are new.	3-9,3-16, 3-84