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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	115
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-1cq208m

Two C-cells, a single R-cell, two Transmit (TX), and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

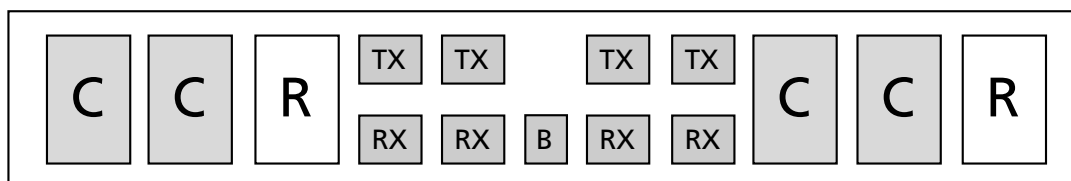


Figure 1-4 • AX SuperCluster

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

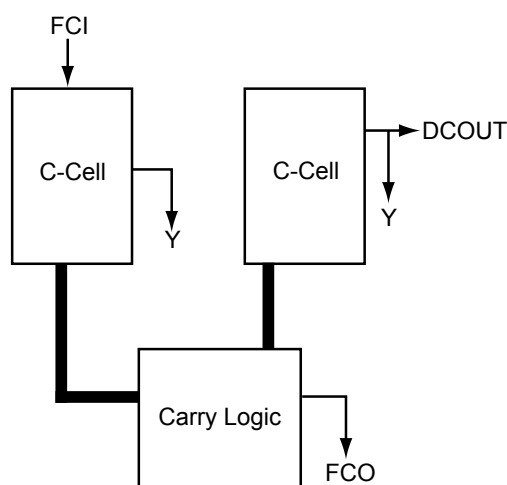


Figure 1-5 • AX 2-Bit Carry Logic

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the AX1000 is composed of a 3x3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1). Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the AX250).

Table 1-1 • Number of Core Tiles per Device

Device	Number of Core Tiles
AX125	1 regular tile
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

SSTL2

Stub Series Terminated Logic for 2.5 V is a general-purpose 2.5 V memory bus standard (JESD8-9). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-44 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF - 0.2	VREF + 0.2	3.6	VREF - 0.57	VREF + 0.57	7.6	-7.6

AC Loadings

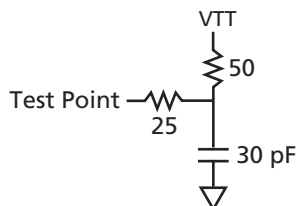


Figure 2-21 • AC Test Loads

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF - 0.75	VREF + 0.75	VREF	1.25	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-46 • 2.5 V SSTL2 Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		-2 Speed		-1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V SSTL2 Class I I/O Module Timing								
t _{DP}	Input Buffer		1.83		2.08		2.45	ns
t _{PY}	Output Buffer		2.39		2.72		3.20	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Models and Waveforms

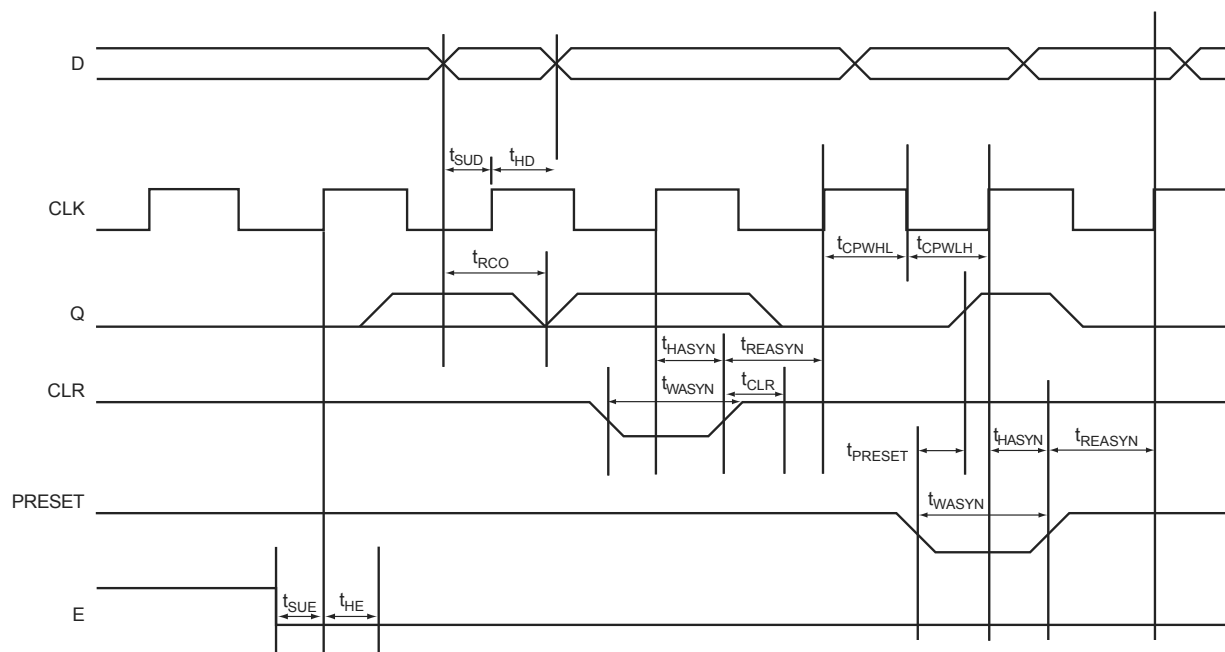


Figure 2-32 • R-Cell Delays

Timing Characteristics

Table 2-63 • R-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
R-Cell Propagation Delays								
t _{RCO}	Sequential Clock-to-Q		0.67		0.77		0.90	ns
t _{CLR}	Asynchronous Clear-to-Q		0.67		0.77		0.90	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.36		0.36		0.36	ns
t _{SUD}	Flip-Flop Data Input Set-Up		0.34		0.34		0.34	ns
t _{SUE}	Flip-Flop Enable Input Set-Up		0.00		0.00		0.00	ns
t _{HD}	Flip-Flop Data Input Hold		0.67		0.77		0.90	ns
t _{HE}	Flip-Flop Enable Input Hold		0.67		0.77		0.90	ns
t _{WASYN}	Asynchronous Pulse Width	0.48		0.48		0.48		ns
t _{REASYN}	Asynchronous Recovery Time		0.23		0.27		0.31	ns
t _{HASYN}	Asynchronous Removal Time		0.36		0.36		0.36	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.36		0.36		0.36		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.36		0.36		0.36		ns

Table 2-77 • AX500 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		2.31		2.63		3.09	ns
t _{RCKH}	Input High to Low		2.44		2.78		3.27	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-78 • AX1000 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-79 • AX2000 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-92 • Eight RAM Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t _{WDASU}	Write Data Setup vs. WCLK		5.78		6.58		7.74	ns
t _{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WADSU}	Write Address Setup vs. WCLK		5.78		6.58		7.74	ns
t _{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WENSU}	Write Enable Setup vs. WCLK		5.78		6.58		7.74	ns
t _{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t _{WCLK}	WCLK Minimum Low Pulse Width	5.13		5.13		5.13		ns
t _{WCKP}	WCLK Minimum Period	5.88		5.88		5.88		ns
Read Mode								
t _{RADSU}	Read Address Setup vs. RCLK		6.75		7.69		9.04	ns
t _{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RENSU}	Read Enable Setup vs. RCLK		6.75		7.69		9.04	ns
t _{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		3.39		3.86		4.54	ns
t _{RCK2RD2}	RCLK-To-OUT (Non-Pipelined)		4.93		5.62		6.61	ns
t _{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t _{RCLKL}	RCLK Minimum Low Pulse Width	5.77		5.77		5.77		ns
t _{RCKP}	RCLK Minimum Period	6.50		6.50		6.50		ns

Note: Timing data for these eight cascaded RAM blocks uses a depth of 32,768. For all other combinations, use Microsemi's timing software.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

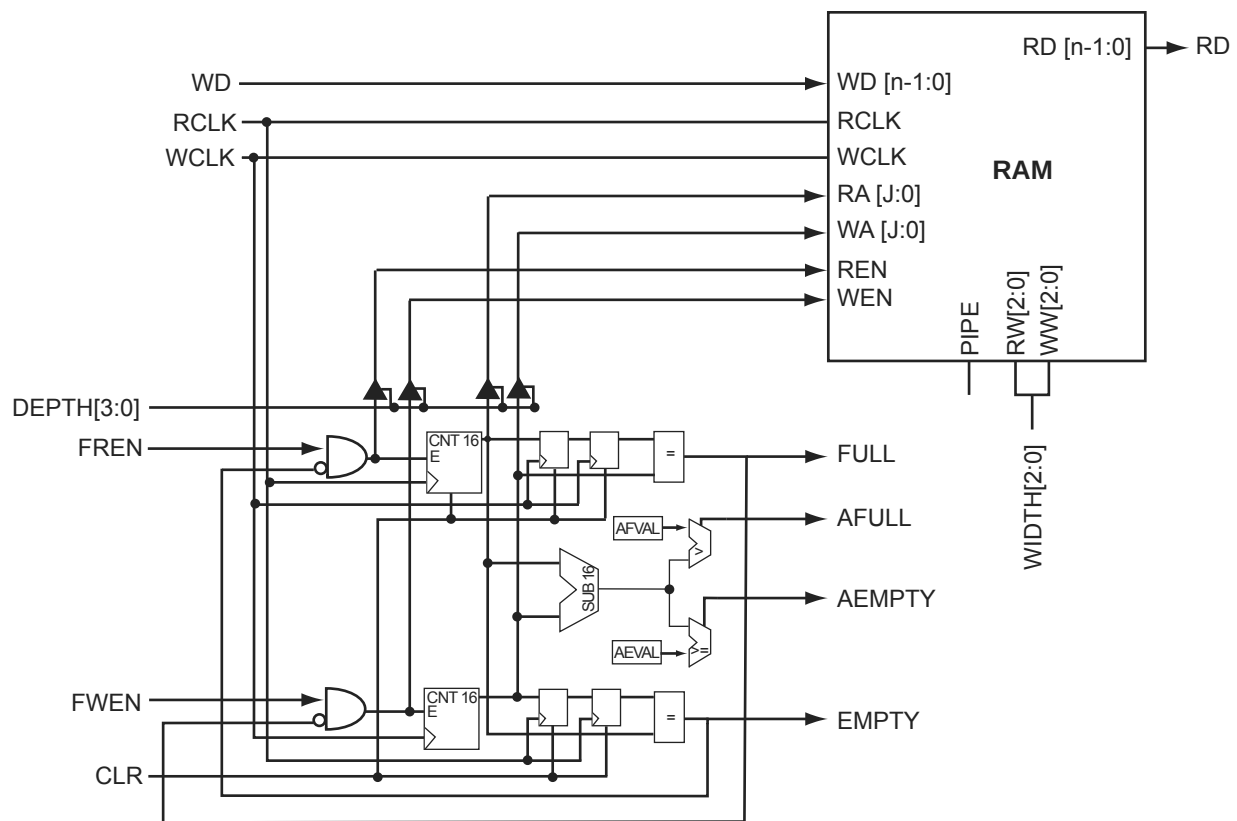


Figure 2-61 • Axcelerator RAM with Embedded FIFO Controller

FG484	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	E3
IO00PB0F0	D3
IO01NB0F0	E7
IO01PB0F0	E6
IO02NB0F0	C5
IO02PB0F0	C4
IO03NB0F0	D7
IO03PB0F0	D6
IO04NB0F0	B5
IO04PB0F0	B4
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	A5
IO06PB0F0	A4
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	B7
IO08PB0F0	B6
IO10NB0F0	B9
IO10PB0F0	B8
IO11NB0F0	E9
IO11PB0F0	E8
IO12NB0F1	D9
IO12PB0F1	D8
IO13NB0F1	C9
IO13PB0F1	C8
IO14NB0F1	A9
IO14PB0F1	A8
IO15NB0F1	B10
IO15PB0F1	A10
IO16NB0F1	B12
IO16PB0F1	B11
IO18NB0F1	C13
IO18PB0F1	C12

FG484	
AX500 Function	Pin Number
IO19NB0F1/HCLKAN	E11
IO19PB0F1/HCLKAP	E10
IO20NB0F1/HCLKBN	D12
IO20PB0F1/HCLKBP	D11
Bank 1	
IO21NB1F2/HCLKCN	F13
IO21PB1F2/HCLKCP	F12
IO22NB1F2/HCLKDN	E14
IO22PB1F2/HCLKDP	E13
IO24NB1F2	A14
IO24PB1F2	A13
IO25NB1F2	B14
IO25PB1F2	B13
IO26NB1F2	C15
IO27NB1F2	A16
IO27PB1F2	A15
IO28NB1F2	B16
IO28PB1F2	B15
IO29NB1F2	D16
IO29PB1F2	D15
IO30NB1F2	A18
IO30PB1F2	A17
IO31NB1F2	F15
IO31PB1F2	F14
IO32NB1F3	C17
IO32PB1F3	C16
IO33NB1F3	E16
IO33PB1F3	E15
IO34NB1F3	B18
IO34PB1F3	B17
IO35NB1F3	B19
IO35PB1F3	A19
IO36NB1F3	C19
IO36PB1F3	C18
IO37NB1F3	F18

FG484	
AX500 Function	Pin Number
IO37PB1F3	F17
IO38NB1F3	D18
IO38PB1F3	E17
IO39NB1F3	E21
IO39PB1F3	D21
IO40NB1F3	E20
IO40PB1F3	D20
IO41NB1F3	G16
IO41PB1F3	G15
Bank 2	
IO42NB2F4	F19
IO42PB2F4	E19
IO43NB2F4	J16
IO43PB2F4	H16
IO44NB2F4	E22
IO44PB2F4	D22
IO45NB2F4	H19
IO45PB2F4	G19
IO46NB2F4	G22
IO46PB2F4	F22
IO47NB2F4	J17
IO47PB2F4	H17
IO48NB2F4	G20
IO48PB2F4	F20
IO49NB2F4	J18
IO49PB2F4	H18
IO50NB2F4	G21
IO50PB2F4	F21
IO51NB2F4	K19
IO51PB2F4	J19
IO52NB2F5	J21
IO52PB2F5	H21
IO53NB2F5	J20
IO53PB2F5	H20
IO54NB2F5	J22

FG484	
AX500 Function	Pin Number
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	Pin Number
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	Pin Number
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG676	
AX500 Function	Pin Number
IO51NB2F4	L20
IO51PB2F4	L21
IO52NB2F5	K26
IO52PB2F5	J26
IO53NB2F5	L23
IO53PB2F5	L22
IO54NB2F5	L24
IO54PB2F5	K24
IO55NB2F5	M20
IO55PB2F5	M21
IO56NB2F5	L26
IO56PB2F5	L25
IO57NB2F5	M23
IO57PB2F5	M22
IO58NB2F5	M26
IO58PB2F5	M25
IO59NB2F5	N22
IO59PB2F5	N23
IO60NB2F5	N24
IO60PB2F5	M24
IO61NB2F5	N20
IO61PB2F5	N21
IO62NB2F5	P25
IO62PB2F5	N25
Bank 3	
IO63NB3F6	T26
IO63PB3F6	R26
IO64NB3F6	R24
IO64PB3F6	P24
IO65NB3F6	P20
IO65PB3F6	P21
IO66NB3F6	T25
IO66PB3F6	R25
IO67NB3F6	T23
IO67PB3F6	R23

FG676	
AX500 Function	Pin Number
IO68NB3F6	V26
IO68PB3F6	U26
IO69NB3F6	V25
IO69PB3F6	U25
IO70NB3F6	Y25
IO70PB3F6	W25
IO71NB3F6	W24
IO71PB3F6	V24
IO72NB3F6	V23
IO72PB3F6	U23
IO73NB3F6	T21
IO73PB3F6	T20
IO74NB3F7	AA26
IO74PB3F7	Y26
IO75NB3F7	AA24
IO75PB3F7	Y24
IO76NB3F7	Y23
IO76PB3F7	W23
IO77NB3F7	V21
IO77PB3F7	U21
IO78NB3F7	AB25
IO78PB3F7	AA25
IO79NB3F7	AC26
IO79PB3F7	AB26
IO80NB3F7	AC24
IO80PB3F7	AB24
IO81NB3F7	AB23
IO81PB3F7	AA23
IO82NB3F7	AA22
IO82PB3F7	Y22
IO83NB3F7	AE26
IO83PB3F7	AD26
Bank 4	
IO84NB4F8	AB21
IO84PB4F8	AA21

FG676	
AX500 Function	Pin Number
IO85NB4F8	AE23
IO85PB4F8	AE24
IO86NB4F8	AC21
IO86PB4F8	AC22
IO87NB4F8	AF22
IO87PB4F8	AF23
IO88NB4F8	AD22
IO88PB4F8	AD23
IO89NB4F8	AC19
IO89PB4F8	AC20
IO90NB4F8	AE21
IO90PB4F8	AE22
IO91NB4F8	AA17
IO91PB4F8	AA18
IO92NB4F8	AD20
IO92PB4F8	AD21
IO93NB4F8	AF20
IO93PB4F8	AF21
IO94NB4F9	AE19
IO94PB4F9	AE20
IO95NB4F9	AC17
IO95PB4F9	AC18
IO96NB4F9	AD18
IO96PB4F9	AD19
IO97NB4F9	AA16
IO97PB4F9	Y16
IO98NB4F9	AE17
IO98PB4F9	AE18
IO99NB4F9	AC16
IO99PB4F9	AB16
IO100NB4F9	AF17
IO100PB4F9	AF18
IO101NB4F9	AA15
IO101PB4F9	Y15
IO102NB4F9	AC15

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896	
AX1000 Function	Pin Number
IO206PB6F19	AB4
IO207NB6F19	W6
IO207PB6F19	W7
IO208NB6F19	AB3
IO208PB6F19	AC3
IO209NB6F19	V8
IO209PB6F19	V9
IO210NB6F19	AA2
IO210PB6F19	AA1
IO211NB6F19	V5
IO211PB6F19	W5
IO212NB6F19	Y3
IO212PB6F19	Y4
IO213NB6F19	V7
IO213PB6F19	V6
IO214NB6F20	W3
IO214PB6F20	W4
IO215NB6F20	U8
IO215PB6F20	U9
IO216NB6F20	W1
IO216PB6F20	W2
IO217NB6F20	U7
IO217PB6F20	U6
IO218NB6F20	U4
IO218PB6F20	V4
IO219NB6F20	T5
IO219PB6F20	U5
IO220NB6F20	U3
IO220PB6F20	V3
IO221NB6F20	T8
IO221PB6F20	T9
IO222NB6F20	U2
IO222PB6F20	V2
IO223NB6F20	T7
IO223PB6F20	T6

FG896	
AX1000 Function	Pin Number
IO224NB6F20	R2
IO224PB6F20	T2
Bank 7	
IO225NB7F21	R7
IO225PB7F21	R6
IO226NB7F21	R4
IO226PB7F21	R5
IO227NB7F21	R8
IO227PB7F21	R9
IO228NB7F21	P1
IO228PB7F21	R1
IO229NB7F21	P9
IO229PB7F21	P8
IO230NB7F21	N2
IO230PB7F21	P2
IO231NB7F21	P7
IO231PB7F21	P6
IO232NB7F21	N3
IO232PB7F21	P3
IO233NB7F21	P4
IO233PB7F21	P5
IO234NB7F21	L1
IO234PB7F21	M1
IO235NB7F21	M4
IO235PB7F21	N4
IO236NB7F22	N7
IO236PB7F22	N6
IO237NB7F22	N8
IO237PB7F22	N9
IO238NB7F22	M5
IO238PB7F22	N5
IO239NB7F22	L2
IO239PB7F22	M2
IO240NB7F22	L3
IO240PB7F22	M3

FG896	
AX1000 Function	Pin Number
IO241NB7F22	M8
IO241PB7F22	M7
IO242NB7F22	K4
IO242PB7F22	L4
IO243NB7F22	L6
IO243PB7F22	M6
IO244NB7F22	K5
IO244PB7F22	L5
IO245NB7F22	J4
IO245PB7F22	J3
IO246NB7F22	G2
IO246PB7F22	H2
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	G3
IO248PB7F23	H3
IO249NB7F23	G4
IO249PB7F23	H4
IO250NB7F23	J6
IO250PB7F23	K6
IO251NB7F23	H5
IO251PB7F23	J5
IO252NB7F23	F2
IO252PB7F23	F1
IO253NB7F23	K8
IO253PB7F23	K7
IO254NB7F23	F4
IO254PB7F23	F3
IO255NB7F23	G6
IO255PB7F23	H6
IO256NB7F23	F5
IO256PB7F23	G5
IO257NB7F23	H7
IO257PB7F23	J7
Dedicated I/O	

FG896	
AX1000 Function	Pin Number
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

FG896	
AX1000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX1000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	Pin Number
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
Bank 3	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26

FG896	
AX2000 Function	Pin Number
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27

FG896	
AX2000 Function	Pin Number
IO163NB3F15	AC26
IO163PB3F15	AB26
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23
IO170PB3F15	AA23
Bank 4	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23

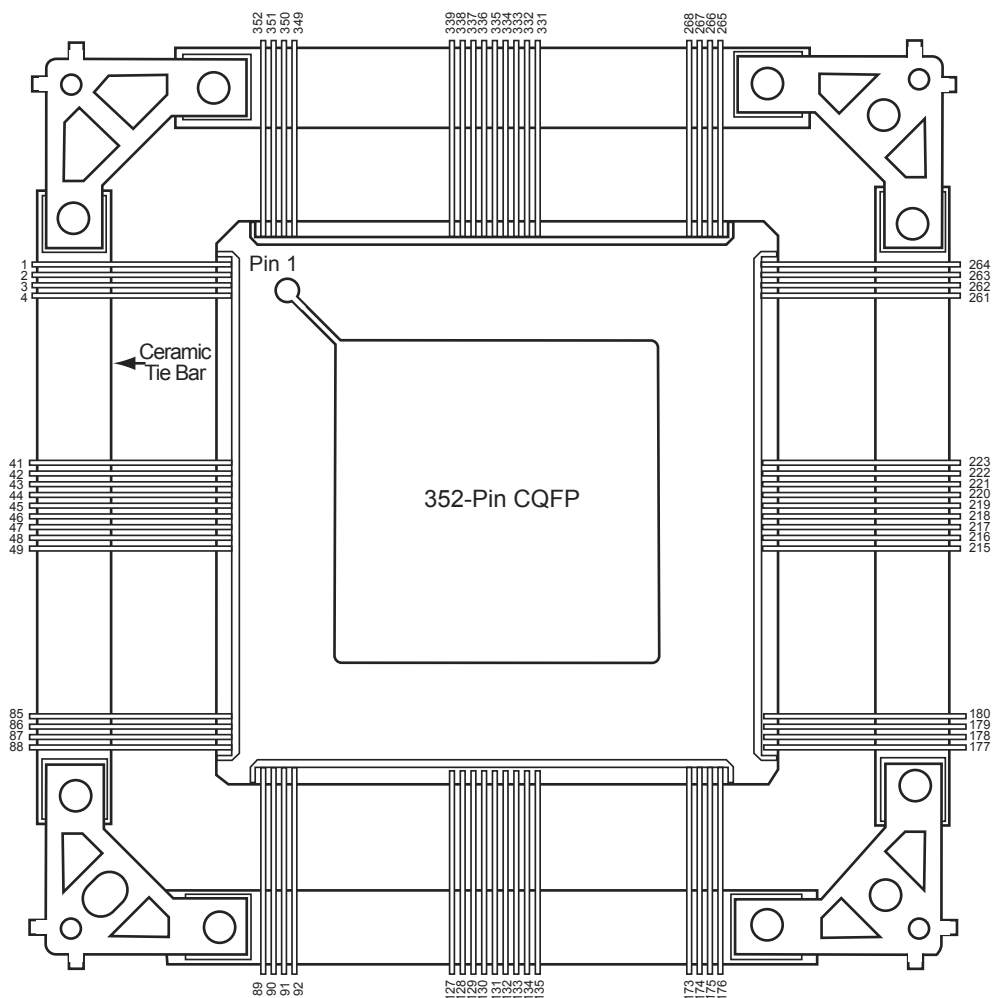
FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO207PB4F19	AL20	IO224PB5F21	AP14	IO242NB5F22	AG11
IO208NB4F19	AG19	IO225NB5F21	AK13	IO242PB5F22	AG12
IO208PB4F19	AF19	IO225PB5F21	AK14	IO243NB5F22	AL9
IO209NB4F19	AN18	IO226NB5F21	AE15	IO243PB5F22	AL10
IO209PB4F19	AP18	IO226PB5F21	AF15	IO244NB5F22	AM8
IO210NB4F19	AE19	IO227NB5F21	AG14	IO244PB5F22	AM9
IO210PB4F19	AD19	IO227PB5F21	AG15	IO245NB5F23	AH10
IO211NB4F19	AL18	IO228NB5F21	AJ13	IO245PB5F23	AJ10
IO211PB4F19	AM18	IO228PB5F21	AJ14	IO246NB5F23	AF10
IO212NB4F19/CLKEN	AJ20	IO229NB5F21	AM13	IO246PB5F23	AF11
IO212PB4F19/CLKEP	AK20	IO229PB5F21	AM14	IO247NB5F23	AJ9
IO213NB4F19/CLKFN	AJ18	IO230NB5F21	AE14	IO247PB5F23	AK9
IO213PB4F19/CLKFP	AJ19	IO230PB5F21	AF14	IO248NB5F23	AN7
Bank 5		IO231NB5F21	AN12	IO248PB5F23	AP7
IO214NB5F20/CLKGN	AJ16	IO231PB5F21	AP12	IO249NB5F23	AL7
IO214PB5F20/CLKGP	AJ17	IO232NB5F21	AG13	IO249PB5F23	AL8
IO215NB5F20/CLKHN	AJ15	IO232PB5F21	AH13	IO250NB5F23	AE10
IO215PB5F20/CLKHP	AK15	IO233NB5F21	AL12	IO250PB5F23	AE11
IO216NB5F20	AD16	IO233PB5F21	AL13	IO251NB5F23	AK8
IO216PB5F20	AE17	IO234NB5F21	AE13	IO251PB5F23	AJ8
IO217NB5F20	AM17	IO234PB5F21	AF13	IO252NB5F23	AH8
IO217PB5F20	AL17	IO235NB5F22	AN11	IO252PB5F23	AH9
IO218NB5F20	AG16	IO235PB5F22	AP11	IO253NB5F23	AN6
IO218PB5F20	AF16	IO236NB5F22	AM11	IO253PB5F23	AP6
IO219NB5F20	AM16	IO236PB5F22	AM12	IO254NB5F23	AG9
IO219PB5F20	AL16	IO237NB5F22	AJ11	IO254PB5F23	AG10
IO220NB5F20	AP16	IO237PB5F22	AJ12	IO255NB5F23	AJ7
IO220PB5F20	AN16	IO238NB5F22	AH11	IO255PB5F23	AK7
IO221NB5F20	AN15	IO238PB5F22	AH12	IO256NB5F23	AL6
IO221PB5F20	AP15	IO239NB5F22	AK10	IO256PB5F23	AM6
IO222NB5F20	AD15	IO239PB5F22	AK11	Bank 6	
IO222PB5F20	AE16	IO240NB5F22	AE12	IO257NB6F24	AG6
IO223NB5F21	AL14	IO240PB5F22	AF12	IO257PB6F24	AH6
IO223PB5F21	AL15	IO241NB5F22	AN10	IO258NB6F24	AD9
IO224NB5F21	AN14	IO241PB5F22	AP10	IO258PB6F24	AE9

CQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

CQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

CQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ352



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CQ352	
AX500 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX500 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO63PB1F5	G18	IO84NB2F7	M20	IO105NB3F9	R23
Bank 2		IO84PB2F7	M21	IO105PB3F9	P23
IO64NB2F6	M17	IO86NB2F8	E25	IO106NB3F9	R19
IO64PB2F6	G22	IO86PB2F8	D25	IO106PB3F9	R20
IO65NB2F6	J21	IO87NB2F8	L24	IO107NB3F10	AB24
IO65PB2F6	J20	IO87PB2F8	K24	IO108NB3F10	R25
IO66NB2F6	L23	IO88NB2F8	G24	IO108PB3F10	P25
IO66PB2F6	K20	IO88PB2F8	F24	IO109NB3F10	U25
IO67NB2F6	F23	IO89NB2F8	J25	IO109PB3F10	T25
IO67PB2F6	E23	IO90NB2F8	G25	IO110NB3F10	U24
IO68NB2F6	L18	IO90PB2F8	F25	IO110PB3F10	U23
IO68PB2F6	K18	IO91NB2F8	L25	IO112NB3F10	T24
IO70NB2F6	E24	IO91PB2F8	K25	IO112PB3F10	R24
IO70PB2F6	D24	IO92NB2F8	J24	IO113NB3F10	Y25
IO71NB2F6	H23	IO92PB2F8	H24	IO113PB3F10	W25
IO71PB2F6	G23	IO93PB2F8	J23	IO114NB3F10	V23
IO72NB2F6	L19	IO94NB2F8	N24	IO114PB3F10	V24
IO72PB2F6	K19	IO94PB2F8	M24	IO116NB3F10	AA24
IO74NB2F7	J22	IO95NB2F8	N25	IO116PB3F10	Y24
IO74PB2F7	H22	IO95PB2F8	M25	IO117NB3F10	AB25
IO75NB2F7	N23	Bank 3		IO117PB3F10	AA25
IO75PB2F7	M23	IO96NB3F9	T18	IO118NB3F11	T20
IO76NB2F7	N17	IO96PB3F9	R18	IO118PB3F11	R21
IO76PB2F7	N16	IO97NB3F9	N20	IO120NB3F11	W22
IO77NB2F7	L22	IO97PB3F9	P24	IO120PB3F11	W23
IO77PB2F7	K22	IO98NB3F9	P20	IO122NB3F11	V22
IO78NB2F7	M19	IO98PB3F9	P19	IO122PB3F11	U22
IO78PB2F7	M18	IO99NB3F9	P21	IO124NB3F11	Y23
IO79NB2F7	N19	IO100NB3F9	T22	IO124PB3F11	AA23
IO79PB2F7	N18	IO100PB3F9	W24	IO126NB3F11	V21
IO80NB2F7	L21	IO101NB3F9	R22	IO126PB3F11	U21
IO80PB2F7	L20	IO101PB3F9	P22	IO128NB3F11	Y22
IO82NB2F7	P18	IO102NB3F9	U19	IO128PB3F11	Y21
IO82PB2F7	P17	IO102PB3F9	T19	Bank 4	
IO83NB2F7	N22	IO104NB3F9	V20	IO129NB4F12	W20
IO83PB2F7	M22	IO104PB3F9	U20	IO129PB4F12	Y20

Revision	Changes	Page
Revision 12 (v2.4)	Revised ordering information and timing data to reflect phase out of –3 speed grade options.	
	Table 2-3 was updated.	2
Revision 11 (v2.3)	The "Packaging Data" section is new.	iv
	Table 2-2 was updated.	2-1
	"VCCDA Supply Voltage" was updated.	2-9
	"PRA/B/C/D Probe A, B, C and D" was updated.	2-10
	The "User I/Os" was updated.	2-11
Revision 10 (v2.2)	Figure 1-3 was updated.	1-2
	Table 2-2 was updated.	2-1
	The "Power-Up/Down Sequence" section was updated.	2-1
	Table 2-4 was updated.	2-3
	Table 2-5 was updated.	2-4
	The "Timing Characteristics" section was added.	2-7
	Table 2-7 was updated.	2-7
	Figure 2-1 was updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) equations in the "Hardwired Clock – Using LVTTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) in the "Routed Clock – Using LVTTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The "Global Pins" section was updated.	2-10
	The "User I/Os" section was updated.	2-11
	Table 2-17 was updated.	2-19
	Figure 2-8 was updated.	2-20
	Figure 2-13 and Figure 2-14 were updated.	2-24
	The following timing parameters were renamed in I/O timing characteristic tables from Table 2-22 to Table 2-60: $t_{IOCLKQ} > t_{CLKQ}$ $t_{IOCLKY} > t_{OCLKQ}$	2-26 to 2-52
	Timing numbers were updated from Table 2-22 to Table 2-78.	2-26 to 2-69
	The "R-Cell" section was updated.	2-58
	Figure 2-59 was updated.	2-89
	Figure 2-60 was updated.	2-89
	Figure 2-67 was updated.	2-100
	Figure 2-68 was updated.	2-101
	Table 2-89 to Table 2-93 were updated.	2-90 to 2-94
	Table 2-98 to Table 2-102 were updated.	2-102 to 2-106

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Axcelerator Family Device Status" table on page iii, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.