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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	138
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-1fgg256i

Table 2-8 • I/O Standards Supported by the Axcelerator Family

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVC MOS 2.5 V	2.5	N/A	N/A
LVC MOS 1.8 V	1.8	N/A	N/A
LVC MOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Note: *2.5 V GTL+ is not supported across the full military temperature range.

Table 2-9 • Supply Voltages

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5 V	1.5 V	3.3 V	1.5 V
1.5 V	1.8 V	3.3 V	1.8 V
1.5 V	2.5 V	3.3 V	2.5 V
1.5 V	3.3 V	3.3 V	3.3 V

Table 2-10 • I/O Features Comparison

I/O Assignment	Clamp Diode	Hot Insertion	5 V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes ¹	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes ^{1, 2}	Enabled/Disabled	
LVC MOS 2.5 V	No	Yes	No	Enabled/Disabled	
LVC MOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVC MOS 1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled ³
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled ⁴

Notes:

1. Can be implemented with an IDT bus switch.
2. Can be implemented with an external resistor.
3. The OE input of the output buffer must be deasserted permanently (handled by software).
4. The OE input of the output buffer must be asserted permanently (handled by software).

3.3 V LVTTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-20 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
−0.3	0.8	2.0	3.6	0.4	2.4	24	−24

AC Loadings

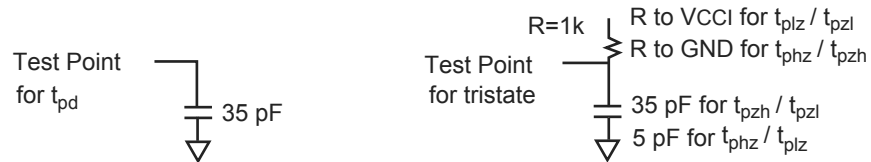


Figure 2-15 • AC Test Loads

Table 2-21 • AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	3.0	1.40	N/A	35

Note: * Measuring Point = VTRIP

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 4 (24mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		2.99		3.41		4.01	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.49		2.51		2.51	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.59		2.95		3.46	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.56		4.06		4.77	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

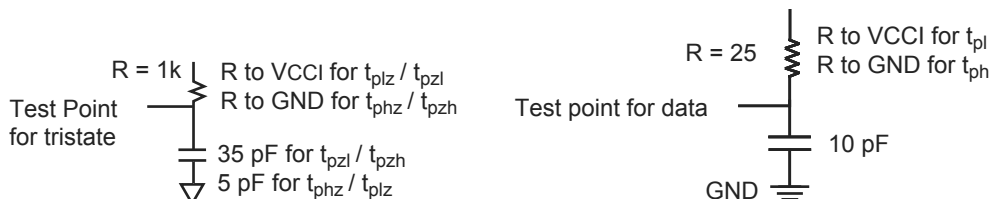


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-35 • 3.3 V PCI I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Output Module Timing								
t _{DP}	Input Buffer		1.57		1.79		2.10	ns
t _{PY}	Output Buffer		1.91		2.18		2.56	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-36 • 3.3 V PCI-X I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI-X Output Module Timing								
t _{DP}	Input Buffer	1.57		1.79		2.10		ns
t _{PY}	Output Buffer	2.10		2.40		2.82		ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low	1.61		1.62		1.63		ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High	1.59		1.60		1.61		ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z	2.65		3.02		3.55		ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z	3.11		3.55		4.17		ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register	0.67		0.77		0.90		ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Carry-Chain Logic

The Axcelerator dedicated carry-chain logic offers a very compact solution for implementing arithmetic functions without sacrificing performance.

To implement the carry-chain logic, two C-cells in a Cluster are connected together so the FCO (i.e. carry out) for the two bits is generated in a carry look-ahead scheme to achieve minimum propagation delay from the FCI (i.e. carry in) into the two-bit Cluster. The two-bit carry logic is shown in Figure 2-29.

The FCI of one C-cell pair is driven by the FCO of the C-cell pair immediately above it. Similarly, the FCO of one C-cell pair, drives the FCI input of the C-cell pair immediately below it (Figure 1-4 on page 1-3 and Figure 2-30 on page 2-57).

The carry-chain logic is selected via the CFN input. When carry logic is not required, this signal is deasserted to save power. Again, this configuration is handled automatically for the user through Microsemi's macro library.

The signal propagation delay between two C-cells in the carry-chain sequence is 0.1 ns.

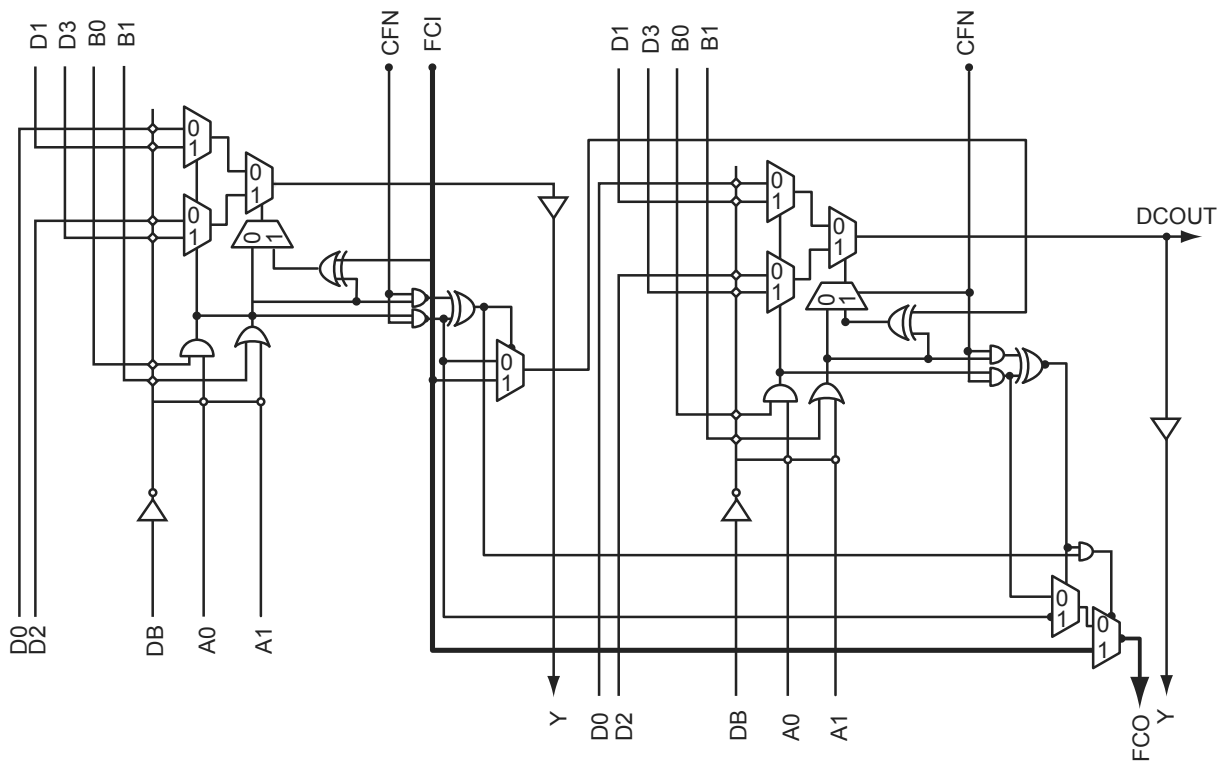


Figure 2-29 • Axcelerator's Two-Bit Carry Logic

R-Cell

Introduction

The R-cell, the sequential logic resource of the Axcelerator devices, is the second logic module type in the AX family architecture. It includes clock inputs for all eight global resources of the Axcelerator architecture as well as global presets and clears (Figure 2-31).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-Cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).
- Independent active-low asynchronous clear (CLR).
- Independent active-low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
 - One of the four high performance hardwired fast clocks (HCLKs)
 - One of the four routed clocks (CLKs)
 - User signals
- Global power-on clear (GCLR) and preset (GPSET), which drive each flip-flop on a chip-wide basis.
 - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET = 1 at device power-up. When the option is checked, GCLR = 1 and GPSET = 0. Both pins are pulled High when the device is in user mode. Refer to the "Simulation Support for GCLR/GPSET in Axcelerator" section of the *Antifuse Macro Library Guide* for information on simulation support for GCLR and GPSET.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Microsemi's extensive macro library (see the *Antifuse Macro Library Guide* for a complete listing of available AX macros).

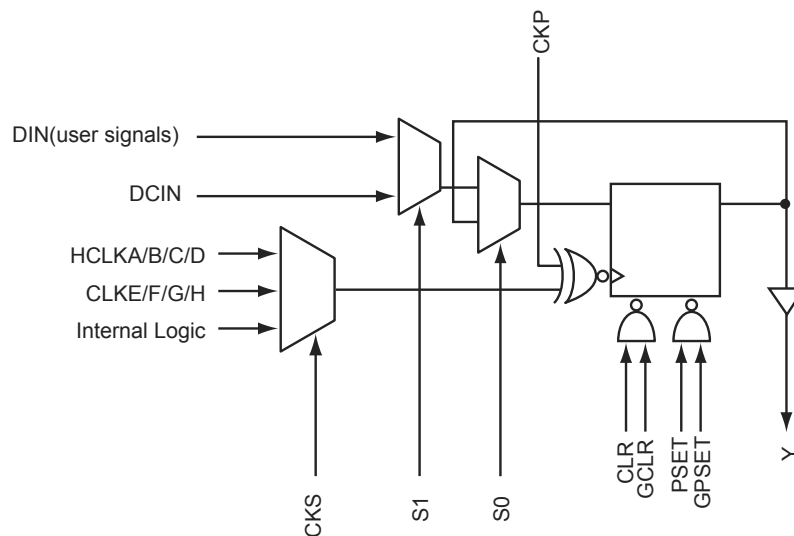


Figure 2-31 • R-Cell

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-70 • AX125 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-71 • AX250 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t _{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-86). Each block has independent read and write ports which enable simultaneous read and write operations.

Table 2-86 • Memory Block WxD Options

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in Table 2-87.

Table 2-87 • Allowable RW and WW Values

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

Table 2-92 • Eight RAM Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t _{WDASU}	Write Data Setup vs. WCLK		5.78		6.58		7.74	ns
t _{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WADSU}	Write Address Setup vs. WCLK		5.78		6.58		7.74	ns
t _{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WENSU}	Write Enable Setup vs. WCLK		5.78		6.58		7.74	ns
t _{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t _{WCLK}	WCLK Minimum Low Pulse Width	5.13		5.13		5.13		ns
t _{WCKP}	WCLK Minimum Period	5.88		5.88		5.88		ns
Read Mode								
t _{RADSU}	Read Address Setup vs. RCLK		6.75		7.69		9.04	ns
t _{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RENSU}	Read Enable Setup vs. RCLK		6.75		7.69		9.04	ns
t _{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		3.39		3.86		4.54	ns
t _{RCK2RD2}	RCLK-To-OUT (Non-Pipelined)		4.93		5.62		6.61	ns
t _{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t _{RCLKL}	RCLK Minimum Low Pulse Width	5.77		5.77		5.77		ns
t _{RCKP}	RCLK Minimum Period	6.50		6.50		6.50		ns

Note: Timing data for these eight cascaded RAM blocks uses a depth of 32,768. For all other combinations, use Microsemi's timing software.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO163PB5F15	AA14	IO182NB5F17	AF7	IO200NB6F18	AA4
IO164NB5F15	AE13	IO182PB5F17	AG7	IO200PB6F18	AA5
IO164PB5F15	AF13	IO183NB5F17	AD7	IO201NB6F18	W5
IO165NB5F15	AF12	IO183PB5F17	AE7	IO201PB6F18	W6
IO165PB5F15	AG12	IO184NB5F17	AC7	IO202NB6F18	AB1
IO166NB5F15	AD12	IO184PB5F17	AC8	IO202PB6F18	AC1
IO166PB5F15	AE12	IO185NB5F17	AF6	IO203NB6F19	Y3
IO167NB5F15	Y13	IO185PB5F17	AG6	IO203PB6F19	AA3
IO167PB5F15	AA13	IO186NB5F17	AB7	IO204NB6F19	AA2
IO168NB5F15	AD11	IO186PB5F17	AB8	IO204PB6F19	AB2
IO168PB5F15	AE11	IO187NB5F17	Y9	IO205NB6F19	U8
IO169NB5F15	AG11	IO187PB5F17	AA9	IO205PB6F19	V8
IO169PB5F15	AF11	IO188NB5F17	AD6	IO206NB6F19	V5
IO170NB5F15	AB11	IO188PB5F17	AE6	IO206PB6F19	V6
IO170PB5F15	AC11	IO189NB5F17	AB6	IO207NB6F19	Y1
IO171NB5F16	AF10	IO189PB5F17	AC6	IO207PB6F19	AA1
IO171PB5F16	AG10	IO190NB5F17	AF5	IO208NB6F19	W4
IO172NB5F16	AD10	IO190PB5F17	AG5	IO208PB6F19	Y4
IO172PB5F16	AE10	IO191NB5F17	AA6	IO209NB6F19	T7
IO173NB5F16	Y12	IO191PB5F17	AA7	IO209PB6F19	U7
IO173PB5F16	AA12	IO192NB5F17	Y8	IO210NB6F19	W2
IO174NB5F16	AB10	IO192PB5F17	AA8	IO210PB6F19	Y2
IO174PB5F16	AC10	Bank 6		IO211NB6F19	U5
IO175NB5F16	AF9	IO193NB6F18	W8	IO211PB6F19	U6
IO175PB5F16	AG9	IO193PB6F18	Y7	IO212NB6F19	V3
IO176NB5F16	AD9	IO194NB6F18	AB5	IO212PB6F19	W3
IO176PB5F16	AE9	IO194PB6F18	AC5	IO213NB6F19	R9
IO177NB5F16	Y11	IO195NB6F18	AC2	IO213PB6F19	T8
IO177PB5F16	AA11	IO195PB6F18	AC3	IO214NB6F20	U4
IO178NB5F16	AF8	IO196NB6F18	AC4	IO214PB6F20	V4
IO178PB5F16	AG8	IO196PB6F18	AD4	IO215NB6F20	T5
IO179NB5F16	AD8	IO197NB6F18	Y5	IO215PB6F20	T6
IO179PB5F16	AE8	IO197PB6F18	Y6	IO216NB6F20	V1
IO180NB5F16	AB9	IO198NB6F18	AB3	IO216PB6F20	W1
IO180PB5F16	AC9	IO198PB6F18	AB4	IO217NB6F20	R7
IO181NB5F17	Y10	IO199NB6F18	V7	IO217PB6F20	R8
IO181PB5F17	AA10	IO199PB6F18	W7	IO218NB6F20	U2

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
IO52NB3F3	P18	IO69PB4F4	AA17	IO87NB5F5	Y4
IO52PB3F3	P19	IO70NB4F4	AB14	IO87PB5F5	Y5
IO53NB3F3	R20	IO70PB4F4	AB15	IO88NB5F5	V6
IO53PB3F3	P20	IO71NB4F4	Y14	IO88PB5F5	V7
IO54NB3F3	T21	IO71PB4F4	W14	IO89NB5F5	T7
IO54PB3F3	R21	IO72NB4F4	AA14	IO89PB5F5	T8
IO55NB3F3	R17	IO72PB4F4	AA15	Bank 6	
IO55PB3F3	P17	IO73NB4F4	AA13	IO90NB6F6	V4
IO56NB3F3	U20	IO73PB4F4	AB13	IO90PB6F6	W5
IO56PB3F3	T20	IO74NB4F4/CLKEN	V12	IO91NB6F6	P7
IO57NB3F3	T18	IO74PB4F4/CLKEP	V13	IO91PB6F6	R7
IO57PB3F3	R18	IO75NB4F4/CLKFN	W11	IO92NB6F6	U5
IO58NB3F3	U19	IO75PB4F4/CLKFP	W12	IO92PB6F6	T5
IO58PB3F3	T19	Bank 5		IO93NB6F6	P6
IO59NB3F3	R16	IO76NB5F5/CLKGN	U10	IO93PB6F6	R6
IO59PB3F3	P16	IO76PB5F5/CLKGP	U11	IO94NB6F6	T4
IO60NB3F3	W20	IO77NB5F5/CLKHN	V9	IO94PB6F6	U4
IO60PB3F3	V20	IO77PB5F5/CLKHP	V10	IO95NB6F6	P5
IO61NB3F3	U18	IO78NB5F5	AA9	IO95PB6F6	R5
IO61PB3F3	V19	IO78PB5F5	AA10	IO96NB6F6	T3
Bank 4		IO79NB5F5	AB9	IO96PB6F6	U3
IO62NB4F4	T15	IO79PB5F5	AB10	IO97NB6F6	P3
IO62PB4F4	T16	IO80NB5F5	AA7	IO97PB6F6	R3
IO63NB4F4	W17	IO80PB5F5	AA8	IO98NB6F6	R2
IO63PB4F4	V17	IO81NB5F5	W8	IO98PB6F6	T2
IO64NB4F4	V15	IO81PB5F5	W9	IO99NB6F6	P4
IO64PB4F4	V16	IO82NB5F5	AB5	IO99PB6F6	R4
IO65NB4F4	Y19	IO82PB5F5	AB6	IO100NB6F6	P1
IO65PB4F4	W18	IO83NB5F5	AA5	IO100PB6F6	R1
IO66NB4F4	AB18	IO83PB5F5	AA6	IO101NB6F6	M7
IO66PB4F4	AB19	IO84NB5F5	U8	IO101PB6F6	N7
IO67NB4F4	W15	IO84PB5F5	U9	IO102NB6F6	N2
IO67PB4F4	W16	IO85NB5F5	Y6	IO102PB6F6	P2
IO68NB4F4	U14	IO85PB5F5	Y7	IO103NB6F6	M6
IO68PB4F4	U15	IO86NB5F5	W6	IO103PB6F6	N6
IO69NB4F4	AA16	IO86PB5F5	W7	IO104NB6F6	M4

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
IO104PB6F6	N4	IO122NB7F7	G5	GND	J9
IO105NB6F6	M5	IO122PB7F7	G6	GND	K10
IO105PB6F6	N5	IO123NB7F7	F5	GND	K11
IO106NB6F6	M3	IO123PB7F7	E4	GND	K12
IO106PB6F6	N3	Dedicated I/O		GND	K13
Bank 7		VCCDA	H7	GND	L1
IO107NB7F7	M2	GND	A1	GND	L10
IO107PB7F7	N1	GND	A11	GND	L11
IO108NB7F7	L3	GND	A12	GND	L12
IO108PB7F7	L2	GND	A2	GND	L13
IO109NB7F7	K2	GND	A21	GND	L22
IO109PB7F7	K1	GND	A22	GND	M1
IO110NB7F7	K5	GND	AA1	GND	M10
IO110PB7F7	L5	GND	AA2	GND	M11
IO111NB7F7	K6	GND	AA21	GND	M12
IO111PB7F7	L6	GND	AA22	GND	M13
IO112NB7F7	K4	GND	AB1	GND	M22
IO112PB7F7	K3	GND	AB11	GND	N10
IO113NB7F7	K7	GND	AB12	GND	N11
IO113PB7F7	L7	GND	AB2	GND	N12
IO114NB7F7	H1	GND	AB21	GND	N13
IO114PB7F7	J1	GND	AB22	GND	P14
IO115NB7F7	H2	GND	B1	GND	P9
IO115PB7F7	J2	GND	B2	GND	R15
IO116NB7F7	H4	GND	B21	GND	R8
IO116PB7F7	J4	GND	B22	GND	U16
IO117NB7F7	H5	GND	C20	GND	U6
IO117PB7F7	J5	GND	C3	GND	V18
IO118NB7F7	F2	GND	D19	GND	V5
IO118PB7F7	G2	GND	D4	GND	W19
IO119NB7F7	H6	GND	E18	GND	W4
IO119PB7F7	J6	GND	E5	GND	Y20
IO120NB7F7	F1	GND	G18	GND	Y3
IO120PB7F7	G1	GND	H15	GND/LP	G7
IO121NB7F7	F4	GND	H8	NC	A17
IO121PB7F7	G4	GND	J14	NC	A18

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO155PB3F14	AC29	IO172PB4F16	AH27	IO190NB4F17	AH22
IO156NB3F14	AE30	IO173NB4F16	AJ27	IO190PB4F17	AH23
IO156PB3F14	AD30	IO173PB4F16	AJ28	IO191NB4F17	AJ23
IO157NB3F14	AC26	IO174NB4F16	AL27	IO191PB4F17	AJ24
IO157PB3F14	AB26	IO174PB4F16	AL28	IO192NB4F17	AG21
IO158NB3F14	AH33	IO175NB4F16	AM28	IO192PB4F17	AG22
IO158PB3F14	AG33	IO175PB4F16	AM29	IO193NB4F18	AP23
IO159NB3F14	AD27	IO176NB4F16	AG25	IO193PB4F18	AP24
IO159PB3F14	AC27	IO176PB4F16	AG26	IO194NB4F18	AN22
IO160NB3F14	AG32	IO177NB4F16	AK26	IO194PB4F18	AN23
IO160PB3F14	AF32	IO177PB4F16	AK27	IO195NB4F18	AM23
IO161NB3F15	AG31	IO178NB4F16	AF25	IO195PB4F18	AL23
IO161PB3F15	AF31	IO178PB4F16	AE25	IO196NB4F18	AF21
IO162NB3F15	AF29	IO179NB4F16	AP28	IO196PB4F18	AF22
IO162PB3F15	AE29	IO179PB4F16	AN28	IO197NB4F18	AL22
IO163NB3F15	AE28	IO180NB4F16	AJ25	IO197PB4F18	AM22
IO163PB3F15	AD28	IO180PB4F16	AJ26	IO198NB4F18	AE21
IO164NB3F15	AG30	IO181NB4F17	AM26	IO198PB4F18	AE22
IO164PB3F15	AF30	IO181PB4F17	AM27	IO199NB4F18	AJ21
IO165NB3F15	AE26	IO182NB4F17	AF24	IO199PB4F18	AJ22
IO165PB3F15	AD26	IO182PB4F17	AE24	IO200NB4F18	AK21
IO166NB3F15	AJ30	IO183NB4F17	AH24	IO200PB4F18	AK22
IO166PB3F15	AH30	IO183PB4F17	AH25	IO201NB4F18	AM21
IO167NB3F15	AG28	IO184NB4F17	AG23	IO201PB4F18	AL21
IO167PB3F15	AF28	IO184PB4F17	AG24	IO202NB4F18	AE20
IO168NB3F15	AF27	IO185NB4F17	AL25	IO202PB4F18	AD20
IO168PB3F15	AE27	IO185PB4F17	AL26	IO203NB4F19	AN21
IO169NB3F15	AH29	IO186NB4F17	AP25	IO203PB4F19	AP21
IO169PB3F15	AG29	IO186PB4F17	AP26	IO204NB4F19	AP20
IO170NB3F15	AD25	IO187NB4F17	AK24	IO204PB4F19	AN20
IO170PB3F15	AC25	IO187PB4F17	AK25	IO205NB4F19	AN19
Bank 4		IO188NB4F17	AF23	IO205PB4F19	AP19
IO171NB4F16	AP29	IO188PB4F17	AE23	IO206NB4F19	AG20
IO171PB4F16	AN29	IO189NB4F17	AN24	IO206PB4F19	AF20
IO172NB4F16	AH26	IO189PB4F17	AM24	IO207NB4F19	AL19

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	AK12	GND	AN34	GND	D1
GND	AK17	GND	AN4	GND	D11
GND	AK18	GND	AN9	GND	D2
GND	AK23	GND	AP13	GND	D24
GND	AK30	GND	AP2	GND	D3
GND	AK5	GND	AP22	GND	D31
GND	AL1	GND	AP27	GND	D32
GND	AL11	GND	AP3	GND	D33
GND	AL2	GND	AP31	GND	D34
GND	AL24	GND	AP32	GND	D4
GND	AL3	GND	AP33	GND	E12
GND	AL31	GND	AP4	GND	E17
GND	AL32	GND	AP8	GND	E18
GND	AL33	GND	B1	GND	E23
GND	AL34	GND	B2	GND	E30
GND	AL4	GND	B26	GND	E5
GND	AM1	GND	B3	GND	F29
GND	AM10	GND	B31	GND	F30
GND	AM15	GND	B32	GND	F6
GND	AM2	GND	B33	GND	G28
GND	AM20	GND	B34	GND	G7
GND	AM25	GND	B4	GND	H1
GND	AM3	GND	B9	GND	H34
GND	AM31	GND	C1	GND	J2
GND	AM32	GND	C10	GND	J33
GND	AM33	GND	C15	GND	K3
GND	AM34	GND	C2	GND	K32
GND	AM4	GND	C20	GND	L11
GND	AN1	GND	C25	GND	L24
GND	AN2	GND	C3	GND	L31
GND	AN26	GND	C31	GND	L4
GND	AN3	GND	C32	GND	M12
GND	AN31	GND	C33	GND	M23
GND	AN32	GND	C34	GND	M30
GND	AN33	GND	C4	GND	M5

PQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	Pin Number
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX250 Function	Pin Number
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX250 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CQ352		CQ352		CQ352	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
Bank 0				Bank 3	
IO01NB0F0	341	IO71NB1F6	277	IO129NB3F12	219
IO01PB0F0	342	IO71PB1F6	278	IO129PB3F12	220
IO02PB0F0	343	IO73NB1F6	269	IO132NB3F12	217
IO04NB0F0	337	IO73PB1F6	270	IO132PB3F12	218
IO04PB0F0	338	IO74NB1F6	271	IO137NB3F12	213
IO05NB0F0	335	IO74PB1F6	272	IO137PB3F12	214
IO05PB0F0	336	Bank 2		IO139NB3F13	211
IO08NB0F0	331	IO87NB2F8	261	IO139PB3F13	212
IO08PB0F0	332	IO87PB2F8	262	IO141NB3F13	205
IO37NB0F3	325	IO88NB2F8	255	IO141PB3F13	206
IO37PB0F3	326	IO88PB2F8	256	IO142NB3F13	207
IO38NB0F3	323	IO89NB2F8	259	IO142PB3F13	208
IO38PB0F3	324	IO89PB2F8	260	IO145NB3F13	199
IO41NB0F3/HCLKAN	319	IO91NB2F8	253	IO145PB3F13	200
IO41PB0F3/HCLKAP	320	IO91PB2F8	254	IO146NB3F13	201
IO42NB0F3/HCLKBN	313	IO99NB2F9	249	IO146PB3F13	202
IO42PB0F3/HCLKBP	314	IO99PB2F9	250	IO147NB3F13	193
Bank 1		IO100NB2F9	247	IO147PB3F13	194
IO43NB1F4/HCLKCN	305	IO100PB2F9	248	IO148NB3F13	195
IO43PB1F4/HCLKCP	306	IO107NB2F10	243	IO148PB3F13	196
IO44NB1F4/HCLKDN	299	IO107PB2F10	244	IO149NB3F13	189
IO44PB1F4/HCLKDP	300	IO110NB2F10	241	IO149PB3F13	190
IO48NB1F4	295	IO110PB2F10	242	IO161NB3F15	183
IO48PB1F4	296	IO111NB2F10	237	IO161PB3F15	184
IO65NB1F6	283	IO111PB2F10	238	IO163NB3F15	187
IO65PB1F6	284	IO112NB2F10	235	IO163PB3F15	188
IO66NB1F6	289	IO112PB2F10	236	IO165NB3F15	181
IO66PB1F6	290	IO113NB2F10	231	IO165PB3F15	182
IO68NB1F6	287	IO113PB2F10	232	IO167NB3F15	179
IO68PB1F6	288	IO114NB2F10	229	IO167PB3F15	180
IO69NB1F6	275	IO114PB2F10	230	Bank 4	
IO69PB1F6	276	IO115NB2F10	225	IO181NB4F17	172
IO70NB1F6	281	IO115PB2F10	226	IO181PB4F17	173
IO70PB1F6	282	IO117NB2F10	223	IO182NB4F17	170
		IO117PB2F10	224		

Revision	Changes	Page
Revision 3 (continued)	The timing characteristics tables from pages 2-26 to 2-60 were updated.	2-26 to 2-60
	The "Global Resources" section was updated.	2-66
	The timing characteristics tables from pages 2-102 to 2-103 were updated.	2-102 to 2-103
	The "PQ208", "FG256", and "FG324" tables are new.	3-9,3-16, 3-84