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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	248
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-1fgg484

The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).
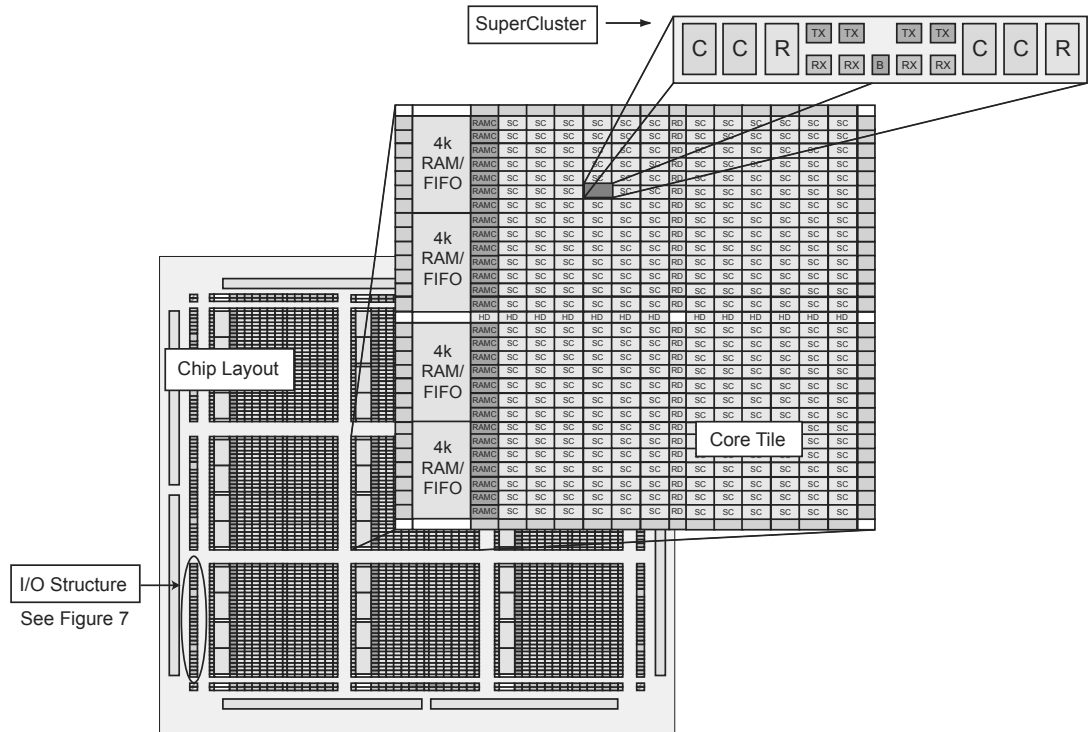
Figure 1-6 • **AX Device Architecture (AX1000 shown)**

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

![Microsemi logo]

Timing Model
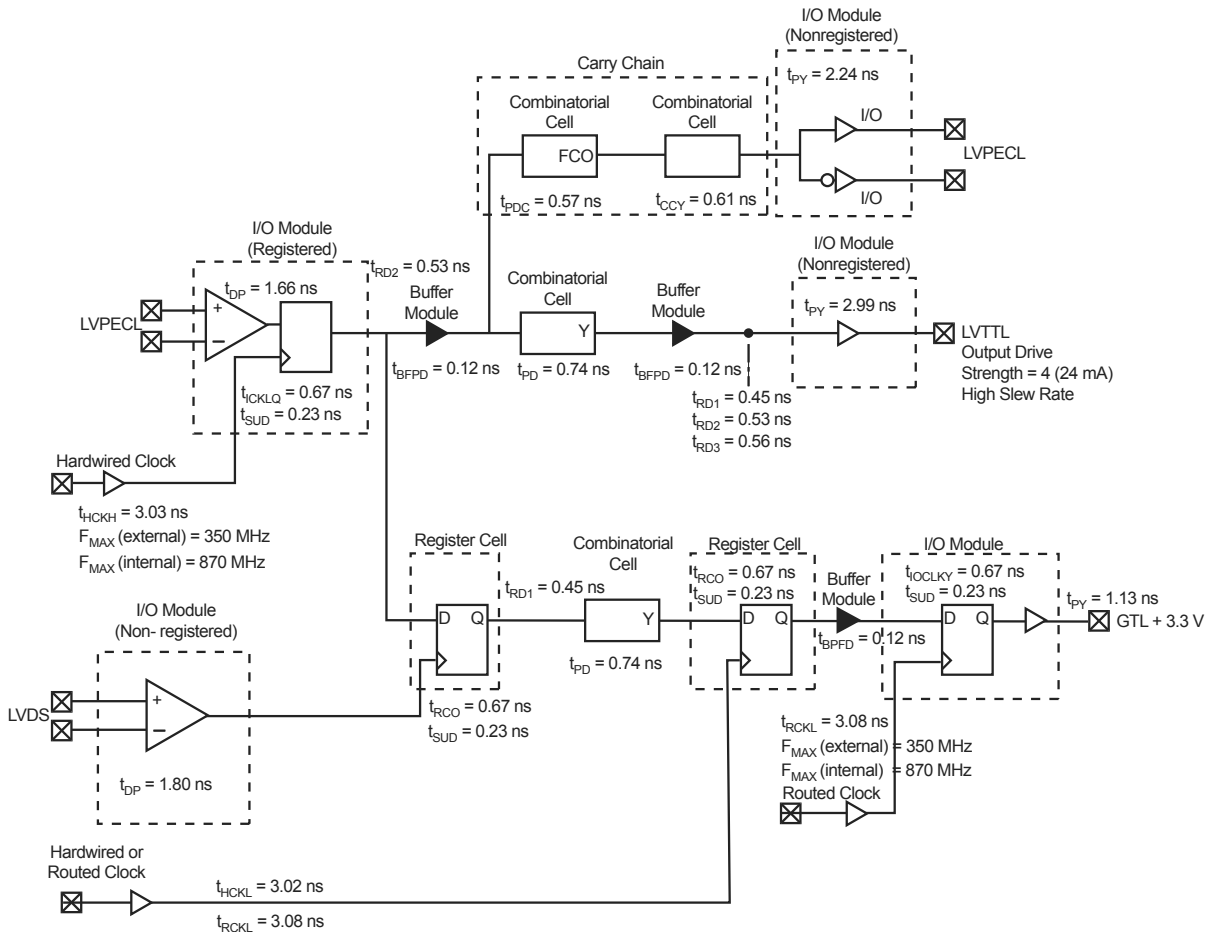
Note: Worst case timing data for the AX1000, –2 speed grade

Figure 2-1 • **Worst Case Timing Data**

Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$$= (t_{DP} + t_{RD2} + t_{SUD)} - t_{HCKL}$$
$$= (1.72 + 0.53 + 0.23) - 3.02 = -0.54 \text{ ns}$$

Clock-to-Out (Pad-to-Pad)

$$= t_{HCKL} + t_{RCO} + t_{RD1} + t_{PY}$$
$$= 3.02 + 0.67 + 0.45 + 2.99 = 7.13 \text{ ns}$$

Routed Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$$= (t_{DP} + t_{RD2} + t_{SUD)} - t_{RCKH}$$
$$= (1.72 + 0.53 + 0.23) - 3.13 = -0.65 \text{ ns}$$

Clock-to-Out (Pad-to-Pad)

$$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$$
$$= 3.13 + 0.67 + 0.45 + 3.03 = 7.24 \text{ ns}$$

I/O Specifications

Pin Descriptions

Supply Pins

GND   **Ground**

Low supply voltage.

VCCA   **Supply Voltage**

Supply voltage for array (1.5V). See "Operating Conditions" on page 2-1 for more information.

VCCIBx   **Supply Voltage**

Supply voltage for I/Os. Bx is the I/O Bank ID – 0 to 7. See "Operating Conditions" on page 2-1 for more information.

VCCDA   **Supply Voltage**

Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. See "Operating Conditions" on page 2-1 for more information. VCCDA should be tied to 3.3V.

VCCPLA/B/C/D/E/F/G/H   **Supply Voltage**

PLL analog power supply (1.5V) for internal PLL. There are eight in each device. VCCPLA supports the PLL associated with global resource HCLKA, VCCPLB supports the PLL associated with global resource HCLKB, etc. The PLL analog power supply pins should be connected to 1.5V whether PLL is used or not.

VCOMPLA/B/C/D/E/F/G/H   **Supply Voltage**

Compensation reference signals for internal PLL. There are eight in each device. **VCOMPLA** supports the PLL associated with global resource HCLKA, VCOMPLE supports the PLL associated with global resource CLKE, etc. (see Figure 2-2 on page 2-9 for correct external connection to the supply). The VCOMPLX pins should be left floating if PLL is not used.

VPUMP   **Supply Voltage (External Pump)**

In the low power mode, VPUMP will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on VPUMP reaches VIH[1]. In normal device operation, when using the internal charge pump, VPUMP should be tied to GND.

Figure 2-2 • **VCCPLX and VCOMPLX Power Supply Connect**

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1. When $V_{PUMP} = V_{IH}$, it shuts off the internal charge pump. See **"Low Power Mode" on page 2-106**.

User I/Os[2]

Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-8 on page 2-12 contains the I/O standards supported by the Axcelerator family, and Table 2-10 on page 2-12 compares the features of the different I/O standards.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (Figure 2-6 on page 2-18). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules:

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.

- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.

- Dedicated I/O pins such as GND and VCCI are counted as part of the 16.

- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.

- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3 V.

A user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.

- Use generic I/O macros and then use Designer's PinEditor to specify the desired I/O standards (please note that this is not applicable to differential standards).

- A combination of the first two methods.

Refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

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2. *Do not use an external resister to pull the I/O above V_{CCI} for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above V_{CCI}.*

Table 2-13 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank.

Table 2-13 • **Legal I/O Usage Matrix**

I/O Standard	LVTTL 3.3 V	LVCMOS 2.5 V	LVCMOS1.8 V	LVCMOS1.5 V (JESD8-11)	3.3V PCI/PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	HSTL Class I (1. 5V)	SSTL2 Class I & II (2.5 V)	SSTL3 Class I & II (3.3 V)	LVDS (2.5 V)	LVPECL (3.3 V)
LVTTL 3.3 V (VREF=1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVTTL 3.3 V(VREF=1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVCMOS 2.5 V (VREF=1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVCMOS 2.5 V (VREF=1.25V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVCMOS1.8 V	–	–	✓	–	–	–	–	–	–	–	–	–
LVCMOS1.5 V (VREF = 1.75 V) (JESD8-11)	–	–	–	✓	–	–	–	✓	–	–	–	–
3.3 V PCI/PCI-X (VREF = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
3.3 V PCI/PCI-X (VREF= 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
GTL + (3.3 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
GTL + (2.5 V)	–	✓	–	–	–	–	✓	–	–	–	–	–
HSTL Class I	–	–	–	✓	–	–	–	✓	–	–	–	–
SSTL2 Class I & II	–	✓	–	–	–	–	–	–	✓	–	✓	–
SSTL3 Class I & II	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVDS (VREF = 1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVDS (VREF = 1.25 V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVPECL (VREF = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVPECL (VREF = 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓

Notes:

1. *Note that GTL+ 2.5 V is not supported across the full military temperature range.*
2. *A "✓" indicates whether standards can be used within a bank at the same time.*
   Examples:
   a) LVTTL can be used with 3.3V PCI and GTL+ (3.3V), when V_{REF} = 1.0V (GTL+ requirement).
   b) LVTTL can be used with 3.3V PCI and SSTL3 Class I and II, when V_{REF} = 1.5V (SSTL3 requirement).

Note that two I/O standards are compatible if:

- Their VCCI values are identical.
- Their VREF standards are identical (if applicable).

For example, if LVTTL 3.3 V (VREF= 1.0 V) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTL 3.3 V PCI/PCI-X, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank.

Timing Characteristics

Table 2-32 • **1.5V LVCMOS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.4 V, TJ = 70°C

Parameter	Description	–2 Speed Min.	–2 Speed Max.	–1 Speed Min.	–1 Speed Max.	Std Speed Min.	Std Speed Max.	Units
LVCMOS15 (JESD8-11) I/O Module Timing								
t_{DP}	Input Buffer		3.59		4.09		4.81	ns
t_{PY}	Output Buffer		6.05		6.89		8.10	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.31		3.34		3.34	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.56		4.58		4.59	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.37		7.25		8.52	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.94		7.90		9.29	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns
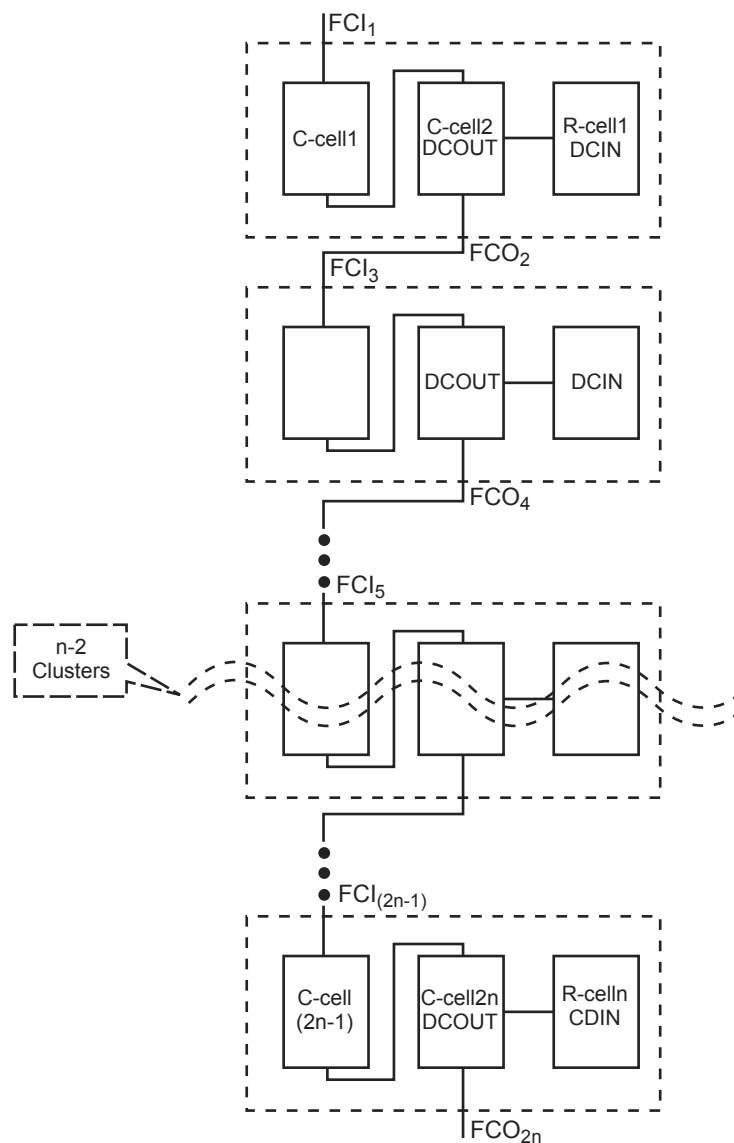
Note: *The carry-chain sequence can end on either C-cell.*

Figure 2-30 • Carry-Chain Sequencing of C-Cells

Timing Characteristics

Refer to Table 2-62 on page 2-55 for more information on carry-chain timing.

Routing Specifications

Routing Resources

The routing structure found in Axcelerator devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the AX architecture: DirectConnect, CarryConnect, FastConnect, and Vertical and Horizontal Routing.

DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 2-35). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

Figure 2-35 • **DirectConnect and CarryConnect**

CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (Figure 2-35). The FCO output of the right C-cell of a two-C-cell Cluster drives the FCI input of the left C-cell in the two-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two-C-cell cluster to the FCI of the two-C-cell cluster immediately below it (see the "Carry-Chain Logic" section on page 2-56 for more information).

FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 2-36 on page 2-62). FastConnects provide a maximum delay of 0.3 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

The HM and CM modules can select between:

- The HCLK or CLK source respectively
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module respectively
- A local signal routed on generic routing resources

The AX architecture is capable of supporting a large number of local clocks—24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Microsemi's Designer software's place-and-route takes advantage of the segmented clock structure found in Axcelerator devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption.

Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s), an internal net, or the output of a PLL. These connections can be made by using one of three types of macros: CLKBUF, CLKINT, and PLLCLK.

CLKBUF and HCLKBUF

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF_LVCMOS25, HCLKBUF_LVDS, etc.) (Figure 2-42).
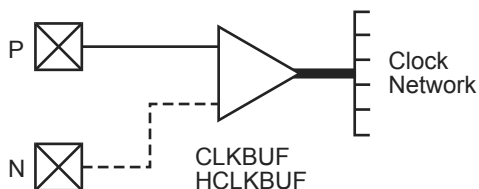
Figure 2-42 • CLKBUF and HCLKBUF

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

CLKINT and HCLKINT

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 2-43).
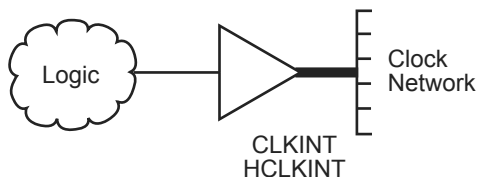
Figure 2-43 • CLKINT and HCLKINT
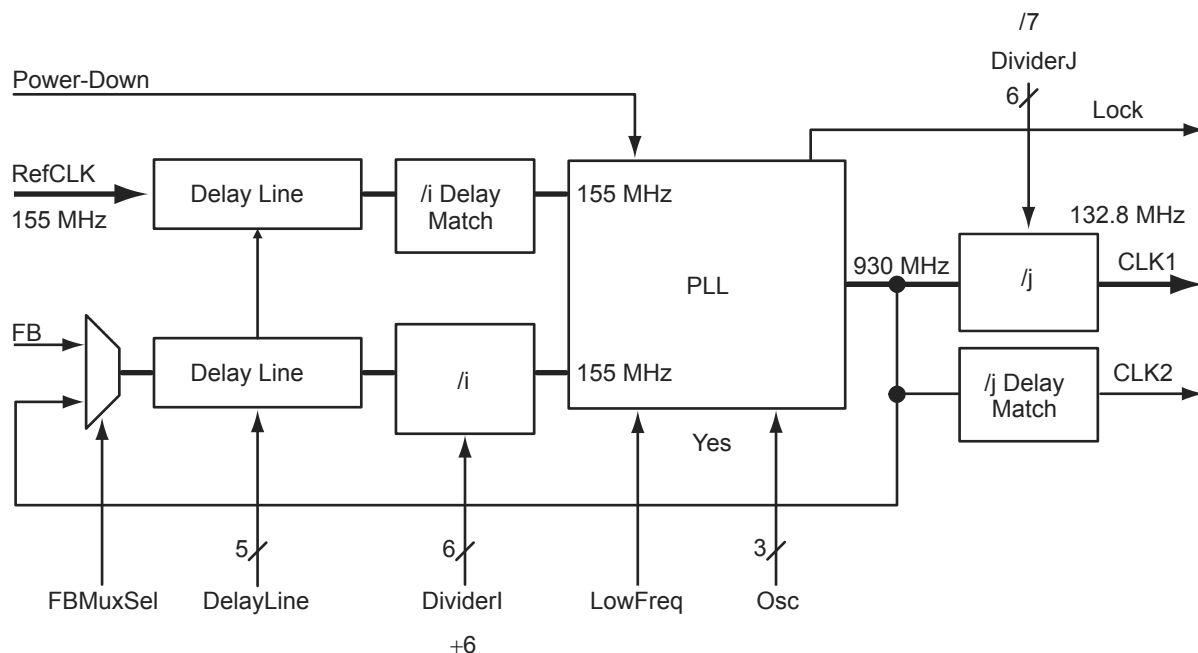
Figure 2-54 • **Using the PLL 155 MHz In, 133 MHz Out**

Figure 2-55 • **Using the PLL Delaying the Reference Clock**

mode if desired. Please note, if the I/O bank is not disabled, differential I/Os belonging to the I/O bank will still consume normal power, even when operating in the low power mode.

The Axcelerator device will resume normal operation 10μs after the LP pin is pulled Low.

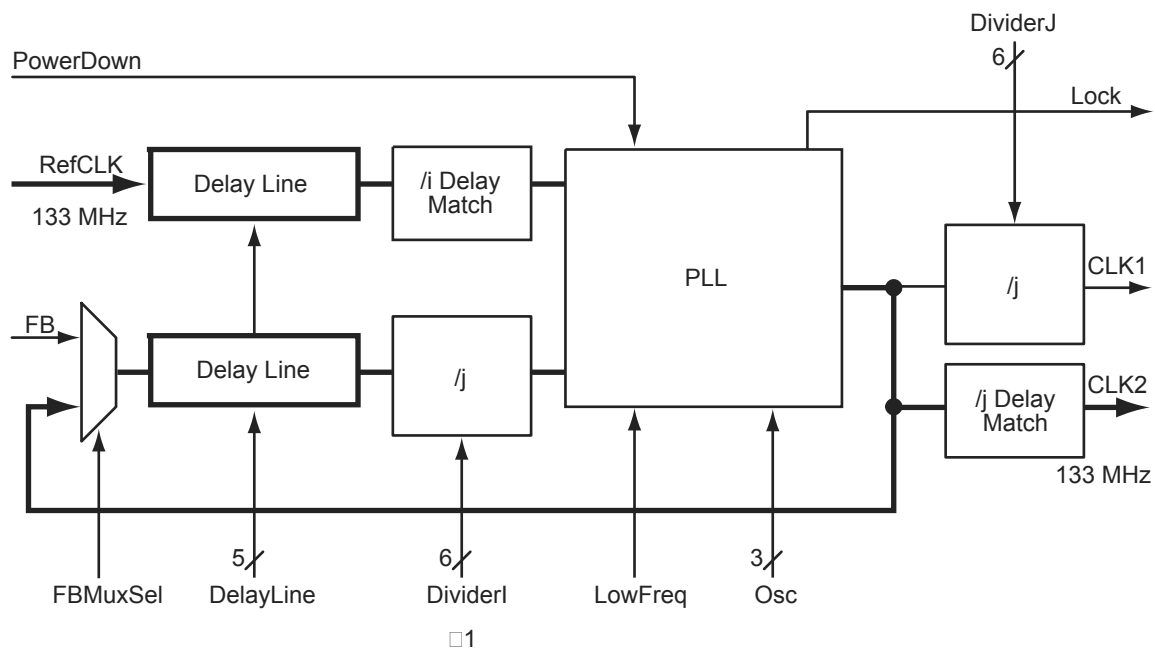To further reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e. high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

In addition, any PLL in use can be powered down to further reduce power consumption. This can be done with the PowerDown pin driven Low. Driving this pin High restarts the PLL with the output clock(s) being stable once lock is restored.

JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the Table 2-103.

Table 2-103 • **JTAG Instruction Code**

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload / Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
Reserved	All others
Bypass	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low, asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1 kΩ resistor.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a VCCA and/or VCCDA voltage drop.

throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is protected with highest level of security in the industry.

Figure 2-69 • **FuseLock Logo**

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to the *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (Figure 2-31 on page 2-58). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-108).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-7). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

BG729		BG729		BG729	
AX1000 Function	**Pin Number**	**AX1000 Function**	**Pin Number**	**AX1000 Function**	**Pin Number**
GND	B27	GND	R11	VCCA	K11
GND	B3	GND	R12	VCCA	K17
GND	C1	GND	R13	VCCA	K18
GND	C2	GND	R14	VCCA	L10
GND	C25	GND	R15	VCCA	L18
GND	C26	GND	R16	VCCA	U10
GND	C27	GND	R17	VCCA	U18
GND	C3	GND	T11	VCCA	V10
GND	E27	GND	T12	VCCA	V11
GND	L11	GND	T13	VCCA	V17
GND	L12	GND	T14	VCCA	V18
GND	L13	GND	T15	VCCPLA	A13
GND	L14	GND	T16	VCCPLB	J13
GND	L15	GND	T17	VCCPLC	B15
GND	L16	GND	U11	VCCPLD	C15
GND	L17	GND	U12	VCCPLE	AG14
GND	M11	GND	U13	VCCPLF	AF14
GND	M12	GND	U14	VCCPLG	AB13
GND	M13	GND	U15	VCCPLH	AG13
GND	M14	GND	U16	VCCDA	A11
GND	M15	GND	U17	VCCDA	AB12
GND	M16	GND/LP	J8	VCCDA	AC12
GND	M17	NC	U3	VCCDA	AC25
GND	N11	PRA	J14	VCCDA	AD16
GND	N12	PRB	D14	VCCDA	AD17
GND	N13	PRC	V14	VCCDA	E16
GND	N14	PRD	AB14	VCCDA	E2
GND	N15	TCK	E4	VCCDA	E24
GND	N16	TDI	D4	VCCDA	F12
GND	N17	TDO	J9	VCCDA	F16
GND	P11	TMS	H8	VCCDA	F7
GND	P12	TRST	E3	VCCDA	K14
GND	P13	VCCA	AA21	VCCDA	P10
GND	P14	VCCA	AD5	VCCDA	P18
GND	P15	VCCA	E1	VCCDA	W14
GND	P16	VCCA	G22	VCCDA	W9
GND	P17	VCCA	K10	VCCIB0	A4

FG256		FG256		FG256	
AX250 Function	**Pin Number**	**AX250 Function**	**Pin Number**	**AX250 Function**	**Pin Number**
Bank 0		IO32NB2F2	C16	IO61PB3F3	L14
IO01NB0F0	B4	IO32PB2F2	B16	**Bank 4**	
IO01PB0F0	B3	IO33NB2F2	F15	IO62NB4F4	N12
IO03NB0F0	A4	IO33PB2F2	E15	IO62PB4F4	N13
IO03PB0F0	A3	IO35NB2F2	H13	IO63NB4F4	T14
IO05NB0F0	B6	IO35PB2F2	G13	IO63PB4F4	R14
IO05PB0F0	B5	IO36NB2F2	E16	IO66PB4F4	T15
IO07NB0F0	A6	IO36PB2F2	D16	IO67NB4F4	R12
IO07PB0F0	A5	IO38NB2F2	H15	IO67PB4F4	R13
IO12NB0F0/HCLKAN	B8	IO38PB2F2	G15	IO69NB4F4	P11
IO12PB0F0/HCLKAP	B7	IO39NB2F2	H14	IO69PB4F4	P12
IO13NB0F0/HCLKBN	A9	IO39PB2F2	G14	IO70PB4F4	T11
IO13PB0F0/HCLKBP	A8	IO40NB2F2	G16	IO73NB4F4	T12
Bank 1		IO40PB2F2	F16	IO73PB4F4	T13
IO14NB1F1/HCLKCN	C10	IO43NB2F2	K15	IO74NB4F4/CLKEN	R9
IO14PB1F1/HCLKCP	C9	IO43PB2F2	K16	IO74PB4F4/CLKEP	R10
IO15NB1F1/HCLKDN	B11	IO44NB2F2	J16	IO75NB4F4/CLKFN	T8
IO15PB1F1/HCLKDP	B10	IO44PB2F2	H16	IO75PB4F4/CLKFP	T9
IO17NB1F1	A13	**Bank 3**		**Bank 5**	
IO17PB1F1	A12	IO45NB3F3	K13	IO76NB5F5/CLKGN	P7
IO19NB1F1	B13	IO45PB3F3	J13	IO76PB5F5/CLKGP	P8
IO19PB1F1	B12	IO46NB3F3	K14	IO77NB5F5/CLKHN	R6
IO21NB1F1	C12	IO46PB3F3	J14	IO77PB5F5/CLKHP	R7
IO21PB1F1	C11	IO52NB3F3	L15	IO79NB5F5	T5
IO23NB1F1	A15	IO52PB3F3	L16	IO79PB5F5	T6
IO23PB1F1	B14	IO54NB3F3	P16	IO81NB5F5	P5
IO26NB1F1	C15	IO54PB3F3	N16	IO81PB5F5	P6
IO26PB1F1	C14	IO55PB3F3	M16	IO83NB5F5	T3
IO27NB1F1	D13	IO56NB3F3	P15	IO83PB5F5	T4
IO27PB1F1	D12	IO56PB3F3	R16	IO85NB5F5	R3
Bank 2		IO58NB3F3	N15	IO85PB5F5	R4
IO29NB2F2	F13	IO58PB3F3	M15	IO88NB5F5	R1
IO29PB2F2	E13	IO59NB3F3	M13	IO88PB5F5	T2
IO30NB2F2	F14	IO59PB3F3	L13	IO89NB5F5	N4
IO30PB2F2	E14	IO61NB3F3	M14	IO89PB5F5	N5

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO155NB4F14	AC17	IO172NB5F16	AK9	IO189PB5F17	AD9
IO155PB4F14	AB17	IO172PB5F16	AK10	IO190NB5F17	AH6
IO156NB4F14	AK19	IO173NB5F16	AE12	IO190PB5F17	AG6
IO156PB4F14	AJ19	IO173PB5F16	AE13	IO191NB5F17	AG5
IO157NB4F14	AE17	IO174NB5F16	AG9	IO191PB5F17	AH5
IO157PB4F14	AD17	IO174PB5F16	AG10	IO192NB5F17	AC8
IO158NB4F14	AJ17	IO175NB5F16	AE11	IO192PB5F17	AC9
IO158PB4F14	AJ18	IO175PB5F16	AF11	**Bank 6**	
IO159NB4F14/CLKEN	AG18	IO176NB5F16	AH8	IO193NB6F18	AB7
IO159PB4F14/CLKEP	AH18	IO176PB5F16	AH9	IO193PB6F18	AC7
IO160NB4F14/CLKFN	AG16	IO177NB5F16	AC12	IO194NB6F18	AD5
IO160PB4F14/CLKFP	AG17	IO177PB5F16	AD12	IO194PB6F18	AE5
Bank 5		IO178NB5F16	AJ7	IO195NB6F18	AB6
IO161NB5F15/CLKGN	AG14	IO178PB5F16	AJ8	IO195PB6F18	AC6
IO161PB5F15/CLKGP	AG15	IO179NB5F16	AF9	IO196NB6F18	AE4
IO162NB5F15/CLKHN	AG13	IO179PB5F16	AF10	IO196PB6F18	AF4
IO162PB5F15/CLKHP	AH13	IO180NB5F16	AE9	IO197NB6F18	AA8
IO163NB5F15	AE14	IO180PB5F16	AE10	IO197PB6F18	AB8
IO163PB5F15	AD14	IO181NB5F17	AC11	IO198NB6F18	AF3
IO164NB5F15	AJ12	IO181PB5F17	AD11	IO198PB6F18	AG3
IO164PB5F15	AJ13	IO182NB5F17	AK6	IO199NB6F18	AC4
IO165NB5F15	AB14	IO182PB5F17	AK7	IO199PB6F18	AD4
IO165PB5F15	AC15	IO183NB5F17	AF8	IO200NB6F18	AB5
IO166NB5F15	AK11	IO183PB5F17	AG8	IO200PB6F18	AC5
IO166PB5F15	AK12	IO184NB5F17	AG7	IO201NB6F18	Y7
IO167NB5F15	AB13	IO184PB5F17	AH7	IO201PB6F18	AA7
IO167PB5F15	AC14	IO185NB5F17	AC10	IO202NB6F18	AD3
IO168NB5F15	AH11	IO185PB5F17	AD10	IO202PB6F18	AE3
IO168PB5F15	AH12	IO186NB5F17	AJ5	IO203NB6F19	Y6
IO169NB5F15	AD13	IO186PB5F17	AJ6	IO203PB6F19	AA6
IO169PB5F15	AC13	IO187NB5F17	AE7	IO204NB6F19	Y5
IO170NB5F15	AJ10	IO187PB5F17	AE8	IO204PB6F19	AA5
IO170PB5F15	AJ11	IO188NB5F17	AF6	IO205NB6F19	W8
IO171NB5F16	AG11	IO188PB5F17	AF7	IO205PB6F19	Y8
IO171PB5F16	AG12	IO189NB5F17	AD8	IO206NB6F19	AA4

FG896		FG896	
AX1000 Function	**Pin Number**	**AX1000 Function**	**Pin Number**
VCCIB2	L22	VCCIB5	AK3
VCCIB2	M21	VCCIB6	AA9
VCCIB2	M22	VCCIB6	AH1
VCCIB2	N21	VCCIB6	AH2
VCCIB2	P21	VCCIB6	T10
VCCIB2	R21	VCCIB6	U10
VCCIB3	AA22	VCCIB6	V10
VCCIB3	AH29	VCCIB6	W10
VCCIB3	AH30	VCCIB6	W9
VCCIB3	T21	VCCIB6	Y10
VCCIB3	U21	VCCIB6	Y9
VCCIB3	V21	VCCIB7	C1
VCCIB3	W21	VCCIB7	C2
VCCIB3	W22	VCCIB7	K9
VCCIB3	Y21	VCCIB7	L10
VCCIB3	Y22	VCCIB7	L9
VCCIB4	AA16	VCCIB7	M10
VCCIB4	AA17	VCCIB7	M9
VCCIB4	AA18	VCCIB7	N10
VCCIB4	AA19	VCCIB7	P10
VCCIB4	AA20	VCCIB7	R10
VCCIB4	AB19	VCOMPLA	F14
VCCIB4	AB20	VCOMPLB	J15
VCCIB4	AB21	VCOMPLC	F17
VCCIB4	AJ28	VCOMPLD	H16
VCCIB4	AK28	VCOMPLE	AF17
VCCIB5	AA11	VCOMPLF	AD16
VCCIB5	AA12	VCOMPLG	AF14
VCCIB5	AA13	VCOMPLH	AB15
VCCIB5	AA14	VPUMP	G24
VCCIB5	AA15		
VCCIB5	AB10		
VCCIB5	AB11		
VCCIB5	AB12		
VCCIB5	AJ3		

FG896		FG896		FG896	
AX2000 Function	**Pin Number**	**AX2000 Function**	**Pin Number**	**AX2000 Function**	**Pin Number**
IO180PB4F16	AG24	IO201PB4F18	AJ19	IO225NB5F21	AH11
IO181NB4F17	AK24	IO202NB4F18	AC18	IO225PB5F21	AH12
IO181PB4F17	AK25	IO202PB4F18	AB18	IO226NB5F21	AC13
IO182NB4F17	AD22	IO206NB4F19	AE18	IO226PB5F21	AD13
IO182PB4F17	AC22	IO206PB4F19	AD18	IO227NB5F21	AE12
IO183NB4F17	AF22	IO207NB4F19	AJ17	IO227PB5F21	AE13
IO183PB4F17	AF23	IO207PB4F19	AJ18	IO228NB5F21	AG11
IO184NB4F17	AE21	IO208NB4F19	AE17	IO228PB5F21	AG12
IO184PB4F17	AE22	IO208PB4F19	AD17	IO229NB5F21	AK11
IO185NB4F17	AJ23	IO209NB4F19	AK17	IO229PB5F21	AK12
IO185PB4F17	AJ24	IO210NB4F19	AC17	IO230NB5F21	AC12
IO187NB4F17	AH22	IO210PB4F19	AB17	IO230PB5F21	AD12
IO187PB4F17	AH23	IO211NB4F19	AJ16	IO232NB5F21	AE11
IO188NB4F17	AD21	IO211PB4F19	AK16	IO232PB5F21	AF11
IO188PB4F17	AC21	IO212NB4F19/CLKEN	AG18	IO233NB5F21	AJ10
IO189PB4F17	AK22	IO212PB4F19/CLKEP	AH18	IO233PB5F21	AJ11
IO190NB4F17	AF20	IO213NB4F19/CLKFN	AG16	IO234NB5F21	AC11
IO190PB4F17	AF21	IO213PB4F19/CLKFP	AG17	IO234PB5F21	AD11
IO191NB4F17	AG21	**Bank 5**		IO236NB5F22	AK9
IO191PB4F17	AG22	IO214NB5F20/CLKGN	AG14	IO236PB5F22	AK10
IO192NB4F17	AE19	IO214PB5F20/CLKGP	AG15	IO237NB5F22	AG9
IO192PB4F17	AE20	IO215NB5F20/CLKHN	AG13	IO237PB5F22	AG10
IO195NB4F18	AK21	IO215PB5F20/CLKHP	AH13	IO238NB5F22	AF9
IO195PB4F18	AJ21	IO216NB5F20	AB14	IO238PB5F22	AF10
IO196NB4F18	AD19	IO216PB5F20	AC15	IO239NB5F22	AH8
IO196PB4F18	AD20	IO217NB5F20	AK15	IO239PB5F22	AH9
IO197NB4F18	AJ20	IO217PB5F20	AJ15	IO240NB5F22	AC10
IO197PB4F18	AK20	IO218NB5F20	AE14	IO240PB5F22	AD10
IO198NB4F18	AC19	IO218PB5F20	AD14	IO242NB5F22	AE9
IO198PB4F18	AC20	IO219NB5F20	AK14	IO242PB5F22	AE10
IO199NB4F18	AG19	IO219PB5F20	AJ14	IO243NB5F22	AJ7
IO199PB4F18	AG20	IO222NB5F20	AB13	IO243PB5F22	AJ8
IO200NB4F18	AH19	IO222PB5F20	AC14	IO244NB5F22	AK6
IO200PB4F18	AH20	IO223NB5F21	AJ12	IO244PB5F22	AK7
IO201NB4F18	AK19	IO223PB5F21	AJ13	IO245NB5F23	AF8

FG896		FG896	
AX2000 Function	**Pin Number**	**AX2000 Function**	**Pin Number**
VCCIB3	AH30	VCCIB6	W9
VCCIB3	T21	VCCIB6	Y10
VCCIB3	U21	VCCIB6	Y9
VCCIB3	V21	VCCIB7	C1
VCCIB3	W21	VCCIB7	C2
VCCIB3	W22	VCCIB7	K9
VCCIB3	Y21	VCCIB7	L10
VCCIB3	Y22	VCCIB7	L9
VCCIB4	AA16	VCCIB7	M10
VCCIB4	AA17	VCCIB7	M9
VCCIB4	AA18	VCCIB7	N10
VCCIB4	AA19	VCCIB7	P10
VCCIB4	AA20	VCCIB7	R10
VCCIB4	AB19	VCCPLA	G14
VCCIB4	AB20	VCCPLB	H15
VCCIB4	AB21	VCCPLC	G17
VCCIB4	AJ28	VCCPLD	J16
VCCIB4	AK28	VCCPLE	AH17
VCCIB5	AA11	VCCPLF	AC16
VCCIB5	AA12	VCCPLG	AH14
VCCIB5	AA13	VCCPLH	AD15
VCCIB5	AA14	VCOMPLA	F14
VCCIB5	AA15	VCOMPLB	J15
VCCIB5	AB10	VCOMPLC	F17
VCCIB5	AB11	VCOMPLD	H16
VCCIB5	AB12	VCOMPLE	AF17
VCCIB5	AJ3	VCOMPLF	AD16
VCCIB5	AK3	VCOMPLG	AF14
VCCIB6	AA9	VCOMPLH	AB15
VCCIB6	AH1	VPUMP	G24
VCCIB6	AH2		
VCCIB6	T10		
VCCIB6	U10		
VCCIB6	V10		
VCCIB6	W10		

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FG1152		FG1152		FG1152	
AX2000 Function	**Pin Number**	**AX2000 Function**	**Pin Number**	**AX2000 Function**	**Pin Number**
Bank 0		IO17NB0F1	F12	IO34PB0F3	D14
IO00NB0F0	D6	IO17PB0F1	F11	IO35NB0F3	A15
IO00PB0F0	C6	IO18NB0F1	E11	IO35PB0F3	B15
IO01NB0F0	H10	IO18PB0F1	E10	IO36NB0F3	B16
IO01PB0F0	H9	IO19NB0F1	F13	IO36PB0F3	A16
IO02NB0F0	F8	IO19PB0F1	G13	IO37NB0F3	G16
IO02PB0F0	G8	IO20NB0F1	A10	IO37PB0F3	G15
IO03NB0F0	A6	IO20PB0F1	A9	IO38NB0F3	D16
IO03PB0F0	B6	IO21NB0F1	K14	IO38PB0F3	C16
IO04NB0F0	C7	IO21PB0F1	K13	IO39NB0F3	K16
IO04PB0F0	D7	IO22NB0F2	B11	IO39PB0F3	L16
IO05NB0F0	K10	IO22PB0F2	B10	IO40NB0F3	D17
IO05PB0F0	J10	IO23NB0F2	C12	IO40PB0F3	C17
IO06NB0F0	F9	IO23PB0F2	C11	IO41NB0F3/HCLKAN	E16
IO06PB0F0	G9	IO24NB0F2	A12	IO41PB0F3/HCLKAP	F16
IO07NB0F0	F10	IO24PB0F2	A11	IO42NB0F3/HCLKBN	G17
IO07PB0F0	G10	IO25NB0F2	H14	IO42PB0F3/HCLKBP	F17
IO08NB0F0	E9	IO25PB0F2	J14	**Bank 1**	
IO08PB0F0	E8	IO26NB0F2	D13	IO43NB1F4/HCLKCN	G19
IO09NB0F0	J11	IO26PB0F2	D12	IO43PB1F4/HCLKCP	G18
IO09PB0F0	K11	IO27NB0F2	F14	IO44NB1F4/HCLKDN	E19
IO10NB0F0	C8	IO27PB0F2	G14	IO44PB1F4/HCLKDP	F19
IO10PB0F0	D8	IO28NB0F2	E14	IO45NB1F4	C18
IO11NB0F0	K12	IO28PB0F2	E13	IO45PB1F4	D18
IO11PB0F0	J12	IO29NB0F2	B13	IO46NB1F4	A18
IO12NB0F1	G11	IO29PB0F2	B12	IO46PB1F4	B18
IO12PB0F1	H11	IO30NB0F2	C14	IO47NB1F4	K19
IO13NB0F1	G12	IO30PB0F2	C13	IO47PB1F4	L19
IO13PB0F1	H12	IO31NB0F2	H15	IO48NB1F4	C19
IO14NB0F1	A7	IO31PB0F2	J15	IO48PB1F4	D19
IO14PB0F1	B7	IO32NB0F2	A14	IO49NB1F4	K20
IO15NB0F1	H13	IO32PB0F2	B14	IO49PB1F4	L20
IO15PB0F1	J13	IO33NB0F2	K15	IO50NB1F4	A19
IO16NB0F1	C9	IO33PB0F2	L15	IO50PB1F4	B19
IO16PB0F1	D9	IO34NB0F3	D15	IO51NB1F4	H20

PQ208			PQ208			PQ208	
AX500 Function	**Pin Number**		**AX500 Function**	**Pin Number**		**AX500 Function**	**Pin Number**
Bank 0			IO61PB2F5	134		IO105PB5F10/CLKGP	77
IO03NB0F0	198		IO62NB2F5	131		IO106NB5F10/CLKHN	70
IO03PB0F0	199		IO62PB2F5	133		IO106PB5F10/CLKHP	71
IO04NB0F0	197		**Bank 3**			IO107NB5F10	66
IO19NB0F1/HCLKAN	191		IO63NB3F6	127		IO107PB5F10	67
IO19PB0F1/HCLKAP	192		IO63PB3F6	129		IO119NB5F11	62
IO20NB0F1/HCLKBN	185		IO64NB3F6	126		IO121NB5F11	60
IO20PB0F1/HCLKBP	186		IO64PB3F6	128		IO121PB5F11	61
Bank 1			IO66NB3F6	122		IO123NB5F11	56
IO21NB1F2/HCLKCN	180		IO66PB3F6	123		IO123PB5F11	57
IO21PB1F2/HCLKCP	181		IO68NB3F6	120		IO125NB5F11	54
IO22NB1F2/HCLKDN	174		IO68PB3F6	121		IO125PB5F11	55
IO22PB1F2/HCLKDP	175		IO77NB3F7	116		**Bank 6**	
IO23NB1F2	170		IO77PB3F7	117		IO127NB6F12	47
IO23PB1F2	171		IO79NB3F7	114		IO127PB6F12	49
IO37NB1F3	165		IO79PB3F7	115		IO128NB6F12	48
IO37PB1F3	166		IO81NB3F7	110		IO128PB6F12	50
IO39NB1F3	161		IO81PB3F7	111		IO129NB6F12	42
IO39PB1F3	162		IO82NB3F7	108		IO129PB6F12	43
IO41NB1F3	159		IO82PB3F7	109		IO130PB6F12	44
IO41PB1F3	160		IO83NB3F7	106		IO132NB6F12	40
Bank 2			IO83PB3F7	107		IO132PB6F12	41
IO43NB2F4	151		**Bank 4**			IO141NB6F13	35
IO43PB2F4	153		IO84PB4F8	103		IO141PB6F13	36
IO44NB2F4	152		IO85NB4F8	100		IO142PB6F13	37
IO44PB2F4	154		IO86NB4F8	101		IO143NB6F13	33
IO45PB2F4	148		IO86PB4F8	102		IO143PB6F13	34
IO46NB2F4	146		IO87NB4F8	96		IO145NB6F13	28
IO46PB2F4	147		IO87PB4F8	97		IO145PB6F13	30
IO48NB2F4	144		IO101NB4F9	91		IO146NB6F13	27
IO48PB2F4	145		IO101PB4F9	92		IO146PB6F13	29
IO57NB2F5	139		IO103NB4F9/CLKEN	87		**Bank 7**	
IO57PB2F5	140		IO103PB4F9/CLKEP	88		IO147NB7F14	23
IO58PB2F5	141		IO104NB4F9/CLKFN	81		IO147PB7F14	25
IO59NB2F5	137		IO104PB4F9/CLKFP	82		IO148NB7F14	22
IO59PB2F5	138		**Bank 5**			IO148PB7F14	24
IO61NB2F5	132		IO105NB5F10/CLKGN	76		IO150NB7F14	18