# Microchip Technology - AX250-1FGG484I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4224 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 55296 |
| Number of I/O | 248 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ax250-1fgg484i |

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The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).

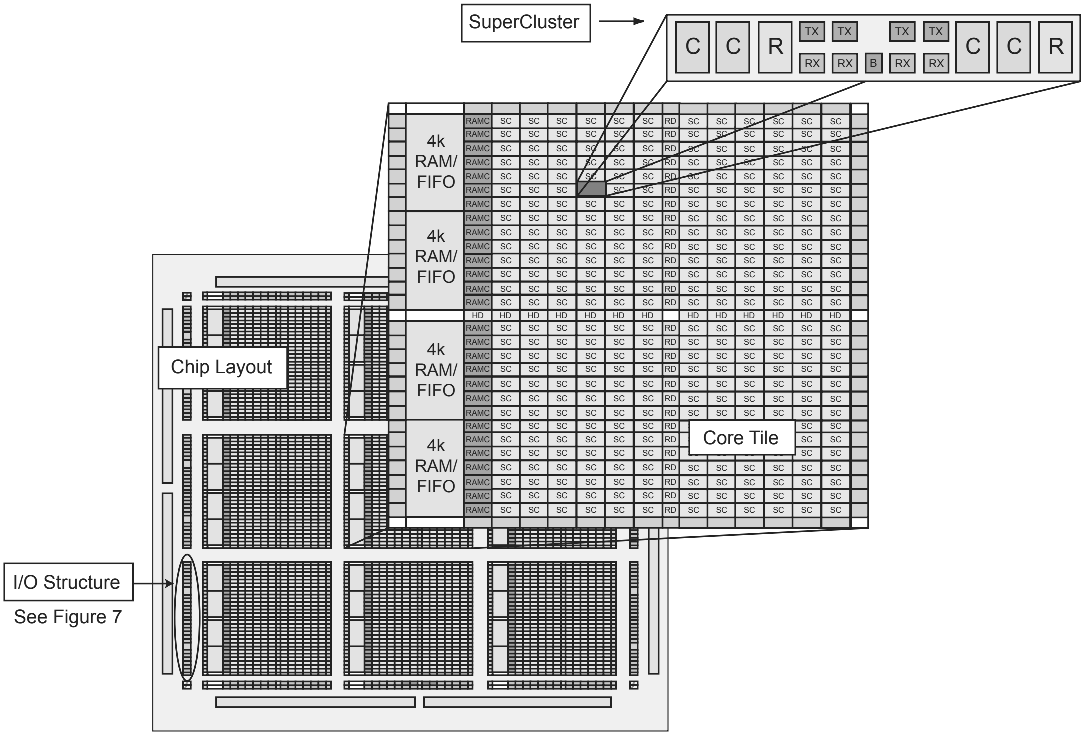

*Figure 1-6 •* **AX Device Architecture (AX1000 shown)**

## Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

# Thermal Characteristics

## Introduction

The temperature variable in Microsemi's Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature. EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_a$$

*EQ 1*

Where:

$T_a$ = Ambient Temperature
$\Delta T$ = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P$$

*EQ 2*

Where:

P = Power
$\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located under Table 2-6 on page 2-7.

## Package Thermal Characteristics

The device junction-to-case thermal characteristic is $\theta_{jc}$, and the junction-to-ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates. $\theta_{jc}$ values are provided for reference. The absolute maximum junction temperature is 125°C.

The maximum power dissipation allowed for commercial- and industrial-grade devices is a function of $\theta_{ja}$. A sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°\text{C}) - \text{Max. ambient temp. } (°\text{C})}{\theta_{ja}(°\text{C/W})} = \frac{125°\text{C} - 70°\text{C}}{13.6°\text{C/W}} = 4.04 \text{ W}$$

The maximum power dissipation allowed for Military temperature and Mil-Std 883B devices is specified as a function of $\theta_{jc}$.

***Table 2-6 •*** **Package Thermal Characteristics**

| Package Type | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ Still Air | $\theta_{ja}$ 1.0m/s | $\theta_{ja}$ 2.5m/s | Units |
|---|---|---|---|---|---|---|
| Chip Scale Package (CSP) | 180 | N/A | 57.8 | 51.0 | 50 | °C/W |
| Plastic Quad Flat Pack (PQFP) | 208 | 8.0 | 26 | 23.5 | 20.9 | °C/W |
| Plastic Ball Grid Array (PBGA) | 729 | 2.2 | 13.7 | 10.6 | 9.6 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 256 | 3.0 | 26.6 | 22.8 | 21.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 324 | 3.0 | 25.8 | 22.1 | 20.9 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 484 | 3.2 | 20.5 | 17.0 | 15.9 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 676 | 3.2 | 16.4 | 13.0 | 12.0 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 896 | 2.4 | 13.6 | 10.4 | 9.4 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 1152 | 1.8 | 12.0 | 8.9 | 7.9 | °C/W |
| Ceramic Quad Flat Pack (CQFP)[1] | 208 | 2.0 | 22 | 19.8 | 18.0 | °C/W |
| Ceramic Quad Flat Pack (CQFP)[1] | 352 | 2.0 | 17.9 | 16.1 | 14.7 | °C/W |
| Ceramic Column Grid Array (CCGA)[2] | 624 | 6.5 | 8.9 | 8.5 | 8 | °C/W |

*Notes:*

1. *$\theta_{jc}$ for the 208-pin and 352-pin CQFP refers to the thermal resistance between the junction and the bottom of the package.*
2. *$\theta_{jc}$ for the 624-pin CCGA refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board ($\theta_{jb}$) for CCGA 624 package is 3.4°C/W.*

## Timing Characteristics

Axcelerator devices are manufactured in a CMOS process, therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-7 should be applied to all timing data contained within this datasheet.

***Table 2-7 •*** **Temperature and Voltage Timing Derating Factors**
**(Normalized to Worst-Case Commercial, $T_J$ = 70°C, VCCA = 1.425V)**

| | Junction Temperature | | | | | | |
|---|---|---|---|---|---|---|---|
| **VCCA** | **–55°C** | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **125°C** |
| 1.4 V | 0.83 | 0.86 | 0.91 | 0.96 | 1.02 | 1.05 | 1.15 |
| 1.425 V | 0.82 | 0.84 | 0.90 | 0.94 | 1.00 | 1.04 | 1.13 |
| 1.5 V | 0.78 | 0.80 | 0.85 | 0.89 | 0.95 | 0.98 | 1.07 |
| 1.575 V | 0.74 | 0.76 | 0.81 | 0.85 | 0.90 | 0.94 | 1.02 |
| 1.6 V | 0.73 | 0.75 | 0.80 | 0.84 | 0.89 | 0.92 | 1.01 |

*Notes:*

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 175°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4V and 1.6V.*

All timing numbers listed in this datasheet represent sample timing characteristics of Axcelerator devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Microsemi's Designer software after place-and-route.

# User I/Os[2]

## Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-8 on page 2-12 contains the I/O standards supported by the Axcelerator family, and Table 2-10 on page 2-12 compares the features of the different I/O standards.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (Figure 2-6 on page 2-18). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules:

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.
- Dedicated I/O pins such as GND and VCCI are counted as part of the 16.
- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.
- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3 V.

A user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.
- Use generic I/O macros and then use Designer’s PinEditor to specify the desired I/O standards (please note that this is not applicable to differential standards).
- A combination of the first two methods.

Refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

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*2. Do not use an external resister to pull the I/O above $V_{CCI}$ for a higher logic “1” voltage level. The desired higher logic “1” voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above $V_{CCI}$.*

## 5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

*EQ 3*

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

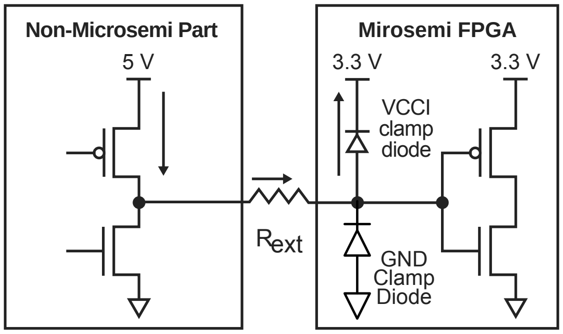

***Figure 2-3 •*** **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

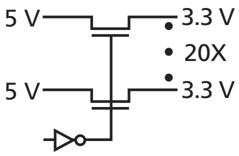

***Figure 2-4 •*** **Bus Switch IDTQS32X2384**

## Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

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[3] *The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.*

### Timing Characteristics

***Table 2-22*** **• 3.3 V LVTTL I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **LVTTL Output Drive Strength = 1 (8 mA) / Low Slew Rate** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.68 | | 1.92 | | 2.26 | ns |
| $t_{PY}$ | Output Buffer | | 14.28 | | 16.27 | | 19.13 | ns |
| $t_{ENZL}$ | Enable to Pad Delay through the Output Buffer—Z to Low | | 15.25 | | 17.37 | | 20.42 | ns |
| $t_{ENZH}$ | Enable to Pad Delay through the Output Buffer—Z to High | | 14.26 | | 16.24 | | 19.09 | ns |
| $t_{ENLZ}$ | Enable to Pad Delay through the Output Buffer—Low to Z | | 1.56 | | 1.57 | | 1.58 | ns |
| $t_{ENHZ}$ | Enable to Pad Delay through the Output Buffer—High to Z | | 1.95 | | 1.96 | | 1.97 | ns |
| $t_{IOCLKQ}$ | Sequential Clock-to-Q for the I/O Input Register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{IOCLKY}$ | Clock-to-output Y for the I/O Output Register and the I/O Enable Register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 039 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |

***Table 2-69* • AX2000 Predicted Routing Delays**
**Worst-Case Commercial Conditions VCCA = 1.425 V, $T_J$ = 70°C**

| | | –2 Speed | –1 Speed | Std Speed | |
|---|---|---|---|---|---|
| **Parameter** | **Description** | **Typical** | **Typical** | **Typical** | **Units** |
| **Predicted Routing Delays** | | | | | |
| $t_{DC}$ | DirectConnect Routing Delay, FO1 | 0.12 | 0.13 | 0.15 | ns |
| $t_{FC}$ | FastConnect Routing Delay, FO1 | 0.35 | 0.39 | 0.46 | ns |
| $t_{RD1}$ | Routing delay for FO1 | 0.50 | 0.56 | 0.66 | ns |
| $t_{RD2}$ | Routing delay for FO2 | 0.59 | 0.67 | 0.79 | ns |
| $t_{RD3}$ | Routing delay for FO3 | 0.70 | 0.80 | 0.94 | ns |
| $t_{RD4}$ | Routing delay for FO4 | 0.76 | 0.87 | 1.02 | ns |
| $t_{RD5}$ | Routing delay for FO5 | 0.98 | 1.11 | 1.31 | ns |
| $t_{RD6}$ | Routing delay for FO6 | 1.48 | 1.68 | 1.97 | ns |
| $t_{RD7}$ | Routing delay for FO7 | 1.65 | 1.87 | 2.20 | ns |
| $t_{RD8}$ | Routing delay for FO8 | 1.73 | 1.96 | 2.31 | ns |
| $t_{RD16}$ | Routing delay for FO16 | 2.58 | 2.92 | 3.44 | ns |
| $t_{RD32}$ | Routing delay for FO32 | 4.24 | 4.81 | 5.65 | ns |

***Table 2-83* • South PLL Connections**

| **CLK1** | **CLK2** |
|---|---|
| CLK1 | Routed net |
| CLK1 | Unused |
| CLK2 | CLK1 |
| CLK2 | Routed net |
| CLK2 | Both CLK1 and routed net |
| CLK2 | Unused |
| Unused | CLK1 |
| Unused | Routed net |
| Unused | Both CLK1 and routed net |
| Unused | Unused |
| Routed net | CLK1 |
| Routed net | Unused |
| Both CLK1 and CLK2 | Routed net |
| Both CLK1 and CLK2 | Unused |
| Both CLK1 and routed net | Unusable |
| Both CLK2 and routed net | CLK1 |
| Both CLK2 and routed net | Unused |
| CLK1, CLK2, and routed net | Unusable |

*Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).*

## Special PLL Macros

Table 2-84 shows the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

***Table 2-84*** **• PLL Special Macros**

| Macro Name | Usage |
|---|---|
| PLLINT | Connects RefCLK to a regular routed net or a pad. |
| PLLRCLK | Connects CLK1 or CLK2 to the CLK network. |
| PLLHCLK | Connects CLK1 or CLK2 to the HCLK network. |
| PLLOUT | Connects CLK1 or CLK2 to a regular routed net. |

***Table 2-85*** **• Electrical Specifications**

| Parameter | Value | Notes |
|---|---|---|
| **Frequency Ranges** | | |
| Reference Frequency (min.) | 14 MHz | Lowest input frequency |
| Reference Frequency (max.) | 200 MHz | Highest input frequency |
| OSC Frequency (min.) | 20 MHz | Lowest output frequency |
| OSC Frequency (max.) | 1 GHz | Highest output frequency |
| **Jitter** | | |
| Long-Term Jitter (max.) | 1% | Percentage of period, low reference clock frequencies |
| Long-Term Jitter (max.) | 100ps | High reference clock frequencies |
| Short-Term Jitter (max.) | 50ps+1% | Percentage of output frequency |
| **Acquisition Time (lock) from Cold Start** | | |
| Acquisition Time (max.)* | 400 cycles | Period of low reference clock frequencies |
| Acquisition Time (max.)* | 1.5 µs | High reference clock frequencies |
| **Power Consumption** | | |
| Analog Supply Current (low freq.) | 200 µA | Current at minimum oscillator frequency |
| Analog Supply Current (high freq.) | 200 µA | Frequency-dependent current |
| Digital Supply Current (low freq.) | 0.5 µA/MHz | Current at maximum oscillator frequency, unloaded |
| Digital Supply Current (high freq.) | 1 µA/MHz | Frequency-dependent current |
| **Duty Cycle** | | |
| Minimum Output Duty Cycle | 45% | |
| Maximum Output Duty Cycle | 55% | |

*Note: *The lock bit remains Low until RefCLK reaches the minimum input frequency.*

## Timing Characteristics

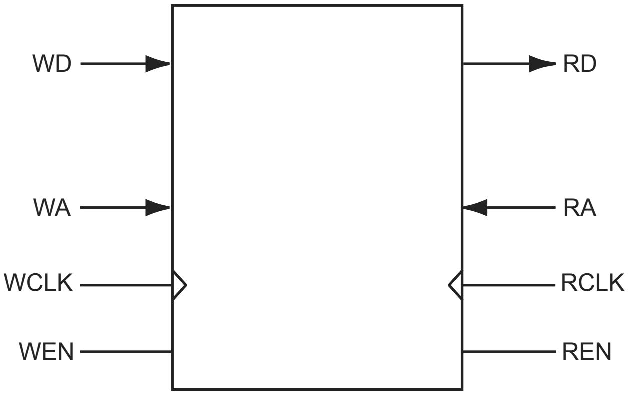


*Figure 2-58 •* **SRAM Model**

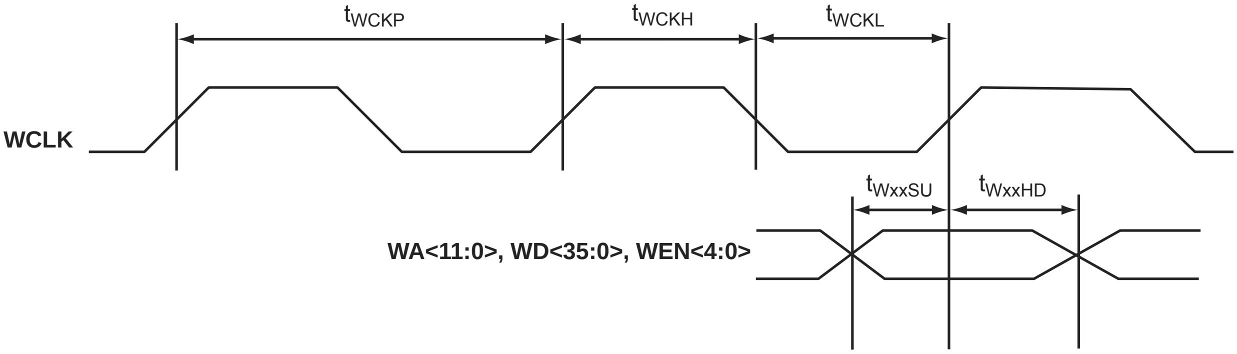


*Figure 2-59 •* **RAM Write Timing Waveforms**

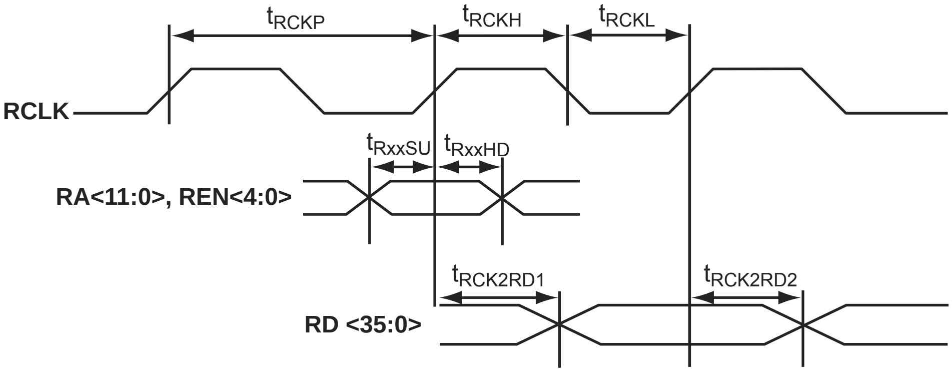


*Figure 2-60 •* **RAM Read Timing Waveforms**

Figure 2-63 illustrates flag generation.

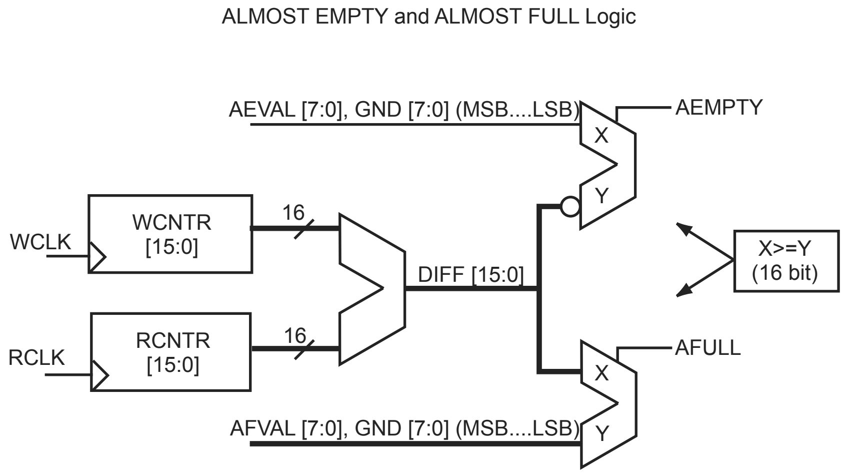


***Figure 2-63* • ALMOST-EMPTY and ALMOST-FULL Logic**

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-95).

***Table 2-95* • Number of Available Configuration Bits**

| Number of Blocks | Block DxW | Number of AEVAL/AFVAL Bits |
|---|---|---|
| 1 | 1x1 | 4 |
| 2 | 1x2 | 4 |
| 2 | 2x1 | 5 |
| 4 | 1x4 | 4 |
| 4 | 2x2 | 5 |
| 4 | 4x1 | 6 |
| 8 | 1x8 | 4 |
| 8 | 2x4 | 5 |
| 8 | 4x2 | 6 |
| 8 | 8x1 | 7 |
| 16 | 1x16 | 4 |
| 16 | 2x8 | 5 |
| 16 | 4x4 | 6 |
| 16 | 8x2 | 7 |
| 16 | 16x1 | 8 |

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-100.

| FG324 | |
|---|---|
| AX125 Function | Pin Number |
| **Bank 0** | |
| IO00NB0F0 | C5 |
| IO00PB0F0 | C4 |
| IO01NB0F0 | A3 |
| IO01PB0F0 | A2 |
| IO02NB0F0 | C7 |
| IO02PB0F0 | C6 |
| IO03NB0F0 | B5 |
| IO03PB0F0 | B4 |
| IO04NB0F0 | A5 |
| IO04PB0F0 | A4 |
| IO05NB0F0 | A7 |
| IO05PB0F0 | A6 |
| IO06NB0F0 | B7 |
| IO06PB0F0 | B6 |
| IO07NB0F0/HCLKAN | C9 |
| IO07PB0F0/HCLKAP | C8 |
| IO08NB0F0/HCLKBN | B10 |
| IO08PB0F0/HCLKBP | B9 |
| **Bank 1** | |
| IO09NB1F1/HCLKCN | D11 |
| IO09PB1F1/HCLKCP | D10 |
| IO10NB1F1/HCLKDN | C12 |
| IO10PB1F1/HCLKDP | C11 |
| IO11NB1F1 | A15 |
| IO11PB1F1 | A14 |
| IO12NB1F1 | B14 |
| IO12PB1F1 | B13 |
| IO13NB1F1 | A17 |
| IO13PB1F1 | A16 |
| IO14NB1F1 | D13 |
| IO14PB1F1 | D12 |
| IO15NB1F1 | C14 |
| IO15PB1F1 | C13 |
| IO16NB1F1 | B16 |
| IO16PB1F1 | C15 |
| IO17NB1F1 | E14 |
| IO17PB1F1 | E13 |
| **Bank 2** | |
| IO18NB2F2 | G14 |
| IO18PB2F2 | F14 |
| IO19NB2F2 | D16 |
| IO19PB2F2 | D15 |
| IO20NB2F2 | C18 |
| IO20PB2F2 | B18 |
| IO21NB2F2 | D17 |
| IO21PB2F2 | C17 |
| IO22NB2F2 | F17 |
| IO22PB2F2 | E17 |
| IO23NB2F2 | G16 |
| IO23PB2F2 | F16 |
| IO24NB2F2 | E18 |
| IO24PB2F2 | D18 |
| IO25NB2F2 | G18 |
| IO25PB2F2 | F18 |
| IO26NB2F2 | H17 |
| IO26PB2F2 | G17 |
| IO27NB2F2 | J16 |
| IO27PB2F2 | H16 |
| IO28NB2F2 | J18 |
| IO28PB2F2 | H18 |
| IO29NB2F2 | K17 |
| IO29PB2F2 | J17 |
| **Bank 3** | |
| IO30NB3F3 | N18 |
| IO30PB3F3 | M18 |
| IO31NB3F3 | L18 |
| IO31PB3F3 | K18 |
| IO32NB3F3 | L16 |
| IO32PB3F3 | L17 |
| IO33NB3F3 | R18 |
| IO33PB3F3 | P18 |
| IO34NB3F3 | N15 |
| IO34PB3F3 | M15 |
| IO35NB3F3 | M16 |
| IO35PB3F3 | M17 |
| IO36NB3F3 | P16 |
| IO36PB3F3 | N16 |
| IO37NB3F3 | R17 |
| IO37PB3F3 | P17 |
| IO38NB3F3 | N14 |
| IO38PB3F3 | M14 |
| IO39NB3F3 | U18 |
| IO39PB3F3 | T18 |
| IO40NB3F3 | R16 |
| IO40PB3F3 | T17 |
| IO41NB3F3 | P13 |
| IO41PB3F3 | P14 |
| **Bank 4** | |
| IO42NB4F4 | T13 |
| IO42PB4F4 | T14 |
| IO43NB4F4 | U15 |
| IO43PB4F4 | T15 |
| IO44NB4F4 | U13 |
| IO44PB4F4 | U14 |
| IO45NB4F4 | V15 |
| IO45PB4F4 | V16 |
| IO46NB4F4 | V13 |
| IO46PB4F4 | V14 |
| IO47NB4F4 | V12 |
| IO47PB4F4 | U12 |
| IO48NB4F4 | V10 |
| IO48PB4F4 | V11 |
| IO49NB4F4/CLKEN | T10 |
| IO49PB4F4/CLKEP | T11 |

| FG324 | |
|---|---|
| AX125 Function | Pin Number |
| GND | R4 |
| GND | T16 |
| GND | T3 |
| GND | U17 |
| GND | U2 |
| GND | V1 |
| GND | V18 |
| GND/LP | E5 |
| NC | A10 |
| NC | A11 |
| NC | A12 |
| NC | A13 |
| NC | A8 |
| NC | A9 |
| NC | B12 |
| NC | F15 |
| NC | F4 |
| NC | G15 |
| NC | G4 |
| NC | H14 |
| NC | H15 |
| NC | H5 |
| NC | J1 |
| NC | J14 |
| NC | J15 |
| NC | J5 |
| NC | K14 |
| NC | K15 |
| NC | K5 |
| NC | L14 |
| NC | L15 |
| NC | L5 |
| NC | M4 |
| NC | M5 |
| NC | N17 |

| FG324 | |
|---|---|
| AX125 Function | Pin Number |
| NC | N4 |
| NC | N5 |
| NC | R12 |
| NC | R13 |
| NC | R6 |
| NC | R7 |
| NC | T12 |
| NC | T6 |
| NC | U16 |
| NC | V17 |
| PRA | E9 |
| PRB | D9 |
| PRC | P10 |
| PRD | R10 |
| TCK | E6 |
| TDI | D7 |
| TDO | D5 |
| TMS | D4 |
| TRST | D6 |
| VCCA | E15 |
| VCCA | G10 |
| VCCA | G11 |
| VCCA | G5 |
| VCCA | G8 |
| VCCA | G9 |
| VCCA | H12 |
| VCCA | H7 |
| VCCA | J12 |
| VCCA | J7 |
| VCCA | K12 |
| VCCA | K7 |
| VCCA | L12 |
| VCCA | L7 |
| VCCA | M10 |
| VCCA | M11 |

| FG324 | |
|---|---|
| AX125 Function | Pin Number |
| VCCA | M8 |
| VCCA | M9 |
| VCCA | P4 |
| VCCA | R15 |
| VCCPLA | D8 |
| VCCPLB | E7 |
| VCCPLC | B11 |
| VCCPLD | E11 |
| VCCPLE | R11 |
| VCCPLF | P12 |
| VCCPLG | U8 |
| VCCPLH | P8 |
| VCCDA | B3 |
| VCCDA | D14 |
| VCCDA | E10 |
| VCCDA | J2 |
| VCCDA | K16 |
| VCCDA | P15 |
| VCCDA | P9 |
| VCCDA | R5 |
| VCCIB0 | F7 |
| VCCIB0 | F8 |
| VCCIB0 | F9 |
| VCCIB1 | F10 |
| VCCIB1 | F11 |
| VCCIB1 | F12 |
| VCCIB2 | G13 |
| VCCIB2 | H13 |
| VCCIB2 | J13 |
| VCCIB3 | K13 |
| VCCIB3 | L13 |
| VCCIB3 | M13 |
| VCCIB4 | N10 |
| VCCIB4 | N11 |
| VCCIB4 | N12 |

| FG676 | |
|---|---|
| AX500 Function | Pin Number |
| IO51NB2F4 | L20 |
| IO51PB2F4 | L21 |
| IO52NB2F5 | K26 |
| IO52PB2F5 | J26 |
| IO53NB2F5 | L23 |
| IO53PB2F5 | L22 |
| IO54NB2F5 | L24 |
| IO54PB2F5 | K24 |
| IO55NB2F5 | M20 |
| IO55PB2F5 | M21 |
| IO56NB2F5 | L26 |
| IO56PB2F5 | L25 |
| IO57NB2F5 | M23 |
| IO57PB2F5 | M22 |
| IO58NB2F5 | M26 |
| IO58PB2F5 | M25 |
| IO59NB2F5 | N22 |
| IO59PB2F5 | N23 |
| IO60NB2F5 | N24 |
| IO60PB2F5 | M24 |
| IO61NB2F5 | N20 |
| IO61PB2F5 | N21 |
| IO62NB2F5 | P25 |
| IO62PB2F5 | N25 |
| **Bank 3** | |
| IO63NB3F6 | T26 |
| IO63PB3F6 | R26 |
| IO64NB3F6 | R24 |
| IO64PB3F6 | P24 |
| IO65NB3F6 | P20 |
| IO65PB3F6 | P21 |
| IO66NB3F6 | T25 |
| IO66PB3F6 | R25 |
| IO67NB3F6 | T23 |
| IO67PB3F6 | R23 |

| FG676 | |
|---|---|
| AX500 Function | Pin Number |
| IO68NB3F6 | V26 |
| IO68PB3F6 | U26 |
| IO69NB3F6 | V25 |
| IO69PB3F6 | U25 |
| IO70NB3F6 | Y25 |
| IO70PB3F6 | W25 |
| IO71NB3F6 | W24 |
| IO71PB3F6 | V24 |
| IO72NB3F6 | V23 |
| IO72PB3F6 | U23 |
| IO73NB3F6 | T21 |
| IO73PB3F6 | T20 |
| IO74NB3F7 | AA26 |
| IO74PB3F7 | Y26 |
| IO75NB3F7 | AA24 |
| IO75PB3F7 | Y24 |
| IO76NB3F7 | Y23 |
| IO76PB3F7 | W23 |
| IO77NB3F7 | V21 |
| IO77PB3F7 | U21 |
| IO78NB3F7 | AB25 |
| IO78PB3F7 | AA25 |
| IO79NB3F7 | AC26 |
| IO79PB3F7 | AB26 |
| IO80NB3F7 | AC24 |
| IO80PB3F7 | AB24 |
| IO81NB3F7 | AB23 |
| IO81PB3F7 | AA23 |
| IO82NB3F7 | AA22 |
| IO82PB3F7 | Y22 |
| IO83NB3F7 | AE26 |
| IO83PB3F7 | AD26 |
| **Bank 4** | |
| IO84NB4F8 | AB21 |
| IO84PB4F8 | AA21 |

| FG676 | |
|---|---|
| AX500 Function | Pin Number |
| IO85NB4F8 | AE23 |
| IO85PB4F8 | AE24 |
| IO86NB4F8 | AC21 |
| IO86PB4F8 | AC22 |
| IO87NB4F8 | AF22 |
| IO87PB4F8 | AF23 |
| IO88NB4F8 | AD22 |
| IO88PB4F8 | AD23 |
| IO89NB4F8 | AC19 |
| IO89PB4F8 | AC20 |
| IO90NB4F8 | AE21 |
| IO90PB4F8 | AE22 |
| IO91NB4F8 | AA17 |
| IO91PB4F8 | AA18 |
| IO92NB4F8 | AD20 |
| IO92PB4F8 | AD21 |
| IO93NB4F8 | AF20 |
| IO93PB4F8 | AF21 |
| IO94NB4F9 | AE19 |
| IO94PB4F9 | AE20 |
| IO95NB4F9 | AC17 |
| IO95PB4F9 | AC18 |
| IO96NB4F9 | AD18 |
| IO96PB4F9 | AD19 |
| IO97NB4F9 | AA16 |
| IO97PB4F9 | Y16 |
| IO98NB4F9 | AE17 |
| IO98PB4F9 | AE18 |
| IO99NB4F9 | AC16 |
| IO99PB4F9 | AB16 |
| IO100NB4F9 | AF17 |
| IO100PB4F9 | AF18 |
| IO101NB4F9 | AA15 |
| IO101PB4F9 | Y15 |
| IO102NB4F9 | AC15 |

| FG676 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| GND | R10 |
| GND | R11 |
| GND | R12 |
| GND | R13 |
| GND | R14 |
| GND | R15 |
| GND | R16 |
| GND | R17 |
| GND | T10 |
| GND | T11 |
| GND | T12 |
| GND | T13 |
| GND | T14 |
| GND | T15 |
| GND | T16 |
| GND | T17 |
| GND | U10 |
| GND | U11 |
| GND | U12 |
| GND | U13 |
| GND | U14 |
| GND | U15 |
| GND | U16 |
| GND | U17 |
| GND | V18 |
| GND | V9 |
| GND | W1 |
| GND | W19 |
| GND | W26 |
| GND | W8 |
| GND | Y20 |
| GND | Y7 |
| GND/LP | C2 |
| NC | A11 |
| NC | A21 |

| FG676 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| NC | A22 |
| NC | A24 |
| NC | A25 |
| NC | AA11 |
| NC | AA19 |
| NC | AA20 |
| NC | AA4 |
| NC | AA5 |
| NC | AA6 |
| NC | AA7 |
| NC | AA8 |
| NC | AA9 |
| NC | AB1 |
| NC | AB11 |
| NC | AB17 |
| NC | AB18 |
| NC | AB19 |
| NC | AB20 |
| NC | AB8 |
| NC | AB9 |
| NC | AC1 |
| NC | AC13 |
| NC | AC14 |
| NC | AC25 |
| NC | AD1 |
| NC | AD11 |
| NC | AD16 |
| NC | AD25 |
| NC | AE1 |
| NC | AF2 |
| NC | AF25 |
| NC | B11 |
| NC | B24 |
| NC | B4 |
| NC | C16 |

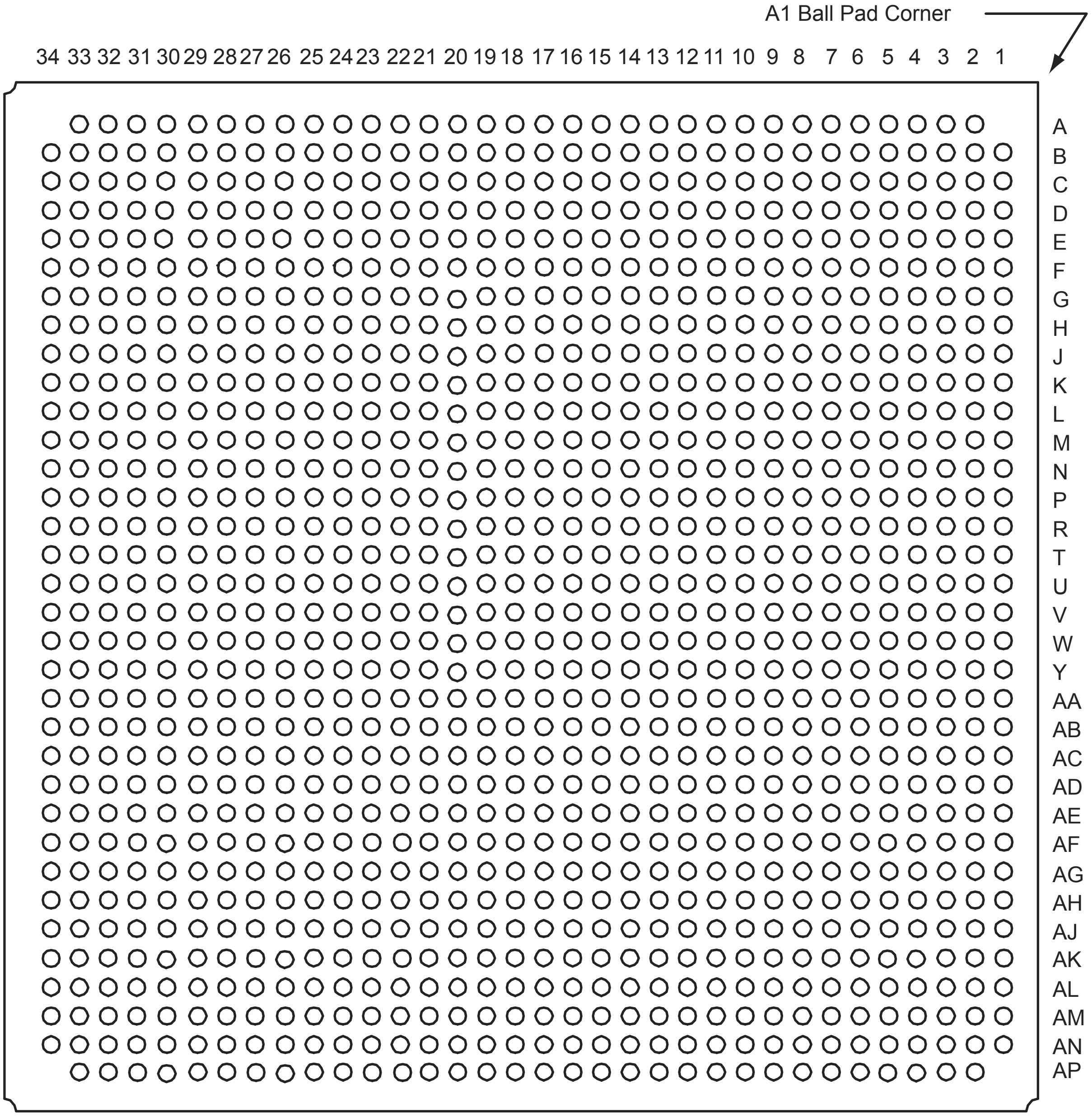
| FG676 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| NC | C4 |
| NC | D1 |
| NC | D13 |
| NC | D14 |
| NC | D17 |
| NC | D18 |
| NC | D2 |
| NC | D26 |
| NC | D3 |
| NC | D9 |
| NC | E1 |
| NC | E18 |
| NC | E23 |
| NC | E24 |
| NC | E26 |
| NC | E3 |
| NC | E4 |
| NC | E9 |
| NC | F1 |
| NC | F18 |
| NC | F20 |
| NC | F21 |
| NC | F22 |
| NC | F23 |
| NC | F24 |
| NC | F4 |
| NC | F6 |
| NC | F7 |
| NC | G21 |
| NC | G22 |
| NC | H21 |
| NC | H22 |
| NC | H23 |
| NC | H5 |
| NC | H6 |

| FG896 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO51PB1F4 | E21 |
| IO52NB1F4 | F22 |
| IO52PB1F4 | E22 |
| IO53NB1F4 | B25 |
| IO53PB1F4 | B24 |
| IO54NB1F5 | D24 |
| IO54PB1F5 | D23 |
| IO55NB1F5 | F23 |
| IO55PB1F5 | E23 |
| IO56NB1F5 | H21 |
| IO56PB1F5 | G21 |
| IO57NB1F5 | D25 |
| IO57PB1F5 | C25 |
| IO58NB1F5 | F24 |
| IO58PB1F5 | E24 |
| IO59NB1F5 | D26 |
| IO59PB1F5 | C26 |
| IO60NB1F5 | G23 |
| IO60PB1F5 | G22 |
| IO61NB1F5 | B27 |
| IO61PB1F5 | A27 |
| IO62NB1F5 | F25 |
| IO62PB1F5 | E25 |
| IO63NB1F5 | H23 |
| IO63PB1F5 | H22 |
| **Bank 2** | |
| IO64NB2F6 | K23 |
| IO64PB2F6 | J23 |
| IO65NB2F6 | J24 |
| IO65PB2F6 | H24 |
| IO66NB2F6 | H26 |
| IO66PB2F6 | H25 |
| IO67NB2F6 | G26 |
| IO67PB2F6 | G25 |
| IO68NB2F6 | K25 |

| FG896 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO68PB2F6 | K24 |
| IO69NB2F6 | F27 |
| IO69PB2F6 | E27 |
| IO70NB2F6 | J26 |
| IO70PB2F6 | J25 |
| IO71NB2F6 | H27 |
| IO71PB2F6 | G27 |
| IO72NB2F6 | J28 |
| IO72PB2F6 | H28 |
| IO73NB2F6 | G28 |
| IO73PB2F6 | F28 |
| IO74NB2F7 | L23 |
| IO74PB2F7 | L24 |
| IO75NB2F7 | L26 |
| IO75PB2F7 | K26 |
| IO76NB2F7 | M25 |
| IO76PB2F7 | L25 |
| IO77NB2F7 | K27 |
| IO77PB2F7 | J27 |
| IO78NB2F7 | M27 |
| IO78PB2F7 | L27 |
| IO79NB2F7 | K30 |
| IO79PB2F7 | K29 |
| IO80NB2F7 | M23 |
| IO80PB2F7 | M24 |
| IO81NB2F7 | M28 |
| IO81PB2F7 | L28 |
| IO82NB2F7 | N26 |
| IO82PB2F7 | M26 |
| IO83NB2F7 | N25 |
| IO83PB2F7 | N24 |
| IO84NB2F7 | N22 |
| IO84PB2F7 | N23 |
| IO85NB2F8 | M29 |
| IO85PB2F8 | L29 |

| FG896 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO86NB2F8 | N28 |
| IO86PB2F8 | N27 |
| IO87NB2F8 | P29 |
| IO87PB2F8 | P30 |
| IO88NB2F8 | P25 |
| IO88PB2F8 | P24 |
| IO89NB2F8 | P28 |
| IO89PB2F8 | P27 |
| IO90NB2F8 | P22 |
| IO90PB2F8 | P23 |
| IO91NB2F8 | R26 |
| IO91PB2F8 | P26 |
| IO92NB2F8 | R24 |
| IO92PB2F8 | R25 |
| IO93NB2F8 | R29 |
| IO93PB2F8 | R30 |
| IO94NB2F8 | R22 |
| IO94PB2F8 | R23 |
| IO95NB2F8 | T27 |
| IO95PB2F8 | R27 |
| **Bank 3** | |
| IO96NB3F9 | T29 |
| IO96PB3F9 | T30 |
| IO97NB3F9 | U29 |
| IO97PB3F9 | U30 |
| IO98NB3F9 | T22 |
| IO98PB3F9 | T23 |
| IO99NB3F9 | U26 |
| IO99PB3F9 | T26 |
| IO100NB3F9 | U24 |
| IO100PB3F9 | T24 |
| IO101NB3F9 | V28 |
| IO101PB3F9 | U28 |
| IO102NB3F9 | U23 |
| IO102PB3F9 | U22 |

## FG1152



### *Note*

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

| CQ352 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| GND | 21 |
| GND | 27 |
| GND | 33 |
| GND | 39 |
| GND | 45 |
| GND | 51 |
| GND | 57 |
| GND | 63 |
| GND | 69 |
| GND | 75 |
| GND | 81 |
| GND | 88 |
| GND | 89 |
| GND | 97 |
| GND | 103 |
| GND | 109 |
| GND | 115 |
| GND | 121 |
| GND | 133 |
| GND | 145 |
| GND | 151 |
| GND | 157 |
| GND | 163 |
| GND | 169 |
| GND | 176 |
| GND | 177 |
| GND | 186 |
| GND | 192 |
| GND | 198 |
| GND | 204 |
| GND | 210 |
| GND | 216 |
| GND | 222 |
| GND | 228 |
| GND | 234 |
| GND | 240 |
| GND | 246 |
| GND | 252 |
| GND | 258 |
| GND | 264 |
| GND | 265 |
| GND | 274 |
| GND | 280 |
| GND | 286 |
| GND | 292 |
| GND | 298 |
| GND | 310 |
| GND | 322 |
| GND | 330 |
| GND | 334 |
| GND | 340 |
| GND | 345 |
| GND/LP | 352 |
| NC | 91 |
| NC | 117 |
| NC | 130 |
| NC | 131 |
| NC | 148 |
| NC | 174 |
| NC | 268 |
| NC | 294 |
| NC | 307 |
| NC | 308 |
| NC | 327 |
| NC | 328 |
| PRA | 312 |
| PRB | 311 |
| PRC | 135 |
| PRD | 134 |
| TCK | 349 |
| TDI | 348 |
| TDO | 347 |
| TMS | 350 |
| TRST | 351 |
| VCCA | 3 |
| VCCA | 14 |
| VCCA | 32 |
| VCCA | 56 |
| VCCA | 74 |
| VCCA | 87 |
| VCCA | 102 |
| VCCA | 114 |
| VCCA | 150 |
| VCCA | 162 |
| VCCA | 175 |
| VCCA | 191 |
| VCCA | 209 |
| VCCA | 233 |
| VCCA | 251 |
| VCCA | 263 |
| VCCA | 279 |
| VCCA | 291 |
| VCCA | 329 |
| VCCA | 339 |
| VCCDA | 2 |
| VCCDA | 44 |
| VCCDA | 90 |
| VCCDA | 116 |
| VCCDA | 132 |
| VCCDA | 149 |
| VCCDA | 178 |
| VCCDA | 221 |
| VCCDA | 266 |
| VCCDA | 293 |
| VCCDA | 309 |

| CG624 | |
|---|---|
| **AX1000 Function** | **Pin Number** |
| IO63PB1F5 | G18 |
| **Bank 2** | |
| IO64NB2F6 | M17 |
| IO64PB2F6 | G22 |
| IO65NB2F6 | J21 |
| IO65PB2F6 | J20 |
| IO66NB2F6 | L23 |
| IO66PB2F6 | K20 |
| IO67NB2F6 | F23 |
| IO67PB2F6 | E23 |
| IO68NB2F6 | L18 |
| IO68PB2F6 | K18 |
| IO70NB2F6 | E24 |
| IO70PB2F6 | D24 |
| IO71NB2F6 | H23 |
| IO71PB2F6 | G23 |
| IO72NB2F6 | L19 |
| IO72PB2F6 | K19 |
| IO74NB2F7 | J22 |
| IO74PB2F7 | H22 |
| IO75NB2F7 | N23 |
| IO75PB2F7 | M23 |
| IO76NB2F7 | N17 |
| IO76PB2F7 | N16 |
| IO77NB2F7 | L22 |
| IO77PB2F7 | K22 |
| IO78NB2F7 | M19 |
| IO78PB2F7 | M18 |
| IO79NB2F7 | N19 |
| IO79PB2F7 | N18 |
| IO80NB2F7 | L21 |
| IO80PB2F7 | L20 |
| IO82NB2F7 | P18 |
| IO82PB2F7 | P17 |
| IO83NB2F7 | N22 |
| IO83PB2F7 | M22 |
| IO84NB2F7 | M20 |
| IO84PB2F7 | M21 |
| IO86NB2F8 | E25 |
| IO86PB2F8 | D25 |
| IO87NB2F8 | L24 |
| IO87PB2F8 | K24 |
| IO88NB2F8 | G24 |
| IO88PB2F8 | F24 |
| IO89NB2F8 | J25 |
| IO90NB2F8 | G25 |
| IO90PB2F8 | F25 |
| IO91NB2F8 | L25 |
| IO91PB2F8 | K25 |
| IO92NB2F8 | J24 |
| IO92PB2F8 | H24 |
| IO93PB2F8 | J23 |
| IO94NB2F8 | N24 |
| IO94PB2F8 | M24 |
| IO95NB2F8 | N25 |
| IO95PB2F8 | M25 |
| **Bank 3** | |
| IO96NB3F9 | T18 |
| IO96PB3F9 | R18 |
| IO97NB3F9 | N20 |
| IO97PB3F9 | P24 |
| IO98NB3F9 | P20 |
| IO98PB3F9 | P19 |
| IO99NB3F9 | P21 |
| IO100NB3F9 | T22 |
| IO100PB3F9 | W24 |
| IO101NB3F9 | R22 |
| IO101PB3F9 | P22 |
| IO102NB3F9 | U19 |
| IO102PB3F9 | T19 |
| IO104NB3F9 | V20 |
| IO104PB3F9 | U20 |
| IO105NB3F9 | R23 |
| IO105PB3F9 | P23 |
| IO106NB3F9 | R19 |
| IO106PB3F9 | R20 |
| IO107NB3F10 | AB24 |
| IO108NB3F10 | R25 |
| IO108PB3F10 | P25 |
| IO109NB3F10 | U25 |
| IO109PB3F10 | T25 |
| IO110NB3F10 | U24 |
| IO110PB3F10 | U23 |
| IO112NB3F10 | T24 |
| IO112PB3F10 | R24 |
| IO113NB3F10 | Y25 |
| IO113PB3F10 | W25 |
| IO114NB3F10 | V23 |
| IO114PB3F10 | V24 |
| IO116NB3F10 | AA24 |
| IO116PB3F10 | Y24 |
| IO117NB3F10 | AB25 |
| IO117PB3F10 | AA25 |
| IO118NB3F11 | T20 |
| IO118PB3F11 | R21 |
| IO120NB3F11 | W22 |
| IO120PB3F11 | W23 |
| IO122NB3F11 | V22 |
| IO122PB3F11 | U22 |
| IO124NB3F11 | Y23 |
| IO124PB3F11 | AA23 |
| IO126NB3F11 | V21 |
| IO126PB3F11 | U21 |
| IO128NB3F11 | Y22 |
| IO128PB3F11 | Y21 |
| **Bank 4** | |
| IO129NB4F12 | W20 |
| IO129PB4F12 | Y20 |

| CG624 | |
|---|---|
| **AX2000 Function** | **Pin Number** |
| GND | M11 |
| GND | M12 |
| GND | M13 |
| GND | M14 |
| GND | M15 |
| GND | N11 |
| GND | N12 |
| GND | N13 |
| GND | N14 |
| GND | N15 |
| GND | P11 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | P15 |
| GND | R11 |
| GND | R12 |
| GND | R13 |
| GND | R14 |
| GND | R15 |
| GND | T21 |
| GND | T23 |
| GND | T3 |
| GND | T5 |
| GND | V1 |
| GND | V25 |
| GND | V5 |
| PRA | F13 |
| PRB | A13 |
| PRC | AB12 |
| PRD | AE13 |
| TCK | F5 |

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

| CG624 | |
|---|---|
| **AX2000 Function** | **Pin Number** |
| TDI | C5 |
| TDO | F6 |
| TMS | D6 |
| TRST | E6 |
| VCCA | AB20 |
| VCCA | F22 |
| VCCA | F4 |
| VCCA | J17 |
| VCCA | J9 |
| VCCA | K10 |
| VCCA | K11 |
| VCCA | K15 |
| VCCA | K16 |
| VCCA | L10 |
| VCCA | L16 |
| VCCA | R10 |
| VCCA | R16 |
| VCCA | T10 |
| VCCA | T11 |
| VCCA | T15 |
| VCCA | T16 |
| VCCA | U17 |
| VCCA | U9 |
| VCCA | Y4 |
| VCCDA | A12 |
| VCCDA | A14 |
| VCCDA | AA13 |
| VCCDA | AA15 |
| VCCDA | AA20 |
| VCCDA | AA7 |
| VCCDA | AB13 |
| VCCDA | AC11 |

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

| CG624 | |
|---|---|
| **AX2000 Function** | **Pin Number** |
| VCCDA | AD11 |
| VCCDA | AD4 |
| VCCDA | AE12 |
| VCCDA | AE17 |
| VCCDA | B15 |
| VCCDA | C15 |
| VCCDA | C6 |
| VCCDA | D13 |
| VCCDA | E13 |
| VCCDA | E19 |
| VCCDA | F21 |
| VCCDA | G10 |
| VCCDA | G5 |
| VCCDA | N21 |
| VCCDA | N5 |
| VCCDA | W21 |
| VCCIB0 | A3 |
| VCCIB0 | B3 |
| VCCIB0 | C4 |
| VCCIB0 | D5 |
| VCCIB0 | J10 |
| VCCIB0 | J11 |
| VCCIB0 | K12 |
| VCCIB1 | A23 |
| VCCIB1 | B23 |
| VCCIB1 | C22 |
| VCCIB1 | D21 |
| VCCIB1 | J15 |
| VCCIB1 | J16 |
| VCCIB1 | K14 |
| VCCIB2 | C24 |
| VCCIB2 | C25 |

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*