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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	115
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax250-1pq208i

Thermal Characteristics

Introduction

The temperature variable in Microsemi's Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature. EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_a$$

EQ 1

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P$$

EQ 2

Where:

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located under Table 2-6 on page 2-7.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} values are provided for reference. The absolute maximum junction temperature is 125°C.

The maximum power dissipation allowed for commercial- and industrial-grade devices is a function of θ_{ja} . A sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{125^\circ\text{C} - 70^\circ\text{C}}{13.6^\circ\text{C/W}} = 4.04 \text{ W}$$

Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 k Ω). These are weak transistors with the gates tied on, so the on resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors; they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8 mA, 12 mA, 16 mA, or 24 mA – that can be specified in Designer.⁵

Table 2-14 • Bank-Wide Delay Values

Bits Setting	Delay (ns)	Bits Setting	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

5. These values are minimum drive strengths.

Voltage-Referenced I/O Standards

GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It requires a differential amplifier input buffer and an Open Drain output buffer. The VCCI pin should be connected to 2.5 V or 3.3 V. Note that 2.5 V GTL+ is not supported across the full military temperature range.

Table 2-37 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
N/A	VREF – 0.1	VREF + 0.1	N/A	0.6	NA	NA	NA

AC Loadings

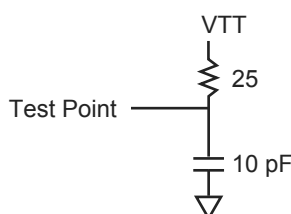


Figure 2-19 • AC Test Loads

Table 2-38 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 0.2	VREF + 0.2	VREF	1.0	10

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-39 • 2.5 V GTL+ I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_j = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V GTL+ I/O Module Timing								
t _{DP}	Input Buffer		1.71		1.95		2.29	ns
t _{PY}	Output Buffer		1.13		1.29		1.52	ns
t _{ICKLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-83 • South PLL Connections

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).

Embedded Memory

The AX architecture provides extensive, high-speed memory resources to the user. Each 4,608 bit block of RAM contains its own embedded FIFO controller, allowing the user to configure each block as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate in synchronous mode for both read and write operations. However, the read and write clocks are completely independent, and each may operate up to and above 500 MHz.

No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The AX memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in Figure 2-57.

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

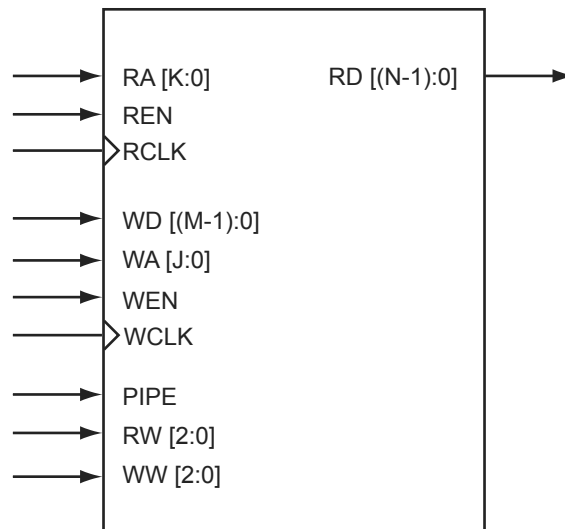


Figure 2-57 • Axcelerator Memory Module

FG324		FG324		FG324	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
GND	R4	NC	N4	VCCA	M8
GND	T16	NC	N5	VCCA	M9
GND	T3	NC	R12	VCCA	P4
GND	U17	NC	R13	VCCA	R15
GND	U2	NC	R6	VCCPLA	D8
GND	V1	NC	R7	VCCPLB	E7
GND	V18	NC	T12	VCCPLC	B11
GND/LP	E5	NC	T6	VCCPLD	E11
NC	A10	NC	U16	VCCPLE	R11
NC	A11	NC	V17	VCCPLF	P12
NC	A12	PRA	E9	VCCPLG	U8
NC	A13	PRB	D9	VCCPLH	P8
NC	A8	PRC	P10	VCCDA	B3
NC	A9	PRD	R10	VCCDA	D14
NC	B12	TCK	E6	VCCDA	E10
NC	F15	TDI	D7	VCCDA	J2
NC	F4	TDO	D5	VCCDA	K16
NC	G15	TMS	D4	VCCDA	P15
NC	G4	TRST	D6	VCCDA	P9
NC	H14	VCCA	E15	VCCDA	R5
NC	H15	VCCA	G10	VCCIB0	F7
NC	H5	VCCA	G11	VCCIB0	F8
NC	J1	VCCA	G5	VCCIB0	F9
NC	J14	VCCA	G8	VCCIB1	F10
NC	J15	VCCA	G9	VCCIB1	F11
NC	J5	VCCA	H12	VCCIB1	F12
NC	K14	VCCA	H7	VCCIB2	G13
NC	K15	VCCA	J12	VCCIB2	H13
NC	K5	VCCA	J7	VCCIB2	J13
NC	L14	VCCA	K12	VCCIB3	K13
NC	L15	VCCA	K7	VCCIB3	L13
NC	L5	VCCA	L12	VCCIB3	M13
NC	M4	VCCA	L7	VCCIB4	N10
NC	M5	VCCA	M10	VCCIB4	N11
NC	N17	VCCA	M11	VCCIB4	N12

FG484		FG484		FG484	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO54PB2F5	H22	IO72PB3F6	P20	IO90NB4F8	Y17
IO55NB2F5	L17	IO73PB3F6	R19	IO90PB4F8	Y18
IO55PB2F5	K17	IO74NB3F7	V21	IO91NB4F8	V15
IO56NB2F5	K21	IO74PB3F7	U21	IO91PB4F8	V16
IO56PB2F5	K22	IO75NB3F7	V22	IO92PB4F8	AB17
IO58NB2F5	L20	IO75PB3F7	U22	IO93NB4F8	Y15
IO58PB2F5	K20	IO76NB3F7	U20	IO93PB4F8	Y16
IO59NB2F5	L18	IO76PB3F7	T20	IO94NB4F9	AA16
IO59PB2F5	K18	IO77NB3F7	R17	IO94PB4F9	AA17
IO60NB2F5	M21	IO77PB3F7	P17	IO95NB4F9	AB14
IO60PB2F5	L21	IO78NB3F7	W21	IO95PB4F9	AB15
IO61NB2F5	L16	IO78PB3F7	W22	IO96NB4F9	W15
IO61PB2F5	K16	IO79NB3F7	T18	IO96PB4F9	W16
IO62NB2F5	M19	IO79PB3F7	R18	IO97NB4F9	AA13
IO62PB2F5	L19	IO80NB3F7	W20	IO97PB4F9	AB13
Bank 3		IO80PB3F7	V20	IO98NB4F9	AA14
IO63NB3F6	N16	IO81NB3F7	U19	IO98PB4F9	AA15
IO63PB3F6	M16	IO81PB3F7	T19	IO100NB4F9	Y14
IO64NB3F6	P22	IO82NB3F7	U18	IO100PB4F9	W14
IO64PB3F6	N22	IO82PB3F7	V19	IO101NB4F9	Y12
IO65NB3F6	N20	IO83NB3F7	R16	IO101PB4F9	Y13
IO65PB3F6	M20	IO83PB3F7	P16	IO102NB4F9	AA11
IO66NB3F6	P21	Bank 4		IO102PB4F9	AA12
IO66PB3F6	N21	IO84NB4F8	AB18	IO103NB4F9/CLKEN	V12
IO67NB3F6	N18	IO84PB4F8	AB19	IO103PB4F9/CLKEP	V13
IO67PB3F6	N19	IO85NB4F8	T15	IO104NB4F9/CLKFN	W11
IO68NB3F6	T22	IO85PB4F8	T16	IO104PB4F9/CLKFP	W12
IO68PB3F6	R22	IO86NB4F8	AA18	Bank 5	
IO69NB3F6	N17	IO86PB4F8	AA19	IO105NB5F10/CLKGN	U10
IO69PB3F6	M17	IO87NB4F8	W17	IO105PB5F10/CLKGP	U11
IO70NB3F6	T21	IO87PB4F8	V17	IO106NB5F10/CLKHN	V9
IO70PB3F6	R21	IO88NB4F8	Y19	IO106PB5F10/CLKHP	V10
IO71NB3F6	P18	IO88PB4F8	W18	IO107NB5F10	Y10
IO71PB3F6	P19	IO89NB4F8	U14	IO107PB5F10	Y11
IO72NB3F6	R20	IO89PB4F8	U15	IO108NB5F10	AA9

FG484	
AX500 Function	Pin Number
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
Bank 6	
IO126NB6F12	V2
IO126PB6F12	W2

FG484	
AX500 Function	Pin Number
IO127NB6F12	P7
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7

FG484	
AX500 Function	Pin Number
IO146NB6F13	M3
IO146PB6F13	N3
Bank 7	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3

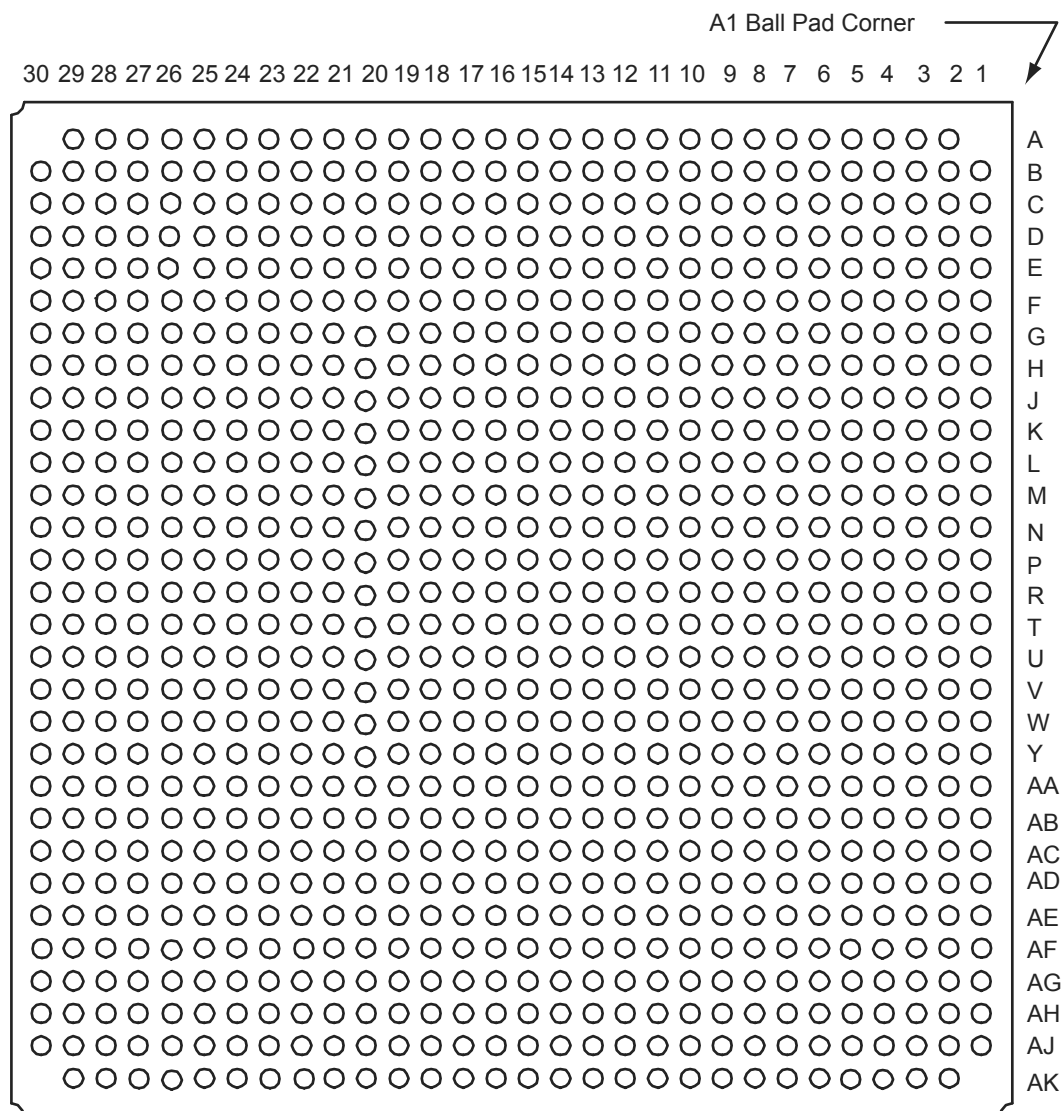
FG484	
AX500 Function	Pin Number
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	Pin Number
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	Pin Number
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO153PB7F14	M6	GND	A8	GND	L11
IO154NB7F14	K2	GND	AC23	GND	L12
IO154PB7F14	L2	GND	AC4	GND	L13
IO155NB7F14	K3	GND	AD24	GND	L14
IO155PB7F14	L3	GND	AD3	GND	L15
IO156NB7F14	L5	GND	AE2	GND	L16
IO156PB7F14	L4	GND	AE25	GND	L17
IO157NB7F14	L6	GND	AF1	GND	M10
IO157PB7F14	L7	GND	AF13	GND	M11
IO158NB7F15	J1	GND	AF14	GND	M12
IO158PB7F15	K1	GND	AF19	GND	M13
IO159NB7F15	J4	GND	AF26	GND	M14
IO159PB7F15	K4	GND	AF8	GND	M15
IO160NB7F15	H2	GND	B2	GND	M16
IO160PB7F15	J2	GND	B25	GND	M17
IO161NB7F15	K6	GND	B26	GND	N1
IO161PB7F15	K5	GND	C24	GND	N10
IO162NB7F15	H3	GND	C3	GND	N11
IO162PB7F15	J3	GND	G20	GND	N12
IO163NB7F15	G2	GND	G7	GND	N13
IO163PB7F15	G1	GND	H1	GND	N14
IO164NB7F15	G4	GND	H19	GND	N15
IO164PB7F15	H4	GND	H26	GND	N16
IO165NB7F15	F3	GND	H8	GND	N17
IO165PB7F15	G3	GND	J18	GND	N26
IO166NB7F15	E2	GND	J9	GND	P1
IO166PB7F15	F2	GND	K10	GND	P10
IO167NB7F15	F5	GND	K11	GND	P11
IO167PB7F15	G5	GND	K12	GND	P12
Dedicated I/O		GND	K13	GND	P13
GND	A1	GND	K14	GND	P14
GND	A13	GND	K15	GND	P15
GND	A14	GND	K16	GND	P16
GND	A19	GND	K17	GND	P17
GND	A26	GND	L10	GND	P26

FG896



Note

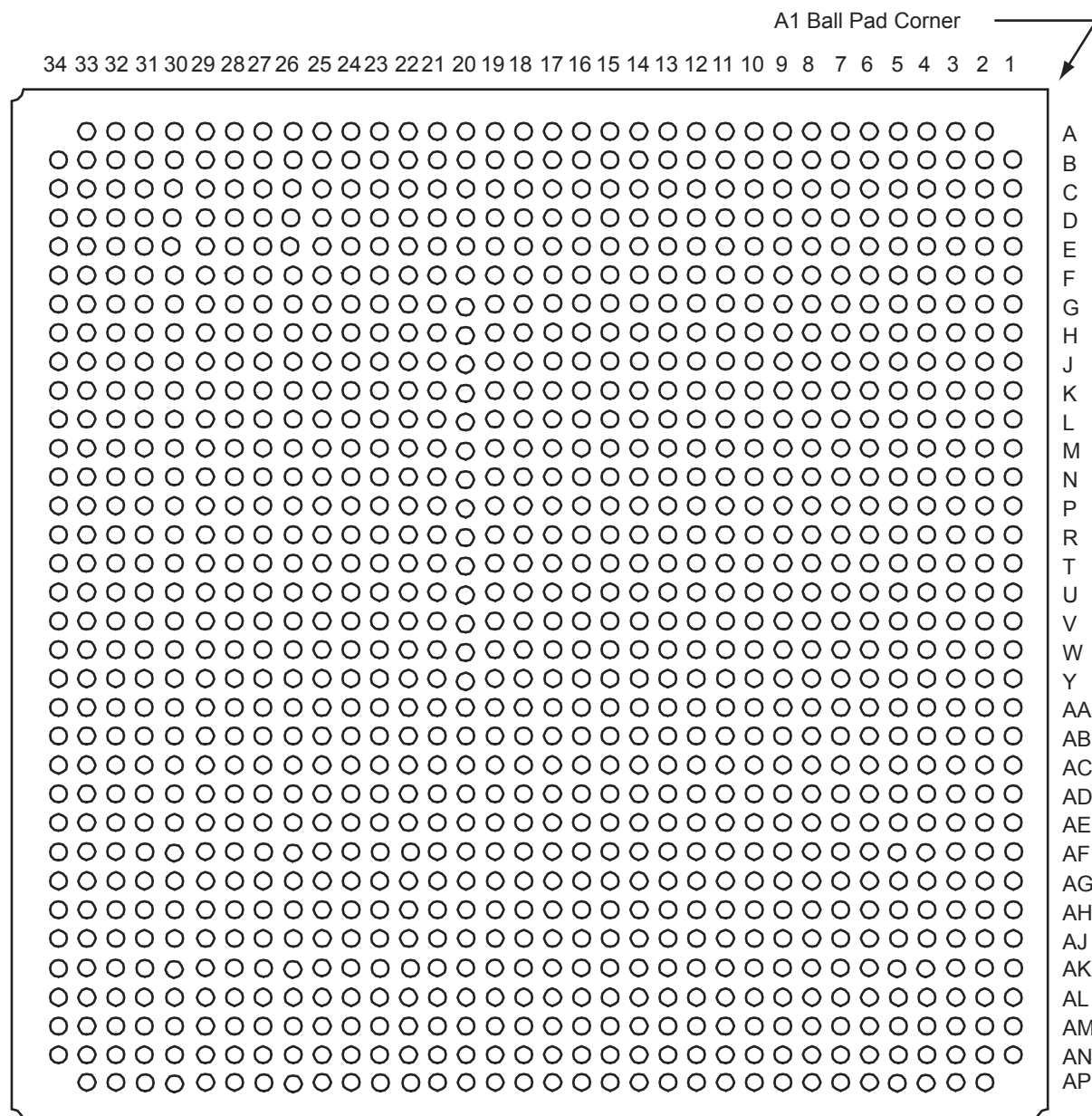
For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG896		FG896		FG896	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
NC	K1	VCCA	N20	VCCDA	AF19
NC	K2	VCCA	P11	VCCDA	C13
NC	L30	VCCA	P20	VCCDA	C5
NC	M30	VCCA	R11	VCCDA	D13
NC	N29	VCCA	R20	VCCDA	D19
NC	T1	VCCA	T11	VCCDA	D3
NC	U1	VCCA	T20	VCCDA	E18
NC	W30	VCCA	U11	VCCDA	F26
NC	Y1	VCCA	U20	VCCDA	G16
NC	Y2	VCCA	V11	VCCDA	T25
NC	Y30	VCCA	V20	VCCDA	T4
PRA	G15	VCCA	W11	VCCIB0	A3
PRB	D16	VCCA	W20	VCCIB0	B3
PRC	AB16	VCCA	Y12	VCCIB0	J10
PRD	AF16	VCCA	Y13	VCCIB0	J11
TCK	G7	VCCA	Y14	VCCIB0	J12
TDI	D5	VCCA	Y15	VCCIB0	K11
TDO	J8	VCCA	Y16	VCCIB0	K12
TMS	F6	VCCA	Y17	VCCIB0	K13
TRST	C4	VCCA	Y18	VCCIB0	K14
VCCA	AD6	VCCA	Y19	VCCIB0	K15
VCCA	AH26	VCCPLA	G14	VCCIB1	A28
VCCA	E28	VCCPLB	H15	VCCIB1	B28
VCCA	E3	VCCPLC	G17	VCCIB1	J19
VCCA	L12	VCCPLD	J16	VCCIB1	J20
VCCA	L13	VCCPLE	AH17	VCCIB1	J21
VCCA	L14	VCCPLF	AC16	VCCIB1	K16
VCCA	L15	VCCPLG	AH14	VCCIB1	K17
VCCA	L16	VCCPLH	AD15	VCCIB1	K18
VCCA	L17	VCCDA	AD24	VCCIB1	K19
VCCA	L18	VCCDA	AD7	VCCIB1	K20
VCCA	L19	VCCDA	AF12	VCCIB2	C29
VCCA	M11	VCCDA	AF13	VCCIB2	C30
VCCA	M20	VCCDA	AF15	VCCIB2	K22
VCCA	N11	VCCDA	AF18	VCCIB2	L21

FG896	
AX2000 Function	Pin Number
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	Pin Number
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152

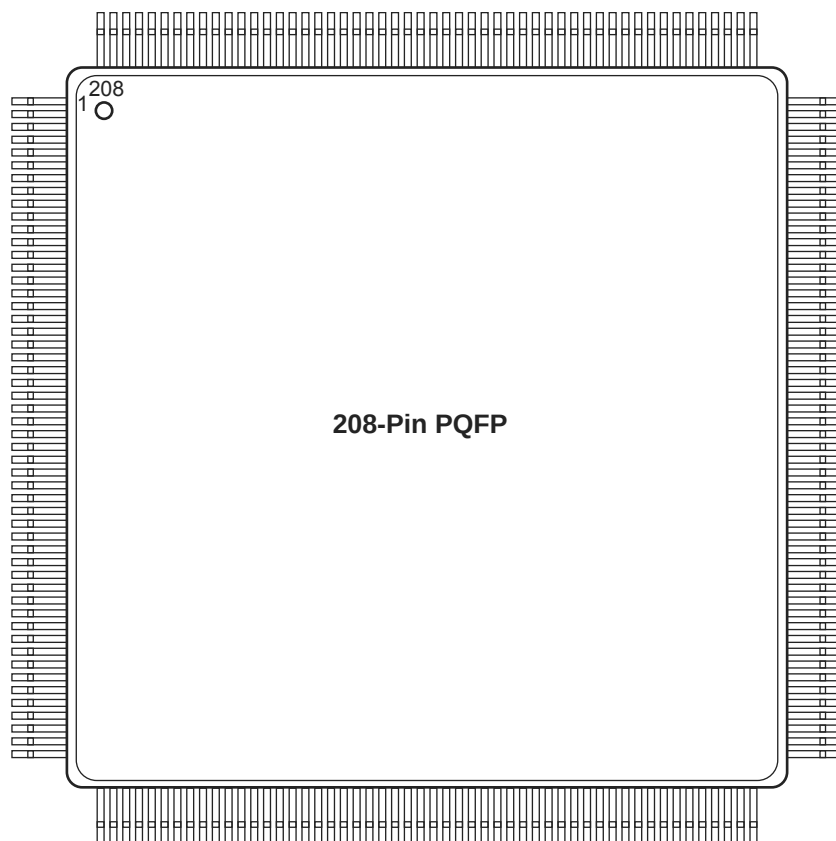


Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO103PB2F9	M28	IO121NB2F11	T27	IO138NB3F12	Y29
IO104NB2F9	M34	IO121PB2F11	T26	IO138PB3F12	W29
IO104PB2F9	L34	IO122NB2F11	T30	IO139NB3F13	Y27
IO105NB2F9	P27	IO122PB2F11	T29	IO139PB3F13	W27
IO105PB2F9	N27	IO123NB2F11	U28	IO140NB3F13	AA33
IO106NB2F9	M32	IO123PB2F11	T28	IO140PB3F13	Y33
IO106PB2F9	M31	IO124NB2F11	T31	IO141NB3F13	Y25
IO107NB2F10	P25	IO124PB2F11	T32	IO141PB3F13	Y24
IO107PB2F10	P26	IO125NB2F11	U24	IO142NB3F13	AA31
IO108NB2F10	N33	IO125PB2F11	U25	IO142PB3F13	Y31
IO108PB2F10	M33	IO126NB2F11	U33	IO143NB3F13	AA28
IO109NB2F10	P29	IO126PB2F11	U34	IO143PB3F13	Y28
IO109PB2F10	N29	IO127NB2F11	U26	IO144NB3F13	AA34
IO110NB2F10	P30	IO127PB2F11	U27	IO144PB3F13	Y34
IO110PB2F10	N30	IO128NB2F11	U31	IO145NB3F13	AA26
IO111NB2F10	R24	IO128PB2F11	U32	IO145PB3F13	Y26
IO111PB2F10	R25	Bank 3		IO146NB3F13	AA29
IO112NB2F10	P31	IO129NB3F12	V29	IO146PB3F13	AA30
IO112PB2F10	N31	IO129PB3F12	U29	IO147NB3F13	AB30
IO113NB2F10	R28	IO130NB3F12	V31	IO147PB3F13	AB29
IO113PB2F10	P28	IO130PB3F12	V32	IO148NB3F13	AB32
IO114NB2F10	P32	IO131NB3F12	V24	IO148PB3F13	AA32
IO114PB2F10	N32	IO131PB3F12	V25	IO149NB3F13	AB27
IO115NB2F10	R30	IO132NB3F12	W28	IO149PB3F13	AA27
IO115PB2F10	R29	IO132PB3F12	V28	IO150NB3F14	AC31
IO116NB2F10	P34	IO133NB3F12	W26	IO150PB3F14	AB31
IO116PB2F10	P33	IO133PB3F12	V26	IO151NB3F14	AD33
IO117NB2F10	R27	IO134NB3F12	W33	IO151PB3F14	AC33
IO117PB2F10	R26	IO134PB3F12	V33	IO152NB3F14	AC28
IO118NB2F11	R34	IO135NB3F12	W25	IO152PB3F14	AB28
IO118PB2F11	R33	IO135PB3F12	W24	IO153NB3F14	AB25
IO119NB2F11	T24	IO136NB3F12	W31	IO153PB3F14	AA25
IO119PB2F11	T25	IO136PB3F12	W32	IO154NB3F14	AD32
IO120NB2F11	T33	IO137NB3F12	Y30	IO154PB3F14	AC32
IO120PB2F11	T34	IO137PB3F12	W30	IO155NB3F14	AD29

PQ208



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
Bank 0		IO35NB1F3	275	Bank 3	
IO00PB0F0	343	IO35PB1F3	276	IO63NB3F6	217
IO03NB0F0	341	IO37NB1F3	271	IO63PB3F6	218
IO03PB0F0	342	IO37PB1F3	272	IO64NB3F6	219
IO05NB0F0	337	IO41NB1F3	269	IO64PB3F6	220
IO05PB0F0	338	IO41PB1F3	270	IO65NB3F6	213
IO07NB0F0	335	Bank 2		IO65PB3F6	214
IO07PB0F0	336	IO43NB2F4	261	IO67NB3F6	207
IO09NB0F0	331	IO43PB2F4	262	IO67PB3F6	208
IO09PB0F0	332	IO45NB2F4	259	IO68NB3F6	211
IO15NB0F1	325	IO45PB2F4	260	IO68PB3F6	212
IO15PB0F1	326	IO47NB2F4	255	IO69NB3F6	205
IO17NB0F1	323	IO47PB2F4	256	IO69PB3F6	206
IO17PB0F1	324	IO49NB2F4	253	IO71NB3F6	201
IO19NB0F1/HCLKAN	319	IO49PB2F4	254	IO71PB3F6	202
IO19PB0F1/HCLKAP	320	IO50NB2F4	247	IO73NB3F6	199
IO20NB0F1/HCLKBN	313	IO50PB2F4	248	IO73PB3F6	200
IO20PB0F1/HCLKBP	314	IO51NB2F4	249	IO75NB3F7	193
Bank 1		IO51PB2F4	250	IO75PB3F7	194
IO21NB1F2/HCLKCN	305	IO53NB2F5	243	IO76NB3F7	195
IO21PB1F2/HCLKCP	306	IO53PB2F5	244	IO76PB3F7	196
IO22NB1F2/HCLKDN	299	IO54NB2F5	241	IO77NB3F7	189
IO22PB1F2/HCLKDP	300	IO54PB2F5	242	IO77PB3F7	190
IO23NB1F2	289	IO55NB2F5	237	IO79NB3F7	187
IO23PB1F2	290	IO55PB2F5	238	IO79PB3F7	188
IO24NB1F2	295	IO57NB2F5	235	IO80NB3F7	183
IO24PB1F2	296	IO57PB2F5	236	IO80PB3F7	184
IO25NB1F2	287	IO58NB2F5	231	IO81NB3F7	181
IO25PB1F2	288	IO58PB2F5	232	IO81PB3F7	182
IO27NB1F2	283	IO59NB2F5	229	IO83NB3F7	179
IO27PB1F2	284	IO59PB2F5	230	IO83PB3F7	180
IO29NB1F2	281	IO61NB2F5	225	Bank 4	
IO29PB1F2	282	IO61PB2F5	226	IO85NB4F8	172
IO31NB1F2	277	IO62NB2F5	223	IO85PB4F8	173
IO31PB1F2	278	IO62PB2F5	224	IO87NB4F8	170

CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO131PB4F12	171	IO187PB5F17	99	IO224NB6F20	46
IO132NB4F12	166	IO188NB5F17	100	IO224PB6F20	47
IO132PB4F12	167	IO188PB5F17	101	Bank 7	
IO133NB4F12	164	IO190NB5F17	94	IO225NB7F21	40
IO133PB4F12	165	IO190PB5F17	95	IO225PB7F21	41
IO134NB4F12	160	IO192NB5F17	92	IO226NB7F21	42
IO134PB4F12	161	IO192PB5F17	93	IO226PB7F21	43
IO136NB4F12	158	Bank 6		IO237NB7F22	34
IO136PB4F12	159	IO193PB6F18	86	IO237PB7F22	35
IO137NB4F12	154	IO194NB6F18	84	IO238NB7F22	36
IO137PB4F12	155	IO194PB6F18	85	IO238PB7F22	37
IO138NB4F12	152	IO196NB6F18	78	IO240NB7F22	30
IO138PB4F12	153	IO196PB6F18	79	IO240PB7F22	31
IO153NB4F14	146	IO197NB6F18	82	IO241NB7F22	28
IO153PB4F14	147	IO197PB6F18	83	IO241PB7F22	29
IO159NB4F14/CLKEN	142	IO198NB6F18	76	IO242NB7F22	24
IO159PB4F14/CLKEP	143	IO198PB6F18	77	IO242PB7F22	25
IO160NB4F14/CLKFN	136	IO203NB6F19	72	IO244NB7F22	22
IO160PB4F14/CLKFP	137	IO203PB6F19	73	IO244PB7F22	23
Bank 5		IO204NB6F19	70	IO245NB7F22	18
IO161NB5F15/CLKGN	128	IO204PB6F19	71	IO245PB7F22	19
IO161PB5F15/CLKGP	129	IO205NB6F19	66	IO246NB7F22	16
IO162NB5F15/CLKHN	122	IO205PB6F19	67	IO246PB7F22	17
IO162PB5F15/CLKHP	123	IO206NB6F19	64	IO249NB7F23	12
IO167NB5F15	118	IO206PB6F19	65	IO249PB7F23	13
IO167PB5F15	119	IO207NB6F19	60	IO250NB7F23	10
IO183NB5F17	110	IO207PB6F19	61	IO250PB7F23	11
IO183PB5F17	111	IO208NB6F19	58	IO256NB7F23	4
IO184NB5F17	112	IO208PB6F19	59	IO256PB7F23	5
IO184PB5F17	113	IO211NB6F19	54	IO257NB7F23	6
IO185NB5F17	104	IO211PB6F19	55	IO257PB7F23	7
IO185PB5F17	105	IO212NB6F19	52	Dedicated I/O	
IO186NB5F17	106	IO212PB6F19	53	GND	1
IO186PB5F17	107	IO223NB6F20	48	GND	9
IO187NB5F17	98	IO223PB6F20	49	GND	15

Revision	Changes	Page
Revision 12 (v2.4)	Revised ordering information and timing data to reflect phase out of –3 speed grade options.	
	Table 2-3 was updated.	2
Revision 11 (v2.3)	The "Packaging Data" section is new.	iv
	Table 2-2 was updated.	2-1
	"VCCDA Supply Voltage" was updated.	2-9
	"PRA/B/C/D Probe A, B, C and D" was updated.	2-10
	The "User I/Os" was updated.	2-11
Revision 10 (v2.2)	Figure 1-3 was updated.	1-2
	Table 2-2 was updated.	2-1
	The "Power-Up/Down Sequence" section was updated.	2-1
	Table 2-4 was updated.	2-3
	Table 2-5 was updated.	2-4
	The "Timing Characteristics" section was added.	2-7
	Table 2-7 was updated.	2-7
	Figure 2-1 was updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) equations in the "Hardwired Clock – Using LVTTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) in the "Routed Clock – Using LVTTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The "Global Pins" section was updated.	2-10
	The "User I/Os" section was updated.	2-11
	Table 2-17 was updated.	2-19
	Figure 2-8 was updated.	2-20
	Figure 2-13 and Figure 2-14 were updated.	2-24
	The following timing parameters were renamed in I/O timing characteristic tables from Table 2-22 to Table 2-60: $t_{IOCLKQ} > t_{CLKQ}$ $t_{IOCLKY} > t_{OCLKQ}$	2-26 to 2-52
	Timing numbers were updated from Table 2-22 to Table 2-78.	2-26 to 2-69
	The "R-Cell" section was updated.	2-58
	Figure 2-59 was updated.	2-89
	Figure 2-60 was updated.	2-89
	Figure 2-67 was updated.	2-100
	Figure 2-68 was updated.	2-101
	Table 2-89 to Table 2-93 were updated.	2-90 to 2-94
	Table 2-98 to Table 2-102 were updated.	2-102 to 2-106

Revision	Changes	Page
Revision 8 (continued)	The following changes were made in the "FG676"(AX500) section: AE2, AE25 Change from NC to GND. AF2, AF25 Changed from GND to NC AB4, AF24, C1, C26 Changed from V_{CCDA} to V_{CCA} AD15 Change from V_{CCDA} to V_{COMPLE} AD17 Changed from V_{COMPLE} to V_{CCDA}	3-37
	In the "FG896" (AX2000) section, the AK28 changed from VCCIB5 to VCCIB4.	3-52
	The "CQ352" and "CG624" sections are new.	3-98, 3-115
Revision 7 (Advance v1.6)	All I/O FIFO capability was removed.	n/a
	Table 1 was updated.	i
	Figure 1-9 was updated.	1-7
	Figure 2-5 was updated.	2-16
	The "Using an I/O Register" section was updated.	2-16
	The AX250 and AX1000 descriptions were added to the "FG484" section.	3-21
Revision 6 (Advance v1.5)	Table 2-3 was updated.	2-2
	Figure 2-1 was updated.	2-8
	Figure 2-48 was updated.	2-75
	Figure 2-52 was updated.	2-82
Revision 5 (Advance v1.4)	In the "PQ208" table, pin 196 was missing, but it has been added in this version with a function of GND.	3-84
	The following pins in the "FG484" table for AX500 were changed: Pin G7 is GND/LP Pins AB8, C10, C11, C14, AB16 are NC.	3-21
	The "FG676" table was updated.	3-37
Revision 4 (Advance v1.3)	The "Device Resources" section was updated for the CS180.	ii
	The "Programmable Interconnect Element" and Figure 1-2 are new.	1-1 and 1-2
	The "CS180" table is new.	3-1
	The "PQ208" tables for the AX500 were updated. The following pins were not defined in the previous version: GND 21 IO106PB5F10/CLKHP 71 GND 136	3-84
Revision 3 (Advance v1.2)	Table 1, "Ordering Information", "Device Resources", and the Product Plan table were updated.	i, ii
	The following figures and tables were updated:	
	Figure 1-3	1-2
	Figure 1-8 (new)	1-6
	Table 2-3	2-2
	Figure 2-2	2-9
	Table 2-8	2-12
	Figure 2-11	2-23
	The "Design Environment" section was updated.	1-7
	The "Package Thermal Characteristics" was updated.	2-6