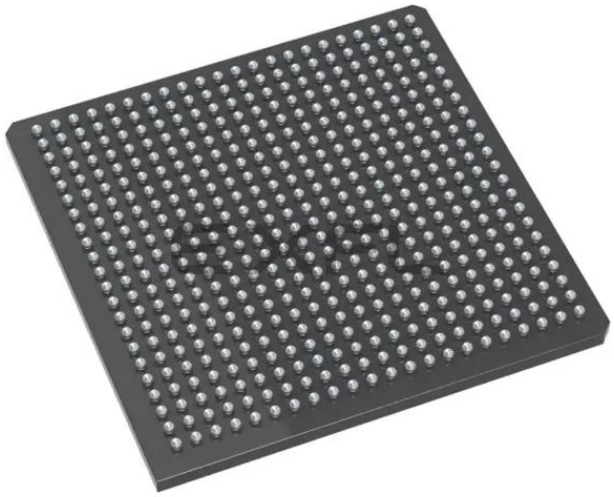

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	248
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-2fg484

Figure 1-2 • Axcelerator Family Interconnect Elements

Logic Modules

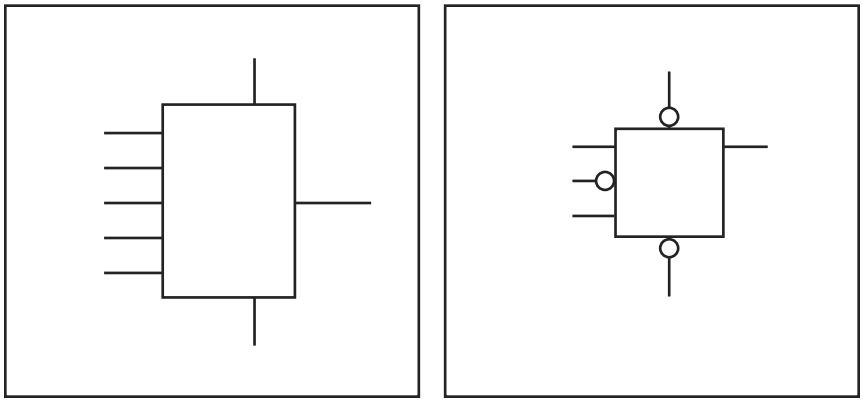

Figure 1-3 • AX C-Cell and R-Cell

Special PLL Macros

Table 2-84 shows the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

***Table 2-84* • PLL Special Macros**

Macro Name	Usage
PLLINT	Connects RefCLK to a regular routed net or a pad.
PLLRCLK	Connects CLK1 or CLK2 to the CLK network.
PLLHCLK	Connects CLK1 or CLK2 to the HCLK network.
PLLOUT	Connects CLK1 or CLK2 to a regular routed net.

***Table 2-85* • Electrical Specifications**

Parameter	Value	Notes
Frequency Ranges		
Reference Frequency (min.)	14 MHz	Lowest input frequency
Reference Frequency (max.)	200 MHz	Highest input frequency
OSC Frequency (min.)	20 MHz	Lowest output frequency
OSC Frequency (max.)	1 GHz	Highest output frequency
Jitter		
Long-Term Jitter (max.)	1%	Percentage of period, low reference clock frequencies
Long-Term Jitter (max.)	100ps	High reference clock frequencies
Short-Term Jitter (max.)	50ps+1%	Percentage of output frequency
Acquisition Time (lock) from Cold Start		
Acquisition Time (max.)*	400 cycles	Period of low reference clock frequencies
Acquisition Time (max.)*	1.5 µs	High reference clock frequencies
Power Consumption		
Analog Supply Current (low freq.)	200 µA	Current at minimum oscillator frequency
Analog Supply Current (high freq.)	200 µA	Frequency-dependent current
Digital Supply Current (low freq.)	0.5 µA/MHz	Current at maximum oscillator frequency, unloaded
Digital Supply Current (high freq.)	1 µA/MHz	Frequency-dependent current
Duty Cycle		
Minimum Output Duty Cycle	45%	
Maximum Output Duty Cycle	55%	

*Note: *The lock bit remains Low until RefCLK reaches the minimum input frequency.*

CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number