Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	138
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-2fgg256

The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).

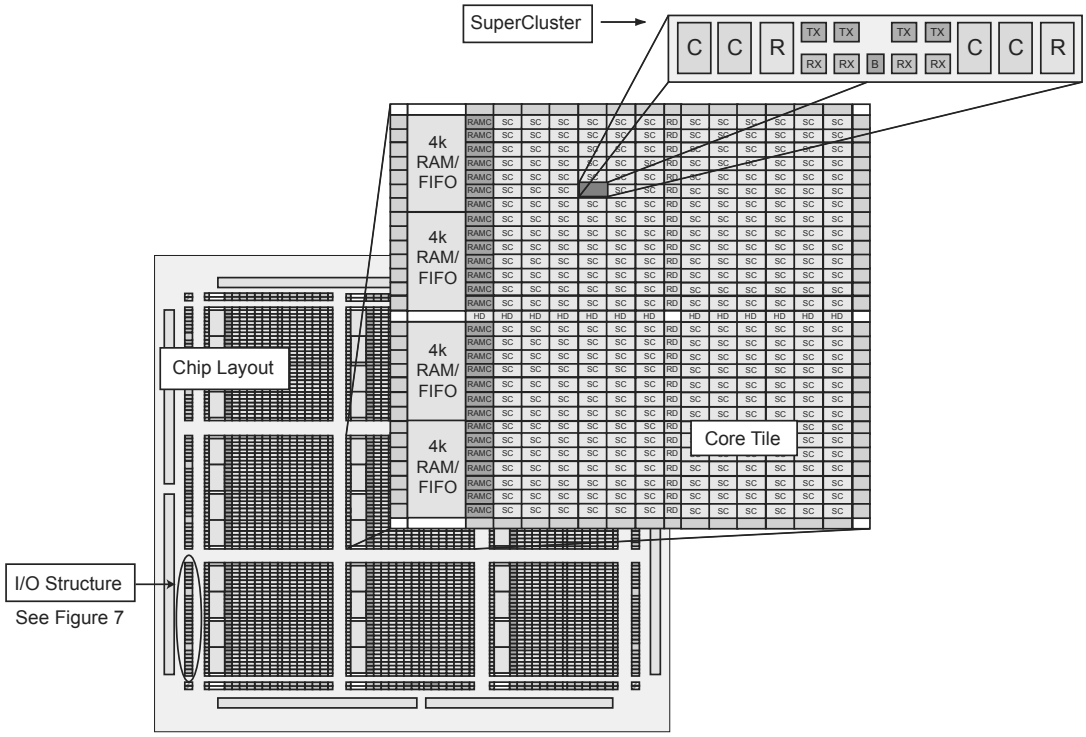


Figure 1-6 • **AX Device Architecture (AX1000 shown)**

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

The maximum power dissipation allowed for Military temperature and Mil-Std 883B devices is specified as a function of θ_{jc}.

Table 2-6 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0m/s	θ_{ja} 2.5m/s	Units
Chip Scale Package (CSP)	180	N/A	57.8	51.0	50	°C/W
Plastic Quad Flat Pack (PQFP)	208	8.0	26	23.5	20.9	°C/W
Plastic Ball Grid Array (PBGA)	729	2.2	13.7	10.6	9.6	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.0	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	324	3.0	25.8	22.1	20.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	208	2.0	22	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA)[2]	624	6.5	8.9	8.5	8	°C/W

Notes:

1. *θ_{jc} for the 208-pin and 352-pin CQFP refers to the thermal resistance between the junction and the bottom of the package.*
2. *θ_{jc} for the 624-pin CCGA refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board (θ_{jb}) for CCGA 624 package is 3.4°C/W.*

Timing Characteristics

Axcelerator devices are manufactured in a CMOS process, therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-7 should be applied to all timing data contained within this datasheet.

Table 2-7 • **Temperature and Voltage Timing Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, VCCA = 1.425V)**

	Junction Temperature						
VCCA	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
1.4 V	0.83	0.86	0.91	0.96	1.02	1.05	1.15
1.425 V	0.82	0.84	0.90	0.94	1.00	1.04	1.13
1.5 V	0.78	0.80	0.85	0.89	0.95	0.98	1.07
1.575 V	0.74	0.76	0.81	0.85	0.90	0.94	1.02
1.6 V	0.73	0.75	0.80	0.84	0.89	0.92	1.01

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 175°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4V and 1.6V.*

All timing numbers listed in this datasheet represent sample timing characteristics of Axcelerator devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Microsemi's Designer software after place-and-route.

Table 2-8 • **I/O Standards Supported by the Axcelerator Family**

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVCMOS 2.5 V	2.5	N/A	N/A
LVCMOS 1.8 V	1.8	N/A	N/A
LVCMOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

*Note: *2.5 V GTL+ is not supported across the full military temperature range.*

Table 2-9 • **Supply Voltages**

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5 V	1.5 V	3.3 V	1.5 V
1.5 V	1.8 V	3.3 V	1.8 V
1.5 V	2.5 V	3.3 V	2.5 V
1.5 V	3.3 V	3.3 V	3.3 V

Table 2-10 • **I/O Features Comparison**

I/O Assignment	Clamp Diode	Hot Insertion	5 V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes[1]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	Yes	No	Yes[1, 2]	Enabled/Disabled	
LVCMOS 2.5 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled[3]
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled[4]

Notes:

1. *Can be implemented with an IDT bus switch.*
2. *Can be implemented with an external resistor.*
3. *The OE input of the output buffer must be deasserted permanently (handled by software).*
4. *The OE input of the output buffer must be asserted permanently (handled by software).*

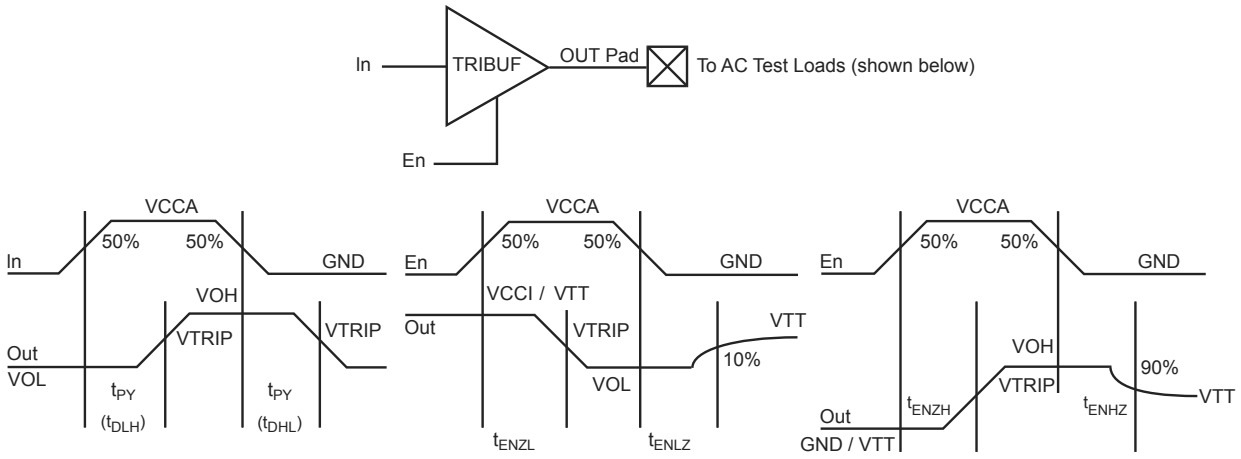


Figure 2-10 • **Output Buffer Delays**

***Table 2-36* • 3.3 V PCI-X I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V PCI-X Output Module Timing								
t_{DP}	Input Buffer		1.57		1.79		2.10	ns
t_{PY}	Output Buffer		2.10		2.40		2.82	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.59		1.60		1.61	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.65		3.02		3.55	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.11		3.55		4.17	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t_{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t_{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t_{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t_{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t_{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t_{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t_{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t_{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t_{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

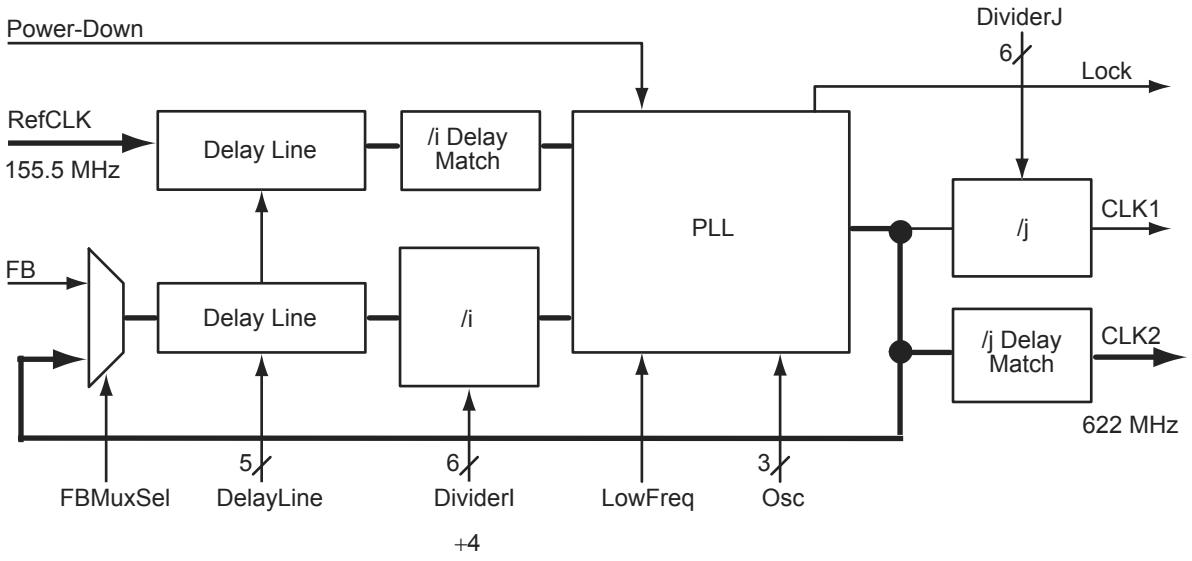


Figure 2-53 • **Using the PLL 155.5 MHz In, 622 MHz Out**

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

Note that the RAM blocks employ little-endian byte order for read and write operations.

***Table 2-88* • RAM Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

***Table 2-91* • Four RAM Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	2.51		2.51		2.51		ns
t_{WCKP}	WCLK Minimum Period	3.26		3.26		3.26		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		3.08		3.51		4.13	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		3.08		3.51		4.13	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		2.83		3.23		3.79	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	2.96		2.96		2.96		ns
t_{RCKP}	RCLK Minimum Period	3.69		3.69		3.69		ns

Note: Timing data for these four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

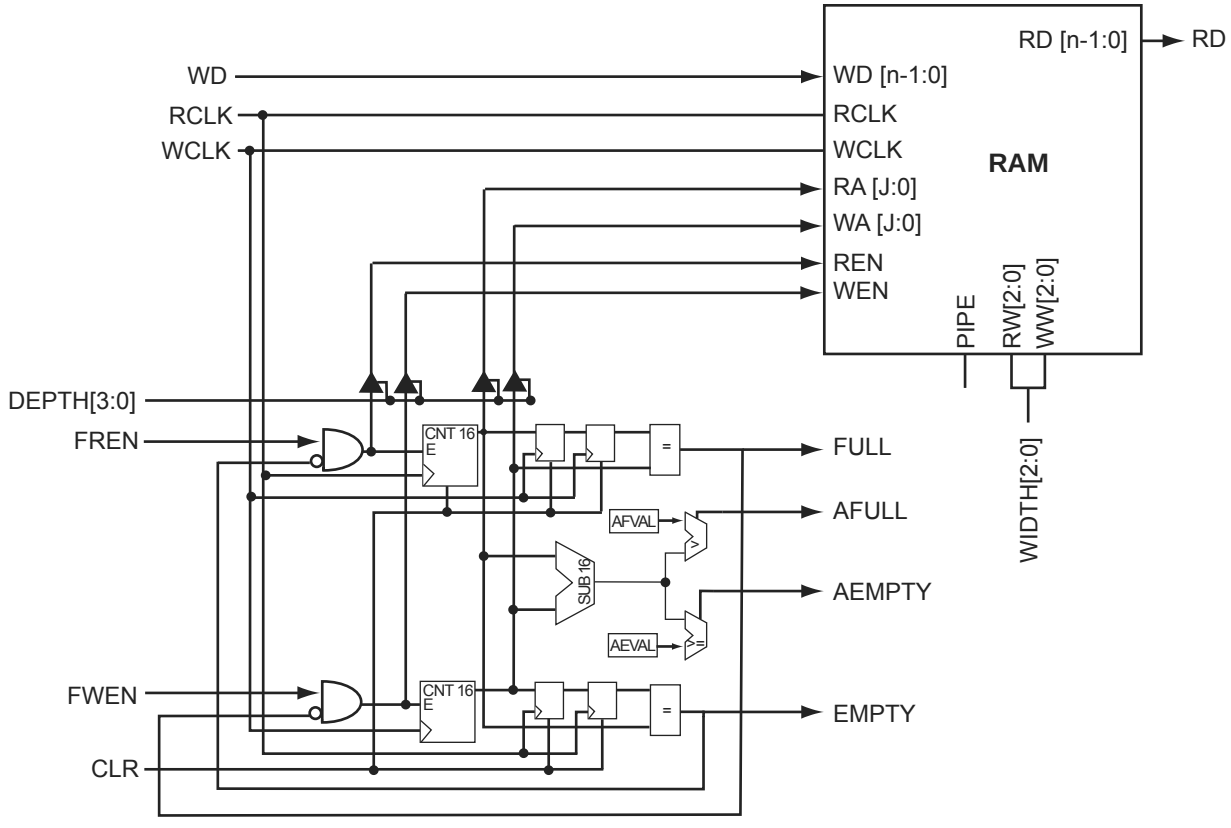


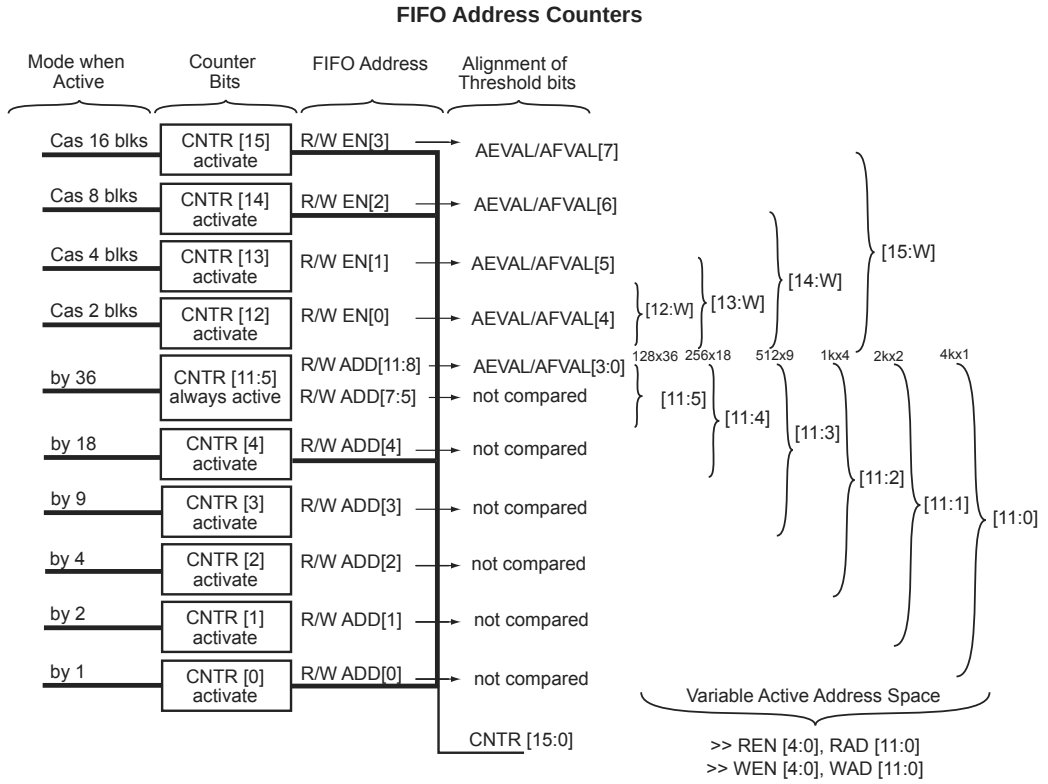
Figure 2-61 • **Axcelerator RAM with Embedded FIFO Controller**

FIFO Flag Logic

The FIFO is user configurable into various DEPTHs and WIDTHs. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.



Note: Inactive counter bits are set to zero.

Figure 2-62 • **FIFO Address Counters**

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

Table 2-94 • **FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

BG729	
AX1000 Function	Pin Number
IO218PB6F20	V2
IO219NB6F20	T1
IO219PB6F20	U1
IO220NB6F20	R5
IO220PB6F20	R6
IO221NB6F20	T3
IO221PB6F20	T4
IO222NB6F20	R2
IO222PB6F20	T2
IO223NB6F20	P8
IO223PB6F20	P9
IO224NB6F20	R3
IO224PB6F20	R4
Bank 7	
IO225NB7F21	P1
IO225PB7F21	R1
IO226NB7F21	P3
IO226PB7F21	P2
IO227NB7F21	N7
IO227PB7F21	P7
IO228NB7F21	P5
IO228PB7F21	P4
IO229NB7F21	N2
IO229PB7F21	N1
IO230NB7F21	N6
IO230PB7F21	P6
IO231NB7F21	N9
IO231PB7F21	N8
IO232NB7F21	N4
IO232PB7F21	N3
IO233NB7F21	M2
IO233PB7F21	M1
IO234NB7F21	M4
IO234PB7F21	M3
IO235NB7F21	M5
IO235PB7F21	N5
IO236NB7F22	L2

BG729	
AX1000 Function	Pin Number
IO236PB7F22	L1
IO237NB7F22	L4
IO237PB7F22	L3
IO238NB7F22	L6
IO238PB7F22	M6
IO239NB7F22	M8
IO239PB7F22	M7
IO240NB7F22	K2
IO240PB7F22	K1
IO241NB7F22	K4
IO241PB7F22	K3
IO242NB7F22	K5
IO242PB7F22	L5
IO243NB7F22	J2
IO243PB7F22	J1
IO244NB7F22	J4
IO244PB7F22	J3
IO245NB7F22	H2
IO245PB7F22	H1
IO246NB7F22	H4
IO246PB7F22	H3
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	J6
IO248PB7F23	K6
IO249NB7F23	H5
IO249PB7F23	J5
IO250NB7F23	G2
IO250PB7F23	G1
IO251NB7F23	K8
IO251PB7F23	K7
IO252NB7F23	G4
IO252PB7F23	G3
IO253NB7F23	F2
IO253PB7F23	F1
IO254NB7F23	G6
IO254PB7F23	H6

BG729	
AX1000 Function	Pin Number
IO255NB7F23	F5
IO255PB7F23	G5
IO256NB7F23	F3
IO256PB7F23	F4
IO257NB7F23	H7
IO257PB7F23	J7
Dedicated I/O	
GND	A1
GND	A2
GND	A25
GND	A26
GND	A27
GND	A3
GND	AC24
GND	AE1
GND	AE2
GND	AE25
GND	AE26
GND	AE27
GND	AE3
GND	AE5
GND	AF1
GND	AF2
GND	AF25
GND	AF26
GND	AF27
GND	AF3
GND	AG1
GND	AG2
GND	AG25
GND	AG26
GND	AG27
GND	AG3
GND	B1
GND	B2
GND	B25
GND	B26

FG256-Pin FBGA	
AX125 Function	**Pin Number**
VCCA	L10
VCCA	L7
VCCA	L8
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A2
VCCDA	C13
VCCDA	D9
V_{CCDA}	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10

FG256-Pin FBGA	
AX125 Function	**Pin Number**
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

FG676	
AX500 Function	Pin Number
IO102PB4F9	AB15
IO103NB4F9/CLKEN	AE16
IO103PB4F9/CLKEP	AF16
IO104NB4F9/CLKFN	AE14
IO104PB4F9/CLKFP	AE15
Bank 5	
IO105NB5F10/CLKGN	AE12
IO105PB5F10/CLKGP	AE13
IO106NB5F10/CLKHN	AE11
IO106PB5F10/CLKHP	AF11
IO107NB5F10	Y12
IO107PB5F10	AA13
IO108NB5F10	AC12
IO108PB5F10	AB12
IO109NB5F10	AC10
IO109PB5F10	AC11
IO110NB5F10	AF9
IO110PB5F10	AF10
IO111NB5F10	Y11
IO111PB5F10	AA12
IO112NB5F10	AE9
IO112PB5F10	AE10
IO113NB5F10	AC9
IO113PB5F10	AD9
IO114NB5F11	AF6
IO114PB5F11	AF7
IO115NB5F11	AA10
IO115PB5F11	AB10
IO116NB5F11	AE7
IO116PB5F11	AE8
IO117NB5F11	AD7
IO117PB5F11	AD8
IO118NB5F11	AC7
IO118PB5F11	AC8
IO119NB5F11	AD6

FG676	
AX500 Function	Pin Number
IO119PB5F11	AE6
IO120NB5F11	AE5
IO120PB5F11	AF5
IO121NB5F11	AF4
IO121PB5F11	AE4
IO122NB5F11	AC5
IO122PB5F11	AC6
IO123NB5F11	AD4
IO123PB5F11	AD5
IO124NB5F11	AB6
IO124PB5F11	AB7
IO125NB5F11	AE3
IO125PB5F11	AF3
Bank 6	
IO126NB6F12	AB3
IO126PB6F12	AC3
IO127NB6F12	AA2
IO127PB6F12	AB2
IO128NB6F12	AC2
IO128PB6F12	AD2
IO129NB6F12	Y1
IO129PB6F12	AA1
IO130NB6F12	Y3
IO130PB6F12	AA3
IO131NB6F12	U6
IO131PB6F12	V6
IO132NB6F12	W2
IO132PB6F12	Y2
IO133NB6F12	V4
IO133PB6F12	W4
IO134NB6F12	V3
IO134PB6F12	W3
IO135NB6F12	V1
IO135PB6F12	V2
IO136NB6F13	U4

FG676	
AX500 Function	Pin Number
IO136PB6F13	U5
IO137NB6F13	T6
IO137PB6F13	T7
IO138NB6F13	T5
IO138PB6F13	T4
IO139NB6F13	R6
IO139PB6F13	R7
IO140NB6F13	T3
IO140PB6F13	U3
IO141NB6F13	U1
IO141PB6F13	U2
IO142NB6F13	R2
IO142PB6F13	T2
IO143NB6F13	P3
IO143PB6F13	R3
IO144NB6F13	P5
IO144PB6F13	P4
IO145NB6F13	P6
IO145PB6F13	P7
IO146NB6F13	R1
IO146PB6F13	T1
Bank 7	
IO147NB7F14	N6
IO147PB7F14	N7
IO148NB7F14	N5
IO148PB7F14	N4
IO149NB7F14	N2
IO149PB7F14	N3
IO150NB7F14	L1
IO150PB7F14	M1
IO151NB7F14	M2
IO151PB7F14	M3
IO152NB7F14	M5
IO152PB7F14	M4
IO153NB7F14	M7

FG676	
AX1000 Function	**Pin Number**
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11

FG676	
AX1000 Function	**Pin Number**
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11

FG676	
AX1000 Function	**Pin Number**
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25

FG896	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	D6
IO00PB0F0	E6
IO01NB0F0	A5
IO01PB0F0	B5
IO02NB0F0	G9
IO02PB0F0	G8
IO03NB0F0	F8
IO03PB0F0	F7
IO04NB0F0	D7
IO04PB0F0	E7
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	H9
IO06PB0F0	H8
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	E9
IO08PB0F0	F9
IO09NB0F0	A7
IO09PB0F0	B7
IO10NB0F0	H10
IO10PB0F0	G10
IO11NB0F0	C9
IO11PB0F0	C8
IO12NB0F1	E10
IO12PB0F1	F10
IO13NB0F1	D10
IO13PB0F1	D9
IO14NB0F1	F11
IO14PB0F1	G11
IO15NB0F1	A10
IO15PB0F1	A9
IO16NB0F1	H12
IO16PB0F1	H11

FG896	
AX1000 Function	Pin Number
IO17NB0F1	B11
IO17PB0F1	B10
IO18NB0F1	D11
IO18PB0F1	E11
IO19NB0F1	C12
IO19PB0F1	C11
IO20NB0F1	F12
IO20PB0F1	G12
IO21NB0F1	D12
IO21PB0F1	E12
IO22NB0F2	H13
IO22PB0F2	J13
IO23NB0F2	A12
IO23PB0F2	A11
IO24NB0F2	F13
IO24PB0F2	G13
IO25NB0F2	B13
IO25PB0F2	B12
IO26NB0F2	E14
IO26PB0F2	E13
IO27NB0F2	B14
IO27PB0F2	A14
IO28NB0F2	H14
IO28PB0F2	J14
IO29NB0F2	B15
IO29PB0F2	A15
IO30NB0F2/HCLKAN	C14
IO30PB0F2/HCLKAP	D14
IO31NB0F2/HCLKBN	E15
IO31PB0F2/HCLKBP	D15
Bank 1	
IO32NB1F3/HCLKCN	E17
IO32PB1F3/HCLKCP	E16
IO33NB1F3/HCLKDN	C17
IO33PB1F3/HCLKDP	D17

FG896	
AX1000 Function	Pin Number
IO34NB1F3	A17
IO34PB1F3	B17
IO35NB1F3	D18
IO35PB1F3	C18
IO36NB1F3	H17
IO36PB1F3	J17
IO37NB1F3	B19
IO37PB1F3	A19
IO38NB1F3	H18
IO38PB1F3	J18
IO39NB1F3	B20
IO39PB1F3	A20
IO40NB1F3	C20
IO40PB1F3	C19
IO41NB1F4	E20
IO41PB1F4	E19
IO42NB1F4	F18
IO42PB1F4	G18
IO43NB1F4	A22
IO43PB1F4	A21
IO44NB1F4	F20
IO44PB1F4	F19
IO45NB1F4	D21
IO45PB1F4	D20
IO46NB1F4	D22
IO46PB1F4	C22
IO47NB1F4	A25
IO47PB1F4	A24
IO48NB1F4	H19
IO48PB1F4	G19
IO49NB1F4	C24
IO49PB1F4	C23
IO50NB1F4	G20
IO50PB1F4	H20
IO51NB1F4	F21

CG624	
AX2000 Function	**Pin Number**
Bank 0	
IO00NB0F0	D7*
IO00PB0F0	E7*
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9*
IO13PB0F1	D8*
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11*
IO26PB0F2	B8*

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

Revision	Changes	Page
Revision 10 (continued)	The "TRST" section was updated.	2-107
	The "Global Set Fuse" section was added.	2-109
	A footnote was added to "FG896" for the AX2000 regarding pins AB1, AE2, G1, and K2.	3-52
	Pinouts for the AX250, AX500, and AX1000 were added for "CQ352".	3-98
	Pinout for the AX1000 was added for "CG624".	3-115
Revision 9 (v2.1)	Table 2-79 was updated.	2-69
	The "Low Power Mode" section was updated.	2-106
Revision 8 (v2.0)	Table 1 has been updated.	i
	The "Ordering Information" section has been updated.	ii
	The "Device Resources" section has been updated.	ii
	The "Temperature Grade Offerings" section is new.	iii
	The "Speed Grade and Temperature Grade Matrix" section has been updated.	iii
	Table 2-9 has been updated.	2-12
	Table 2-10 has been updated.	2-12
	Table 2-1 has been updated.	2-1
	Table 2-2 has been updated.	2-1
	Table 2-3 has been updated.	2-2
	Table 2-4 has been updated.	2-3
	Table 2-5 has been updated.	2-4
	The "Power Estimation Example" section has been updated.	2-5
	The "Thermal Characteristics" section has been updated.	2-6
	The "Package Thermal Characteristics" section has been updated.	2-6
	The "Timing Characteristics" section has been updated.	2-7
	The "Pin Descriptions" section has been updated.	2-9
	Timing numbers have been updated from the "3.3 V LVTTL" section to the "Timing Characteristics" section. Many AC Loads were updated as well.	2-25 to 2-59
	Timing characteristics for the "Hardwired Clocks" and "Routed Clocks" sections were updated.	2-66, 2-68
	Table 2-89 to Table 2-92 and Table 2-98 to Table 2-99 were updated.	2-90 to 2-93, 2-102 to 2-103
	The following sections were updated: "Low Power Mode", "Interface", "Data Registers (DRs)", "Security", "Silicon Explorer II Probe Interface", and "Programming"	2-106 to 2-110
	In the "PQ208" (AX500) section, pins 2, 52, and 156 changed from V_{CCDA} to V_{CCA}. For pins 170 and 171, the I/O names refer to pair 23 instead of 24.	3-84

Microsemi

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

5172160-18/3.12