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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	115
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	208-BFCQFP with Tie Bar
Supplier Device Package	208-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-cq208m

User-Defined Supply Pins

VREF Supply Voltage

Reference voltage for I/O banks. VREF pins are configured by the user from regular I/O pins; VREF pins are not in fixed locations. There can be one or more VREF pins in an I/O bank.

Global Pins

HCLKA/B/C/D Dedicated (Hardwired) Clocks A, B, C and D

These pins are the clock inputs for sequential modules or north PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When the HCLK pins are unused, it is recommended that they are tied to ground.

CLKE/F/G/H Routed Clocks E, F, G, and H

These pins are clock inputs for clock distribution networks or south PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. The clock input is buffered prior to clocking the R-cells. When the CLK pins are unused, Microsemi recommends that they are tied to ground.

JTAG/Probe Pins

PRA/B/C/D Probe A, B, C and D

The Probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins' probe capabilities can be permanently disabled to protect programmed design confidentiality. The probe pins are of LVTTTL output levels.

TCK Test Clock

Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

TDI Test Data Input

Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal 10 k Ω pull-up resistor.

TDO Test Data Output

Serial output for JTAG boundary-scan testing.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, TRST). TMS is equipped with an internal 10 k Ω pull-up resistor.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a 10 k Ω pull-up resistor.

Special Functions

LP Low Power Pin

The LP pin controls the low power mode of Axcelerator devices. The device is placed in the low power mode by connecting the LP pin to logic high. To exit the low power mode, the LP pin must be set Low. Additionally, the LP pin must be set Low during chip powering-up or chip powering-down operations. See "Low Power Mode" on page 2-106 for more details.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

SSTL2

Stub Series Terminated Logic for 2.5 V is a general-purpose 2.5 V memory bus standard (JESD8-9). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-44 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF - 0.2	VREF + 0.2	3.6	VREF - 0.57	VREF + 0.57	7.6	-7.6

AC Loadings

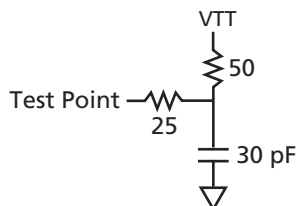


Figure 2-21 • AC Test Loads

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF - 0.75	VREF + 0.75	VREF	1.25	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-46 • 2.5 V SSTL2 Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		-2 Speed		-1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V SSTL2 Class I I/O Module Timing								
t _{DP}	Input Buffer		1.83		2.08		2.45	ns
t _{PY}	Output Buffer		2.39		2.72		3.20	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Module Specifications

C-Cell

Introduction

The C-cell is one of the two logic module types in the AX architecture. It is the combinatorial logic resource in the Axcelerator device. The AX architecture implements a new combinatorial cell that is an extension of the C-cell implemented in the SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The C-cell features the following (Figure 2-27):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns.
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns.

This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with Microsemi's extensive macro library (please see the *Antifuse Macro Library Guide* for a complete listing of available Axcelerator macros).

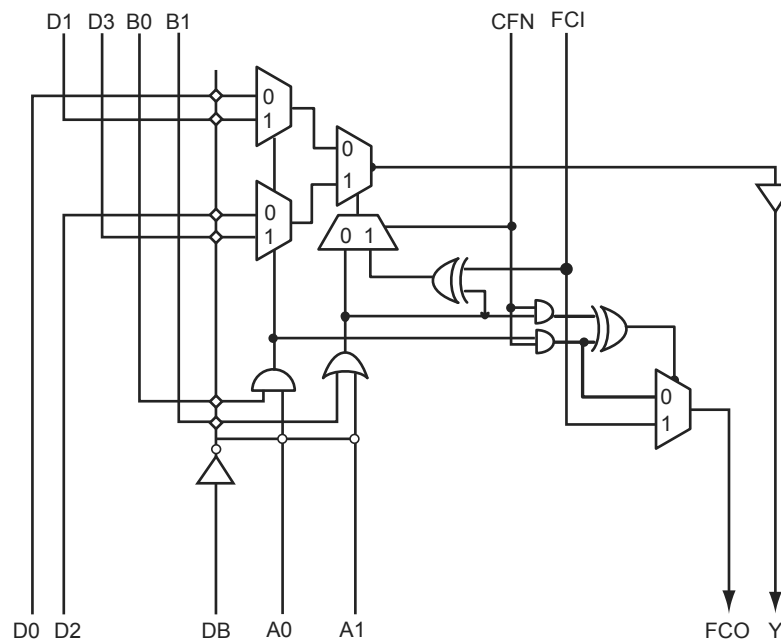


Figure 2-27 • C-Cell

Table 2-67 • AX500 Predicted Routing Delays
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $T_J = 70^\circ\text{C}$

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-68 • AX1000 Predicted Routing Delays
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $T_J = 70^\circ\text{C}$

		-2 Speed	-1 Speed	Std Speed	
Parameter	Description	Typical	Typical	Typical	Units
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.45	0.51	0.60	ns
t_{RD2}	Routing delay for FO2	0.53	0.60	0.71	ns
t_{RD3}	Routing delay for FO3	0.56	0.63	0.74	ns
t_{RD4}	Routing delay for FO4	0.63	0.71	0.84	ns
t_{RD5}	Routing delay for FO5	0.73	0.82	0.97	ns
t_{RD6}	Routing delay for FO6	0.99	1.13	1.32	ns
t_{RD7}	Routing delay for FO7	1.02	1.15	1.36	ns
t_{RD8}	Routing delay for FO8	1.48	1.68	1.97	ns
t_{RD16}	Routing delay for FO16	2.57	2.91	3.42	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Implementation Example:

Figure 2-47 shows a complex clock distribution example. The reference clock (RefCLK) of PLLE is being sourced from non-clock signal pins (INBUF to PLLINT). The CLK1 output of PLLE is being fed to the RefCLK input of PLLF. The CLK2 output of PLLE is driving logic (via PLLOUT). In turn, this logic is driving the global resource CLKE. PLLF is driving both CLKF and CLKG global resources.

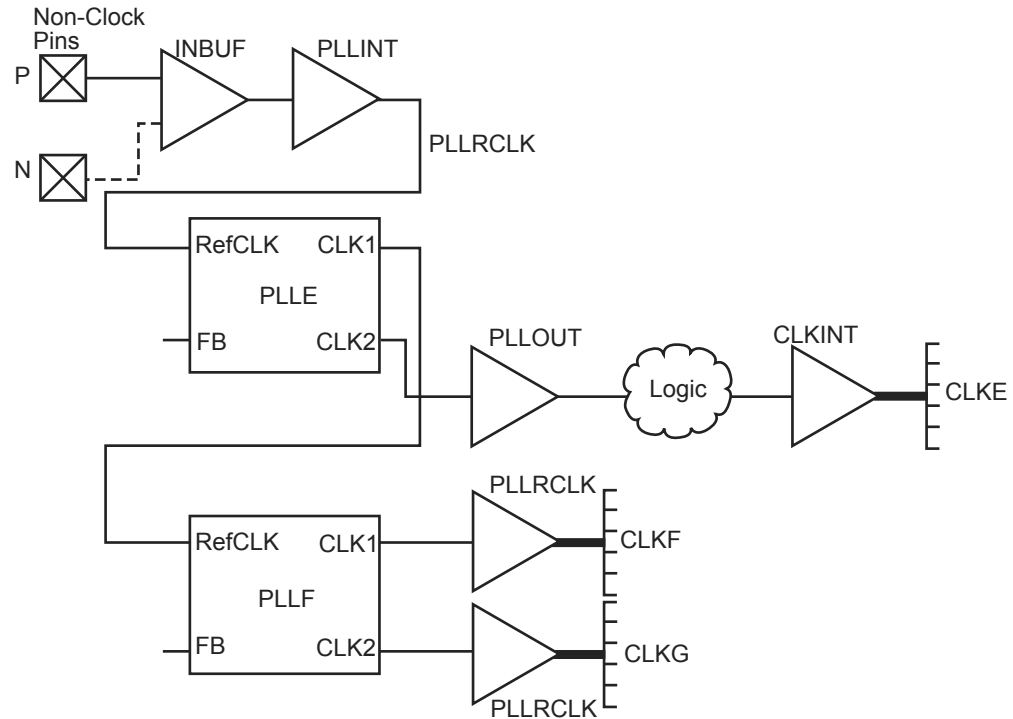


Figure 2-47 • Complex Clock Distribution Example

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

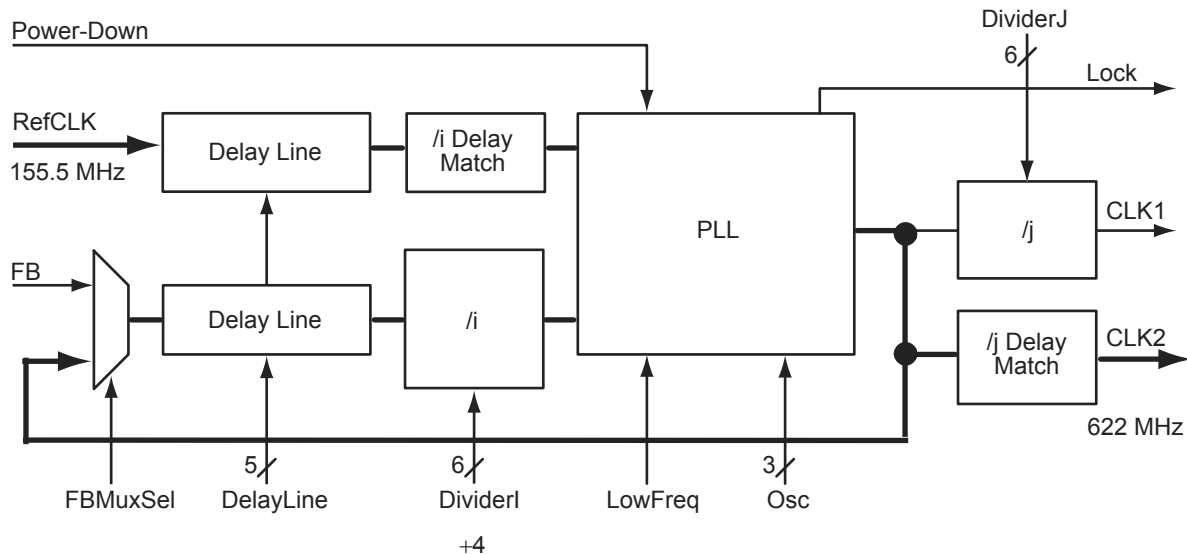


Figure 2-53 • Using the PLL 155.5 MHz In, 622 MHz Out

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

Table 2-89 • One RAM Block

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Write Mode								
t _{WDASU}	Write Data Setup vs. WCLK		1.08		1.23		1.45	ns
t _{WDAHD}	Write Data Hold vs. WCLK		0.22		0.25		0.30	ns
t _{WADSU}	Write Address Setup vs. WCLK		1.08		1.23		1.45	ns
t _{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WENSU}	Write Enable Setup vs. WCLK		1.08		1.23		1.45	ns
t _{WENHD}	Write Enable Hold vs. WCLK		0.22		0.25		0.30	ns
t _{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t _{WCLK}	WCLK Minimum Low Pulse Width	0.88		0.88		0.88		ns
t _{WCKP}	WCLK Minimum Period	1.63		1.63		1.63		ns
Read Mode								
t _{RADSU}	Read Address Setup vs. RCLK		0.81		0.92		1.08	ns
t _{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RENSU}	Read Enable Setup vs. RCLK		0.81		0.92		1.08	ns
t _{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RCK2RD1}	RCLK-to-OUT (Pipelined)		1.32		1.51		1.77	ns
t _{RCK2RD2}	RCLK-to-OUT (Non-Pipelined)		2.16		2.46		2.90	ns
t _{RCLKH}	RCLK Minimum High Pulse Width	0.77		0.77		0.77		ns
t _{RCLKL}	RCLK Minimum Low Pulse Width	0.93		0.93		0.93		ns
t _{RCKP}	RCLK Minimum Period	1.70		1.70		1.70		ns

Note: Timing data for this single block RAM has a depth of 4,096. For all other combinations, use Microsemi's timing software.

Table 2-98 • One FIFO Block

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		11.40		12.98		15.26	ns
t _{WHD}	Write Hold		0.22		0.25		0.30	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		0.88		0.88		0.88	ns
t _{WCKP}	Minimum WCLK Period	1.63		1.63		1.63		ns
t _{RSU}	Read Setup		11.63		13.25		15.58	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.77		0.77		0.77	ns
t _{RCKL}	RCLK Low		0.93		0.93		0.93	ns
t _{RCKP}	Minimum RCLK period	1.70		1.70		1.70		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		1.32		1.51		1.77	ns
t _{RCK2RD2}	RCLK-To-OUT (Non-Pipelined)		2.16		2.46		2.90	ns

Note: Timing data for this single block FIFO has a depth of 4,096. For all other combinations, use Microsemi's timing software.

Table 2-100 • Four FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		14.60		16.63		19.55	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		2.51		2.51		2.51	ns
t _{WCKP}	Minimum WCLK Period	3.26		3.26		3.26		ns
t _{RSU}	Read Setup		15.27		17.39		20.44	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		2.96		2.96		2.96	ns
t _{RCKP}	Minimum RCLK period	3.69		3.69		3.69		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		2.83		3.23		3.79	ns

Note: Timing data for these four cascaded FIFO blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0					
IO00NB0F0	E6	IO18NB0F1	C10	IO36NB1F3	H15
IO00PB0F0	F6	IO18PB0F1	C9	IO36PB1F3	G15
IO01NB0F0	G8	IO19NB0F1	E11	IO37NB1F3	C17
IO01PB0F0	G7	IO19PB0F1	F11	IO37PB1F3	C16
IO02NB0F0	D7	IO20NB0F1	G12	IO38NB1F3	B18
IO02PB0F0	E7	IO20PB0F1	H12	IO38PB1F3	B17
IO03NB0F0	D5	IO21NB0F1	D11	IO39NB1F3	A18
IO03PB0F0	E5	IO21PB0F1	D10	IO39PB1F3	A17
IO04NB0F0	G9	IO22NB0F2	A10	IO40NB1F3	H16
IO04PB0F0	H9	IO22PB0F2	A9	IO40PB1F3	G16
IO05NB0F0	E8	IO23NB0F2	B11	IO41NB1F4	B19
IO05PB0F0	F8	IO23PB0F2	B10	IO41PB1F4	A19
IO06NB0F0	C6	IO24NB0F2	G13	IO42NB1F4	C19
IO06PB0F0	D6	IO24PB0F2	H13	IO42PB1F4	C18
IO07NB0F0	B5	IO25NB0F2	C12	IO43NB1F4	D18
IO07PB0F0	C5	IO25PB0F2	C11	IO43PB1F4	D17
IO08NB0F0	A6	IO26NB0F2	E12	IO44NB1F4	H17
IO08PB0F0	A5	IO26PB0F2	D12	IO44PB1F4	G17
IO09NB0F0	E9	IO27NB0F2	E13	IO45NB1F4	F17
IO09PB0F0	F9	IO27PB0F2	F13	IO45PB1F4	E17
IO10NB0F0	G10	IO28NB0F2	G14	IO46NB1F4	B20
IO10PB0F0	H10	IO28PB0F2	H14	IO46PB1F4	A20
IO11NB0F0	B7	IO29NB0F2	A12	IO47NB1F4	C21
IO11PB0F0	B6	IO29PB0F2	B12	IO47PB1F4	C20
IO12NB0F1	C8	IO30NB0F2/HCLKAN	C13	IO48NB1F4	H18
IO12PB0F1	C7	IO30PB0F2/HCLKAP	D13	IO48PB1F4	G18
IO13NB0F1	E10	IO31NB0F2/HCLKBN	F14	IO49NB1F4	F18
IO13PB0F1	F10	IO31PB0F2/HCLKBP	E14	IO49PB1F4	E18
IO14NB0F1	G11	Bank 1		IO50NB1F4	D20
IO14PB0F1	H11	IO32NB1F3/HCLKCN	C14	IO50PB1F4	D19
IO15NB0F1	D9	IO32PB1F3/HCLKCP	B14	IO51NB1F4	A22
IO15PB0F1	D8	IO33NB1F3/HCLKDN	D16	IO51PB1F4	A21
IO16NB0F1	A8	IO33PB1F3/HCLKDP	D15	IO52NB1F4	B22
IO16PB0F1	A7	IO34NB1F3	B16	IO52PB1F4	B21
IO17NB0F1	B9	IO34PB1F3	A16	IO53NB1F4	F19
IO17PB0F1	B8	IO35NB1F3	E15	IO53PB1F4	E19
		IO35PB1F3	F15	IO54NB1F5	F20

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO163PB5F15	AA14	IO182NB5F17	AF7	IO200NB6F18	AA4
IO164NB5F15	AE13	IO182PB5F17	AG7	IO200PB6F18	AA5
IO164PB5F15	AF13	IO183NB5F17	AD7	IO201NB6F18	W5
IO165NB5F15	AF12	IO183PB5F17	AE7	IO201PB6F18	W6
IO165PB5F15	AG12	IO184NB5F17	AC7	IO202NB6F18	AB1
IO166NB5F15	AD12	IO184PB5F17	AC8	IO202PB6F18	AC1
IO166PB5F15	AE12	IO185NB5F17	AF6	IO203NB6F19	Y3
IO167NB5F15	Y13	IO185PB5F17	AG6	IO203PB6F19	AA3
IO167PB5F15	AA13	IO186NB5F17	AB7	IO204NB6F19	AA2
IO168NB5F15	AD11	IO186PB5F17	AB8	IO204PB6F19	AB2
IO168PB5F15	AE11	IO187NB5F17	Y9	IO205NB6F19	U8
IO169NB5F15	AG11	IO187PB5F17	AA9	IO205PB6F19	V8
IO169PB5F15	AF11	IO188NB5F17	AD6	IO206NB6F19	V5
IO170NB5F15	AB11	IO188PB5F17	AE6	IO206PB6F19	V6
IO170PB5F15	AC11	IO189NB5F17	AB6	IO207NB6F19	Y1
IO171NB5F16	AF10	IO189PB5F17	AC6	IO207PB6F19	AA1
IO171PB5F16	AG10	IO190NB5F17	AF5	IO208NB6F19	W4
IO172NB5F16	AD10	IO190PB5F17	AG5	IO208PB6F19	Y4
IO172PB5F16	AE10	IO191NB5F17	AA6	IO209NB6F19	T7
IO173NB5F16	Y12	IO191PB5F17	AA7	IO209PB6F19	U7
IO173PB5F16	AA12	IO192NB5F17	Y8	IO210NB6F19	W2
IO174NB5F16	AB10	IO192PB5F17	AA8	IO210PB6F19	Y2
IO174PB5F16	AC10	Bank 6		IO211NB6F19	U5
IO175NB5F16	AF9	IO193NB6F18	W8	IO211PB6F19	U6
IO175PB5F16	AG9	IO193PB6F18	Y7	IO212NB6F19	V3
IO176NB5F16	AD9	IO194NB6F18	AB5	IO212PB6F19	W3
IO176PB5F16	AE9	IO194PB6F18	AC5	IO213NB6F19	R9
IO177NB5F16	Y11	IO195NB6F18	AC2	IO213PB6F19	T8
IO177PB5F16	AA11	IO195PB6F18	AC3	IO214NB6F20	U4
IO178NB5F16	AF8	IO196NB6F18	AC4	IO214PB6F20	V4
IO178PB5F16	AG8	IO196PB6F18	AD4	IO215NB6F20	T5
IO179NB5F16	AD8	IO197NB6F18	Y5	IO215PB6F20	T6
IO179PB5F16	AE8	IO197PB6F18	Y6	IO216NB6F20	V1
IO180NB5F16	AB9	IO198NB6F18	AB3	IO216PB6F20	W1
IO180PB5F16	AC9	IO198PB6F18	AB4	IO217NB6F20	R7
IO181NB5F17	Y10	IO199NB6F18	V7	IO217PB6F20	R8
IO181PB5F17	AA10	IO199PB6F18	W7	IO218NB6F20	U2

FG256		FG256		FG256	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
Bank 0		IO32NB2F2	C16	IO61PB3F3	L14
IO01NB0F0	B4	IO32PB2F2	B16	Bank 4	
IO01PB0F0	B3	IO33NB2F2	F15	IO62NB4F4	N12
IO03NB0F0	A4	IO33PB2F2	E15	IO62PB4F4	N13
IO03PB0F0	A3	IO35NB2F2	H13	IO63NB4F4	T14
IO05NB0F0	B6	IO35PB2F2	G13	IO63PB4F4	R14
IO05PB0F0	B5	IO36NB2F2	E16	IO66PB4F4	T15
IO07NB0F0	A6	IO36PB2F2	D16	IO67NB4F4	R12
IO07PB0F0	A5	IO38NB2F2	H15	IO67PB4F4	R13
IO12NB0F0/HCLKAN	B8	IO38PB2F2	G15	IO69NB4F4	P11
IO12PB0F0/HCLKAP	B7	IO39NB2F2	H14	IO69PB4F4	P12
IO13NB0F0/HCLKBN	A9	IO39PB2F2	G14	IO70PB4F4	T11
IO13PB0F0/HCLKBP	A8	IO40NB2F2	G16	IO73NB4F4	T12
Bank 1		IO40PB2F2	F16	IO73PB4F4	T13
IO14NB1F1/HCLKCN	C10	IO43NB2F2	K15	IO74NB4F4/CLKEN	R9
IO14PB1F1/HCLKCP	C9	IO43PB2F2	K16	IO74PB4F4/CLKEP	R10
IO15NB1F1/HCLKDN	B11	IO44NB2F2	J16	IO75NB4F4/CLKFN	T8
IO15PB1F1/HCLKDP	B10	IO44PB2F2	H16	IO75PB4F4/CLKFP	T9
IO17NB1F1	A13	Bank 3		Bank 5	
IO17PB1F1	A12	IO45NB3F3	K13	IO76NB5F5/CLKGN	P7
IO19NB1F1	B13	IO45PB3F3	J13	IO76PB5F5/CLKGP	P8
IO19PB1F1	B12	IO46NB3F3	K14	IO77NB5F5/CLKHN	R6
IO21NB1F1	C12	IO46PB3F3	J14	IO77PB5F5/CLKHP	R7
IO21PB1F1	C11	IO52NB3F3	L15	IO79NB5F5	T5
IO23NB1F1	A15	IO52PB3F3	L16	IO79PB5F5	T6
IO23PB1F1	B14	IO54NB3F3	P16	IO81NB5F5	P5
IO26NB1F1	C15	IO54PB3F3	N16	IO81PB5F5	P6
IO26PB1F1	C14	IO55PB3F3	M16	IO83NB5F5	T3
IO27NB1F1	D13	IO56NB3F3	P15	IO83PB5F5	T4
IO27PB1F1	D12	IO56PB3F3	R16	IO85NB5F5	R3
Bank 2		IO58NB3F3	N15	IO85PB5F5	R4
IO29NB2F2	F13	IO58PB3F3	M15	IO88NB5F5	R1
IO29PB2F2	E13	IO59NB3F3	M13	IO88PB5F5	T2
IO30NB2F2	F14	IO59PB3F3	L13	IO89NB5F5	N4
IO30PB2F2	E14	IO61NB3F3	M14	IO89PB5F5	N5

FG256		FG256		FG256	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
Bank 6		IO117NB7F7	C2	GND	M12
IO91NB6F6	L4	IO117PB7F7	B1	GND	M5
IO91PB6F6	M4	IO118NB7F7	D2	GND	P13
IO92NB6F6	L3	IO118PB7F7	D3	GND	P3
IO92PB6F6	M3	IO119NB7F7	E3	GND	R15
IO94NB6F6	P2	IO119PB7F7	F3	GND	R2
IO94PB6F6	N2	Dedicated I/O		GND	T1
IO97NB6F6	J4	VCCDA	E4	GND	T16
IO97PB6F6	K4	GND	A1	GND/LP	D4
IO98NB6F6	N1	GND	A16	PRA	D8
IO98PB6F6	P1	GND	B15	PRB	C8
IO100NB6F6	L2	GND	B2	PRC	N9
IO100PB6F6	M2	GND	D15	PRD	P9
IO102NB6F6	L1	GND	E12	TCK	D5
IO102PB6F6	M1	GND	E5	TDI	C6
IO103NB6F6	J3	GND	F11	TDO	C4
IO103PB6F6	K3	GND	F6	TMS	C3
IO104NB6F6	J2	GND	G10	TRST	C5
IO104PB6F6	K2	GND	G7	VCCA	D14
Bank 7		GND	G8	VCCA	F10
IO107NB7F7	J1	GND	G9	VCCA	F4
IO107PB7F7	K1	GND	H10	VCCA	F7
IO108NB7F7	G2	GND	H7	VCCA	F8
IO108PB7F7	H2	GND	H8	VCCA	F9
IO111NB7F7	G3	GND	H9	VCCA	G11
IO111PB7F7	H3	GND	J10	VCCA	G6
IO112NB7F7	E1	GND	J7	VCCA	H11
IO112PB7F7	F1	GND	J8	VCCA	H6
IO113NB7F7	G1	GND	J9	VCCA	J11
IO114NB7F7	E2	GND	K10	VCCA	J6
IO114PB7F7	F2	GND	K7	VCCA	K11
IO115NB7F7	G4	GND	K8	VCCA	K6
IO115PB7F7	H4	GND	K9	VCCA	L10
IO116NB7F7	C1	GND	L11	VCCA	L7
IO116PB7F7	D1	GND	L6	VCCA	L8

FG324	
AX125 Function	Pin Number
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
NC	J5	VCCA	J10	VCCDA	AD10
NC	J6	VCCA	J11	VCCDA	AD13
NC	P22	VCCA	J12	VCCDA	AD17
NC	R20	VCCA	J13	VCCDA	B1
NC	R21	VCCA	J14	VCCDA	B17
NC	R22	VCCA	J15	VCCDA	D24
NC	R4	VCCA	J16	VCCDA	E14
NC	R5	VCCA	J17	VCCDA	P2
NC	T22	VCCA	K18	VCCDA	P23
NC	T24	VCCA	K9	VCCIB0	G10
NC	U22	VCCA	L18	VCCIB0	G8
NC	U24	VCCA	L9	VCCIB0	G9
NC	V22	VCCA	M18	VCCIB0	H10
NC	V5	VCCA	M9	VCCIB0	H11
NC	W21	VCCA	N18	VCCIB0	H12
NC	W22	VCCA	N9	VCCIB0	H13
NC	W5	VCCA	P18	VCCIB0	H9
NC	W6	VCCA	P9	VCCIB1	G17
NC	Y21	VCCA	R18	VCCIB1	G18
NC	Y4	VCCA	R9	VCCIB1	G19
NC	Y5	VCCA	T18	VCCIB1	H14
NC	Y6	VCCA	T9	VCCIB1	H15
PRA	E13	VCCA	U18	VCCIB1	H16
PRB	B14	VCCA	U9	VCCIB1	H17
PRC	Y14	VCCA	V10	VCCIB1	H18
PRD	AD14	VCCA	V11	VCCIB2	H20
TCK	E5	VCCA	V12	VCCIB2	J19
TDI	B3	VCCA	V13	VCCIB2	J20
TDO	G6	VCCA	V14	VCCIB2	K19
TMS	D4	VCCA	V15	VCCIB2	K20
TRST	A2	VCCA	V16	VCCIB2	L19
VCCA	AB4	VCCA	V17	VCCIB2	M19
VCCA	AF24	VCCDA	A3	VCCIB2	N19
VCCA	C1	VCCDA	AB22	VCCIB3	P19
VCCA	C26	VCCDA	AB5	VCCIB3	R19

FG896	
AX1000 Function	Pin Number
IO51PB1F4	E21
IO52NB1F4	F22
IO52PB1F4	E22
IO53NB1F4	B25
IO53PB1F4	B24
IO54NB1F5	D24
IO54PB1F5	D23
IO55NB1F5	F23
IO55PB1F5	E23
IO56NB1F5	H21
IO56PB1F5	G21
IO57NB1F5	D25
IO57PB1F5	C25
IO58NB1F5	F24
IO58PB1F5	E24
IO59NB1F5	D26
IO59PB1F5	C26
IO60NB1F5	G23
IO60PB1F5	G22
IO61NB1F5	B27
IO61PB1F5	A27
IO62NB1F5	F25
IO62PB1F5	E25
IO63NB1F5	H23
IO63PB1F5	H22
Bank 2	
IO64NB2F6	K23
IO64PB2F6	J23
IO65NB2F6	J24
IO65PB2F6	H24
IO66NB2F6	H26
IO66PB2F6	H25
IO67NB2F6	G26
IO67PB2F6	G25
IO68NB2F6	K25

FG896	
AX1000 Function	Pin Number
IO68PB2F6	K24
IO69NB2F6	F27
IO69PB2F6	E27
IO70NB2F6	J26
IO70PB2F6	J25
IO71NB2F6	H27
IO71PB2F6	G27
IO72NB2F6	J28
IO72PB2F6	H28
IO73NB2F6	G28
IO73PB2F6	F28
IO74NB2F7	L23
IO74PB2F7	L24
IO75NB2F7	L26
IO75PB2F7	K26
IO76NB2F7	M25
IO76PB2F7	L25
IO77NB2F7	K27
IO77PB2F7	J27
IO78NB2F7	M27
IO78PB2F7	L27
IO79NB2F7	K30
IO79PB2F7	K29
IO80NB2F7	M23
IO80PB2F7	M24
IO81NB2F7	M28
IO81PB2F7	L28
IO82NB2F7	N26
IO82PB2F7	M26
IO83NB2F7	N25
IO83PB2F7	N24
IO84NB2F7	N22
IO84PB2F7	N23
IO85NB2F8	M29
IO85PB2F8	L29

FG896	
AX1000 Function	Pin Number
IO86NB2F8	N28
IO86PB2F8	N27
IO87NB2F8	P29
IO87PB2F8	P30
IO88NB2F8	P25
IO88PB2F8	P24
IO89NB2F8	P28
IO89PB2F8	P27
IO90NB2F8	P22
IO90PB2F8	P23
IO91NB2F8	R26
IO91PB2F8	P26
IO92NB2F8	R24
IO92PB2F8	R25
IO93NB2F8	R29
IO93PB2F8	R30
IO94NB2F8	R22
IO94PB2F8	R23
IO95NB2F8	T27
IO95PB2F8	R27
Bank 3	
IO96NB3F9	T29
IO96PB3F9	T30
IO97NB3F9	U29
IO97PB3F9	U30
IO98NB3F9	T22
IO98PB3F9	T23
IO99NB3F9	U26
IO99PB3F9	T26
IO100NB3F9	U24
IO100PB3F9	T24
IO101NB3F9	V28
IO101PB3F9	U28
IO102NB3F9	U23
IO102PB3F9	U22

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
VCCIB0	C5	VCCIB3	AA24	VCCIB6	AA11
VCCIB0	D5	VCCIB3	AB23	VCCIB6	AA12
VCCIB0	L12	VCCIB3	AB24	VCCIB6	AB11
VCCIB0	L13	VCCIB3	AC24	VCCIB6	AB12
VCCIB0	L14	VCCIB3	AK31	VCCIB6	AC11
VCCIB0	M13	VCCIB3	AK32	VCCIB6	AK1
VCCIB0	M14	VCCIB3	AK33	VCCIB6	AK2
VCCIB0	M15	VCCIB3	AK34	VCCIB6	AK3
VCCIB0	M16	VCCIB3	V23	VCCIB6	AK4
VCCIB0	M17	VCCIB3	W23	VCCIB6	V12
VCCIB1	A30	VCCIB3	Y23	VCCIB6	W12
VCCIB1	B30	VCCIB4	AC18	VCCIB6	Y12
VCCIB1	C30	VCCIB4	AC19	VCCIB7	E1
VCCIB1	D30	VCCIB4	AC20	VCCIB7	E2
VCCIB1	L21	VCCIB4	AC21	VCCIB7	E3
VCCIB1	L22	VCCIB4	AC22	VCCIB7	E4
VCCIB1	L23	VCCIB4	AD21	VCCIB7	M11
VCCIB1	M18	VCCIB4	AD22	VCCIB7	N11
VCCIB1	M19	VCCIB4	AD23	VCCIB7	N12
VCCIB1	M20	VCCIB4	AL30	VCCIB7	P11
VCCIB1	M21	VCCIB4	AM30	VCCIB7	P12
VCCIB1	M22	VCCIB4	AN30	VCCIB7	R12
VCCIB2	E31	VCCIB4	AP30	VCCIB7	T12
VCCIB2	E32	VCCIB5	AC13	VCCIB7	U12
VCCIB2	E33	VCCIB5	AC14	VCCPLA	J16
VCCIB2	E34	VCCIB5	AC15	VCCPLB	K17
VCCIB2	M24	VCCIB5	AC16	VCCPLC	J19
VCCIB2	N23	VCCIB5	AC17	VCCPLD	L18
VCCIB2	N24	VCCIB5	AD12	VCCPLE	AK19
VCCIB2	P23	VCCIB5	AD13	VCCPLF	AE18
VCCIB2	P24	VCCIB5	AD14	VCCPLG	AK16
VCCIB2	R23	VCCIB5	AL5	VCCPLH	AF17
VCCIB2	T23	VCCIB5	AM5	VCOMPLA	H16
VCCIB2	U23	VCCIB5	AN5	VCOMPLB	L17
VCCIB3	AA23	VCCIB5	AP5	VCOMPLC	H19

CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO87PB4F8	171	IO119PB5F11	101	IO146NB6F13	46
IO89NB4F8	166	IO121NB5F11	98	IO146PB6F13	47
IO89PB4F8	167	IO121PB5F11	99	Bank 7	
IO94NB4F9	164	IO123NB5F11	94	IO147NB7F14	40
IO94PB4F9	165	IO123PB5F11	95	IO147PB7F14	41
IO95NB4F9	160	IO125NB5F11	92	IO148NB7F14	42
IO95PB4F9	161	IO125PB5F11	93	IO148PB7F14	43
IO97NB4F9	158	Bank 6		IO149NB7F14	36
IO97PB4F9	159	IO126PB6F12	86	IO149PB7F14	37
IO99NB4F9	154	IO127NB6F12	84	IO151NB7F14	30
IO99PB4F9	155	IO127PB6F12	85	IO151PB7F14	31
IO100NB4F9	146	IO129NB6F12	82	IO152NB7F14	34
IO100PB4F9	147	IO129PB6F12	83	IO152PB7F14	35
IO101NB4F9	152	IO131NB6F12	78	IO153NB7F14	28
IO101PB4F9	153	IO131PB6F12	79	IO153PB7F14	29
IO103NB4F9/CLKEN	142	IO133NB6F12	76	IO155NB7F14	24
IO103PB4F9/CLKEP	143	IO133PB6F12	77	IO155PB7F14	25
IO104NB4F9/CLKFN	136	IO134NB6F12	72	IO157NB7F14	22
IO104PB4F9/CLKFP	137	IO134PB6F12	73	IO157PB7F14	23
Bank 5		IO135NB6F12	70	IO159NB7F15	16
IO105NB5F10/CLKGN	128	IO135PB6F12	71	IO159PB7F15	17
IO105PB5F10/CLKGP	129	IO137NB6F13	66	IO160NB7F15	18
IO106NB5F10/CLKHN	122	IO137PB6F13	67	IO160PB7F15	19
IO106PB5F10/CLKHP	123	IO138NB6F13	64	IO161NB7F15	12
IO107NB5F10	118	IO138PB6F13	65	IO161PB7F15	13
IO107PB5F10	119	IO139NB6F13	60	IO163NB7F15	10
IO114NB5F11	112	IO139PB6F13	61	IO163PB7F15	11
IO114PB5F11	113	IO141NB6F13	54	IO165NB7F15	6
IO115NB5F11	110	IO141PB6F13	55	IO165PB7F15	7
IO115PB5F11	111	IO142NB6F13	58	IO167NB7F15	4
IO116NB5F11	106	IO142PB6F13	59	IO167PB7F15	5
IO116PB5F11	107	IO143NB6F13	52	Dedicated I/O	
IO117NB5F11	104	IO143PB6F13	53	GND	1
IO117PB5F11	105	IO145NB6F13	48	GND	9
IO119NB5F11	100	IO145PB6F13	49	GND	15

CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
GND	21	GND	240	TDI	348
GND	27	GND	246	TDO	347
GND	33	GND	252	TMS	350
GND	39	GND	258	TRST	351
GND	45	GND	264	VCCA	3
GND	51	GND	265	VCCA	14
GND	57	GND	274	VCCA	32
GND	63	GND	280	VCCA	56
GND	69	GND	286	VCCA	74
GND	75	GND	292	VCCA	87
GND	81	GND	298	VCCA	102
GND	88	GND	310	VCCA	114
GND	89	GND	322	VCCA	150
GND	97	GND	330	VCCA	162
GND	103	GND	334	VCCA	175
GND	109	GND	340	VCCA	191
GND	115	GND	345	VCCA	209
GND	121	GND/LP	352	VCCA	233
GND	133	NC	91	VCCA	251
GND	145	NC	117	VCCA	263
GND	151	NC	130	VCCA	279
GND	157	NC	131	VCCA	291
GND	163	NC	148	VCCA	329
GND	169	NC	174	VCCA	339
GND	176	NC	268	VCCDA	2
GND	177	NC	294	VCCDA	44
GND	186	NC	307	VCCDA	90
GND	192	NC	308	VCCDA	116
GND	198	NC	327	VCCDA	132
GND	204	NC	328	VCCDA	149
GND	210	PRA	312	VCCDA	178
GND	216	PRB	311	VCCDA	221
GND	222	PRC	135	VCCDA	266
GND	228	PRD	134	VCCDA	293
GND	234	TCK	349	VCCDA	309