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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	198
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	352-BFCQFP with Tie Bar
Supplier Device Package	352-CQFP (75x75)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-cq352m

$$P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po}$$

C_{load} = the output load (technology dependent)
 V_{CCI} = the output voltage (technology dependent)
 po = the number of outputs
 F_{po} = the average output frequency

$$P_{\text{memory}} = P_{11} * N_{\text{block}} * FR_{\text{CLK}} + P_{12} * N_{\text{block}} * FW_{\text{CLK}}$$

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
 F_{RCLK} = the read-clock frequency of the memory
 F_{WCLK} = the write-clock frequency of the memory

$$P_{\text{PLL}} = P_{13} * F_{\text{CLK}}$$

F_{RefCLK} = the clock frequency of the clock input of the PLL
 F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
 F_s = 100 MHz
 s = 1080

$$\Rightarrow P_{\text{HCLK}} = (P_1 + P_2 * s + P_3 * \sqrt{s}) * F_s = 79 \text{ mW}$$

and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{R-cells}} = P_7 * ms * F_s = 173 \text{ mW}$$

mc = 1 (1 C-cell in this shift-register)
and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{C-cells}} = P_8 * mc * F_s = 0.14 \text{ mW}$$

$F_{pi} \sim 0 \text{ MHz}$

and $pi = 1$ (1 reset input => this is why $F_{pi} = 0$)

$$\Rightarrow P_{\text{inputs}} = P_9 * pi * F_{pi} = 0 \text{ mW}$$

$F_{po} = 50 \text{ MHz}$

and $po = 1$

$$\Rightarrow P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po} = 27.10 \text{ mW}$$

No RAM/FIFO in this shift-register

$$\Rightarrow P_{\text{memory}} = 0 \text{ mW}$$

No PLL in this shift-register

$$\Rightarrow P_{\text{PLL}} = 0 \text{ mW}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}} = 276 \text{ mW}$$

$$P_{\text{dc}} = 7.5\text{mA} * 1.5\text{V} = 11.25 \text{ mW}$$

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}} = 11.25 \text{ mW} + 276\text{mW} = 290.30 \text{ mW}$$

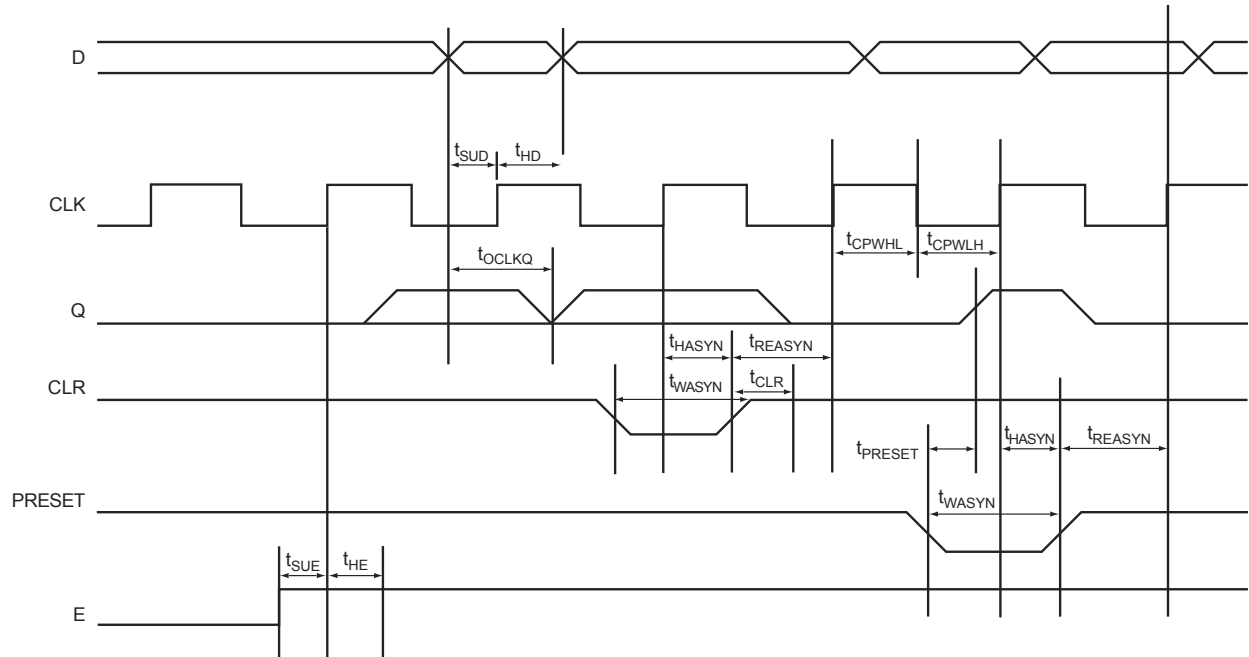


Figure 2-13 • Output Register Timing Characteristics

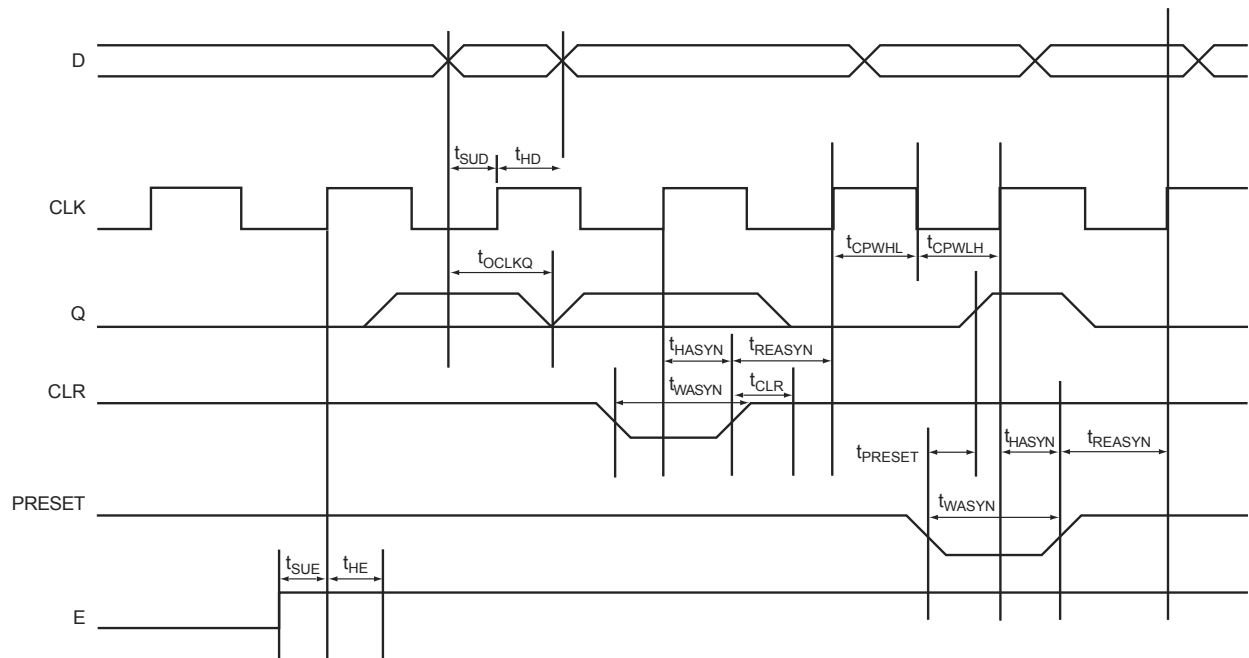


Figure 2-14 • Output Enable Register Timing Characteristics

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength =3 (16 mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		3.12		3.56		4.18	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.54		4.04		4.75	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.78		3.17		3.72	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.58		2.59		2.60	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-32 • 1.5V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.4 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS15 (JESD8-11) I/O Module Timing								
t _{DP}	Input Buffer		3.59		4.09		4.81	ns
t _{PY}	Output Buffer		6.05		6.89		8.10	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.31		3.34		3.34	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.56		4.58		4.59	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.37		7.25		8.52	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.94		7.90		9.29	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-61 • LVPECL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVPECL Output Module Timing								
t _{DP}	Input Buffer		1.66		1.89		2.22	ns
t _{PY}	Output Buffer		2.24		2.55		3.00	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Model and Waveforms

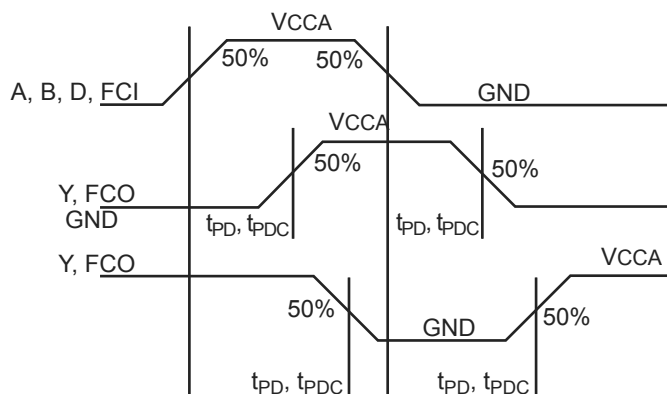


Figure 2-28 • C-Cell Timing Model and Waveforms

Timing Characteristics

Table 2-62 • C-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t _{PD}	Any input to output Y	0.74		0.84		0.99		ns
t _{PDC}	Any input to carry chain output (FCO)	0.57		0.64		0.76		ns
t _{PDB}	Any input through DB when one input is used	0.95		1.09		1.28		ns
t _{CCY}	Input to carry chain (FCI) to Y	0.61		0.69		0.82		ns
t _{CC}	Input to carry chain (FCI) to carry chain output (FCO)	0.08		0.09		0.11		ns

PLLCLK and PLLHCLK

PLLCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 2-44).

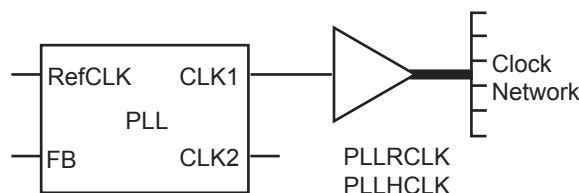


Figure 2-44 • PLLCLK and PLLHCLK

Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc. (Figure 2-45).

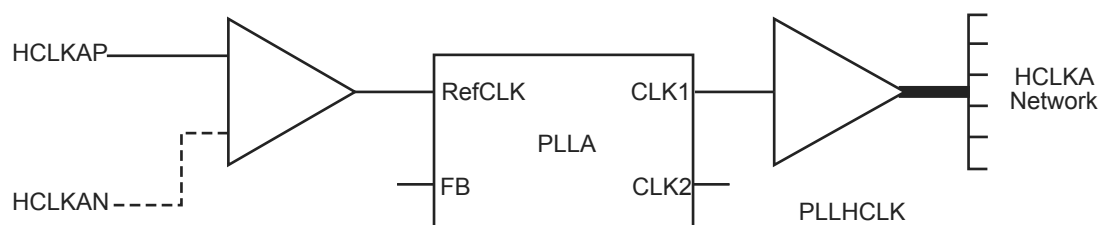


Figure 2-45 • Example of HCLKA Driven from a PLL with External Clock Source

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 2-46).

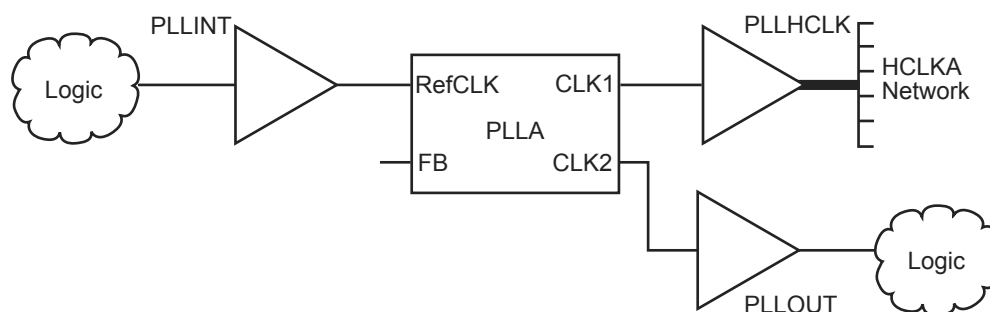


Figure 2-46 • Example of PLLINT and PLLOUT Usage

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 2-64). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 2-64).

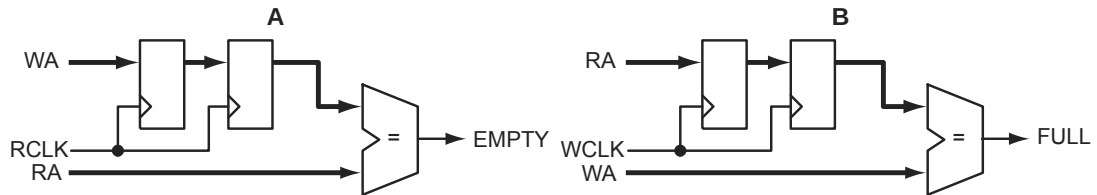


Figure 2-64 • Overflow and Underflow Control

FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 2-96.

Table 2-96 • FIFO Width Configurations

WIDTH(2:0)	W x D
000	1 x 4k
001	2 x 2k
010	4 x 1k
011	9 x 512
100	18 x 256
101	36 x 128
11x	reserved

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-86 on page 2-87 describes the FIFO depth options for various data width and memory blocks.

Interface

Figure 2-65 on page 2-99 shows a logic block diagram of the Accelerator FIFO module.

Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using SmartGen, the user only needs to specify the depth and width of the necessary FIFO blocks. SmartGen automatically configures these blocks to optimize performance.

Clock

As with RAM configuration, the RCLK and WCLK pins have independent polarity selection.

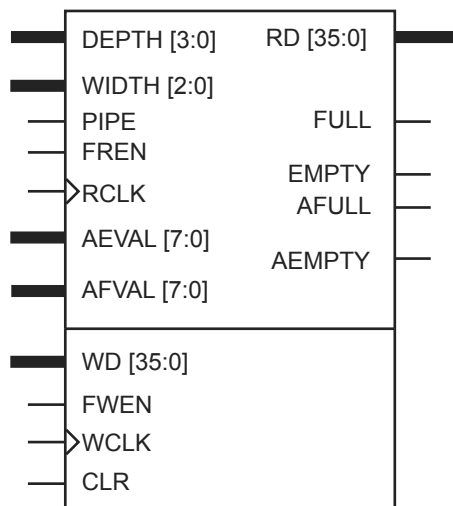


Figure 2-65 • FIFO Block Diagram

Table 2-97 • FIFO Signal Description

Signal	Direction	Description
WCLK	Input	Write clock (active either edge).
FWEN	Input	FIFO write enable. When this signal is asserted, the WD bus data is latched into the FIFO, and the internal write counters are incremented.
WD[N-1:0]	Input	Write data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
FULL	Output	Active high signal indicating that the FIFO is FULL. When this signal is set, additional write requests are ignored.
AFULL	Output	Active high signal indicating that the FIFO is AFULL.
AFVAL	Input	8-bit input defining the AFULL value of the FIFO.
RCLK	Input	Read clock (active either edge).
FREN	Input	FIFO read enable.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
EMPTY	Output	Empty flag indicating that the FIFO is EMPTY. When this signal is asserted, attempts to read the FIFO will be ignored.
AEMPTY	Output	Active high signal indicating that the FIFO is AEMPTY.
AEVAL	Input	8-bit input defining the almost-empty value of the FIFO.
PIPE	Input	Sets the pipe option on or off.
CLR	Input	Active high clear input.
DEPTH	Input	Determines the depth of the FIFO and the number of FIFOs to be cascaded.
WIDTH	Input	Determines the width of the dataword/FIFO, and the number of the FIFOs to be cascaded.

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0					
IO00NB0F0	E6	IO18NB0F1	C10	IO36NB1F3	H15
IO00PB0F0	F6	IO18PB0F1	C9	IO36PB1F3	G15
IO01NB0F0	G8	IO19NB0F1	E11	IO37NB1F3	C17
IO01PB0F0	G7	IO19PB0F1	F11	IO37PB1F3	C16
IO02NB0F0	D7	IO20NB0F1	G12	IO38NB1F3	B18
IO02PB0F0	E7	IO20PB0F1	H12	IO38PB1F3	B17
IO03NB0F0	D5	IO21NB0F1	D11	IO39NB1F3	A18
IO03PB0F0	E5	IO21PB0F1	D10	IO39PB1F3	A17
IO04NB0F0	G9	IO22NB0F2	A10	IO40NB1F3	H16
IO04PB0F0	H9	IO22PB0F2	A9	IO40PB1F3	G16
IO05NB0F0	E8	IO23NB0F2	B11	IO41NB1F4	B19
IO05PB0F0	F8	IO23PB0F2	B10	IO41PB1F4	A19
IO06NB0F0	C6	IO24NB0F2	G13	IO42NB1F4	C19
IO06PB0F0	D6	IO24PB0F2	H13	IO42PB1F4	C18
IO07NB0F0	B5	IO25NB0F2	C12	IO43NB1F4	D18
IO07PB0F0	C5	IO25PB0F2	C11	IO43PB1F4	D17
IO08NB0F0	A6	IO26NB0F2	E12	IO44NB1F4	H17
IO08PB0F0	A5	IO26PB0F2	D12	IO44PB1F4	G17
IO09NB0F0	E9	IO27NB0F2	E13	IO45NB1F4	F17
IO09PB0F0	F9	IO27PB0F2	F13	IO45PB1F4	E17
IO10NB0F0	G10	IO28NB0F2	G14	IO46NB1F4	B20
IO10PB0F0	H10	IO28PB0F2	H14	IO46PB1F4	A20
IO11NB0F0	B7	IO29NB0F2	A12	IO47NB1F4	C21
IO11PB0F0	B6	IO29PB0F2	B12	IO47PB1F4	C20
IO12NB0F1	C8	IO30NB0F2/HCLKAN	C13	IO48NB1F4	H18
IO12PB0F1	C7	IO30PB0F2/HCLKAP	D13	IO48PB1F4	G18
IO13NB0F1	E10	IO31NB0F2/HCLKBN	F14	IO49NB1F4	F18
IO13PB0F1	F10	IO31PB0F2/HCLKBP	E14	IO49PB1F4	E18
IO14NB0F1	G11	Bank 1		IO50NB1F4	D20
IO14PB0F1	H11	IO32NB1F3/HCLKCN	C14	IO50PB1F4	D19
IO15NB0F1	D9	IO32PB1F3/HCLKCP	B14	IO51NB1F4	A22
IO15PB0F1	D8	IO33NB1F3/HCLKDN	D16	IO51PB1F4	A21
IO16NB0F1	A8	IO33PB1F3/HCLKDP	D15	IO52NB1F4	B22
IO16PB0F1	A7	IO34NB1F3	B16	IO52PB1F4	B21
IO17NB0F1	B9	IO34PB1F3	A16	IO53NB1F4	F19
IO17PB0F1	B8	IO35NB1F3	E15	IO53PB1F4	E19
		IO35PB1F3	F15	IO54NB1F5	F20

FG484		FG484		FG484	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO54PB2F5	H22	IO72PB3F6	P20	IO90NB4F8	Y17
IO55NB2F5	L17	IO73PB3F6	R19	IO90PB4F8	Y18
IO55PB2F5	K17	IO74NB3F7	V21	IO91NB4F8	V15
IO56NB2F5	K21	IO74PB3F7	U21	IO91PB4F8	V16
IO56PB2F5	K22	IO75NB3F7	V22	IO92PB4F8	AB17
IO58NB2F5	L20	IO75PB3F7	U22	IO93NB4F8	Y15
IO58PB2F5	K20	IO76NB3F7	U20	IO93PB4F8	Y16
IO59NB2F5	L18	IO76PB3F7	T20	IO94NB4F9	AA16
IO59PB2F5	K18	IO77NB3F7	R17	IO94PB4F9	AA17
IO60NB2F5	M21	IO77PB3F7	P17	IO95NB4F9	AB14
IO60PB2F5	L21	IO78NB3F7	W21	IO95PB4F9	AB15
IO61NB2F5	L16	IO78PB3F7	W22	IO96NB4F9	W15
IO61PB2F5	K16	IO79NB3F7	T18	IO96PB4F9	W16
IO62NB2F5	M19	IO79PB3F7	R18	IO97NB4F9	AA13
IO62PB2F5	L19	IO80NB3F7	W20	IO97PB4F9	AB13
Bank 3		IO80PB3F7	V20	IO98NB4F9	AA14
IO63NB3F6	N16	IO81NB3F7	U19	IO98PB4F9	AA15
IO63PB3F6	M16	IO81PB3F7	T19	IO100NB4F9	Y14
IO64NB3F6	P22	IO82NB3F7	U18	IO100PB4F9	W14
IO64PB3F6	N22	IO82PB3F7	V19	IO101NB4F9	Y12
IO65NB3F6	N20	IO83NB3F7	R16	IO101PB4F9	Y13
IO65PB3F6	M20	IO83PB3F7	P16	IO102NB4F9	AA11
IO66NB3F6	P21	Bank 4		IO102PB4F9	AA12
IO66PB3F6	N21	IO84NB4F8	AB18	IO103NB4F9/CLKEN	V12
IO67NB3F6	N18	IO84PB4F8	AB19	IO103PB4F9/CLKEP	V13
IO67PB3F6	N19	IO85NB4F8	T15	IO104NB4F9/CLKFN	W11
IO68NB3F6	T22	IO85PB4F8	T16	IO104PB4F9/CLKFP	W12
IO68PB3F6	R22	IO86NB4F8	AA18	Bank 5	
IO69NB3F6	N17	IO86PB4F8	AA19	IO105NB5F10/CLKGN	U10
IO69PB3F6	M17	IO87NB4F8	W17	IO105PB5F10/CLKGP	U11
IO70NB3F6	T21	IO87PB4F8	V17	IO106NB5F10/CLKHN	V9
IO70PB3F6	R21	IO88NB4F8	Y19	IO106PB5F10/CLKHP	V10
IO71NB3F6	P18	IO88PB4F8	W18	IO107NB5F10	Y10
IO71PB3F6	P19	IO89NB4F8	U14	IO107PB5F10	Y11
IO72NB3F6	R20	IO89PB4F8	U15	IO108NB5F10	AA9

FG484	
AX500 Function	Pin Number
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX500 Function	Pin Number
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX500 Function	Pin Number
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9

FG676	
AX500 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21

FG676	
AX500 Function	Pin Number
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	Pin Number
VCOMPLH	Y13
VPUMP	E22

FG896	
AX1000 Function	Pin Number
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

FG896	
AX1000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX1000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
NC	AP9	PRB	F18	VCCA	T22
NC	B17	PRC	AD18	VCCA	U13
NC	B22	PRD	AH18	VCCA	U22
NC	B27	TCK	J9	VCCA	V13
NC	B8	TDI	F7	VCCA	V22
NC	D10	TDO	L10	VCCA	W13
NC	D20	TMS	H8	VCCA	W22
NC	D23	TRST	E6	VCCA	Y13
NC	D25	VCCA	AA13	VCCA	Y22
NC	F3	VCCA	AA22	VCCDA	AF26
NC	F32	VCCA	AB14	VCCDA	AF9
NC	F33	VCCA	AB15	VCCDA	AG17
NC	F34	VCCA	AB16	VCCDA	AG18
NC	F4	VCCA	AB17	VCCDA	AH14
NC	G1	VCCA	AB18	VCCDA	AH15
NC	G32	VCCA	AB19	VCCDA	AH17
NC	G33	VCCA	AB20	VCCDA	AH20
NC	G34	VCCA	AB21	VCCDA	AH21
NC	H31	VCCA	AF8	VCCDA	AK29
NC	H33	VCCA	AK28	VCCDA	AK6
NC	J1	VCCA	G30	VCCDA	E15
NC	J3	VCCA	G5	VCCDA	E29
NC	J34	VCCA	N14	VCCDA	E7
NC	M1	VCCA	N15	VCCDA	F15
NC	M4	VCCA	N16	VCCDA	F21
NC	P1	VCCA	N17	VCCDA	F5
NC	P2	VCCA	N18	VCCDA	G20
NC	R31	VCCA	N19	VCCDA	H17
NC	T1	VCCA	N20	VCCDA	H18
NC	T2	VCCA	N21	VCCDA	H28
NC	V3	VCCA	P13	VCCDA	J18
NC	V34	VCCA	P22	VCCDA	V27
NC	W3	VCCA	R13	VCCDA	V6
NC	W34	VCCA	R22	VCCIB0	A5
PRA	J17	VCCA	T13	VCCIB0	B5

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX250 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
GND	21	GND	240	TDI	348
GND	27	GND	246	TDO	347
GND	33	GND	252	TMS	350
GND	39	GND	258	TRST	351
GND	45	GND	264	VCCA	3
GND	51	GND	265	VCCA	14
GND	57	GND	274	VCCA	32
GND	63	GND	280	VCCA	56
GND	69	GND	286	VCCA	74
GND	75	GND	292	VCCA	87
GND	81	GND	298	VCCA	102
GND	88	GND	310	VCCA	114
GND	89	GND	322	VCCA	150
GND	97	GND	330	VCCA	162
GND	103	GND	334	VCCA	175
GND	109	GND	340	VCCA	191
GND	115	GND	345	VCCA	209
GND	121	GND/LP	352	VCCA	233
GND	133	NC	91	VCCA	251
GND	145	NC	117	VCCA	263
GND	151	NC	130	VCCA	279
GND	157	NC	131	VCCA	291
GND	163	NC	148	VCCA	329
GND	169	NC	174	VCCA	339
GND	176	NC	268	VCCDA	2
GND	177	NC	294	VCCDA	44
GND	186	NC	307	VCCDA	90
GND	192	NC	308	VCCDA	116
GND	198	NC	327	VCCDA	132
GND	204	NC	328	VCCDA	149
GND	210	PRA	312	VCCDA	178
GND	216	PRB	311	VCCDA	221
GND	222	PRC	135	VCCDA	266
GND	228	PRD	134	VCCDA	293
GND	234	TCK	349	VCCDA	309

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO194NB6F18	Y3	IO215PB6F20	V4	IO237NB7F22	N8
IO194PB6F18	AA3	IO216NB6F20	P8	IO237PB7F22	N7
IO195NB6F18	V6	IO216PB6F20	R3	IO238NB7F22	M5
IO195PB6F18	W4	IO217NB6F20	P7	IO239NB7F22	L6
IO197NB6F18	R5	IO217PB6F20	R7	IO239PB7F22	L5
IO197PB6F18	U3	IO219NB6F20	R4	IO240NB7F22	M4
IO198NB6F18	P6	IO219PB6F20	T4	IO241NB7F22	L7
IO199NB6F18	Y5	IO220NB6F20	P2	IO241PB7F22	M7
IO199PB6F18	W5	IO220PB6F20	R2	IO242NB7F22	J3
IO200NB6F18	V3	IO221NB6F20	N4	IO243NB7F22	M9
IO200PB6F18	W3	IO221PB6F20	P4	IO243PB7F22	M8
IO201NB6F18	T7	IO223NB6F20	M2	IO244NB7F22	P9
IO201PB6F18	U7	IO223PB6F20	N2	IO244PB7F22	N6
IO202NB6F18	V2	IO224NB6F20	N3	IO245NB7F22	K8
IO203NB6F19	W2	IO224PB6F20	P3	IO245PB7F22	L8
IO203PB6F19	Y2	Bank 7		IO246NB7F22	F3
IO204NB6F19	AA1	IO225NB7F21	J2	IO246PB7F22	E3
IO204PB6F19	AB1	IO225PB7F21	J1	IO247NB7F23	K7
IO205NB6F19	R6	IO226PB7F21	G2	IO247PB7F23	K6
IO205PB6F19	T6	IO227NB7F21	H3	IO248NB7F23	D2
IO206NB6F19	W1	IO227PB7F21	H2	IO249NB7F23	G4
IO206PB6F19	Y1	IO229NB7F21	K2	IO249PB7F23	G3
IO207NB6F19	T2	IO229PB7F21	L2	IO251NB7F23	N10
IO207PB6F19	U2	IO230NB7F21	K1	IO251PB7F23	N9
IO208NB6F19	T1	IO230PB7F21	L1	IO253NB7F23	H4
IO208PB6F19	U1	IO231NB7F21	E2	IO253PB7F23	J4
IO209NB6F19	AA2	IO231PB7F21	F2	IO255NB7F23	J6
IO209PB6F19	AB2	IO232NB7F21	F1	IO255PB7F23	J5
IO210NB6F19	P5	IO232PB7F21	G1	IO257NB7F23	H5
IO211NB6F19	M1	IO233NB7F21	L3	IO257PB7F23	H6
IO211PB6F19	N1	IO233PB7F21	M3	Dedicated I/O	
IO212NB6F19	P1	IO234NB7F21	D1	GND	K5
IO212PB6F19	R1	IO234PB7F21	E1	GND	A18
IO213NB6F19	R8	IO235NB7F21	K4	GND	A2
IO213PB6F19	T8	IO235PB7F21	L4	GND	A24
IO215NB6F20	U4	IO236NB7F22	M6	GND	A25