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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	138
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Axcelerator Family Device Status

Axcelerator [®] Devices	Status
AX125	Production
AX250	Production
AX500	Production
AX1000	Production
AX2000	Production

Temperature Grade Offerings

Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	-	C, I, M	C, I, M	-	-
CQ208	-	М	М	-	-
CQ256	-	-	-	-	М
FG256	C, I	C, I, M	-	-	-
FG324	C, I	_	-	_	-
CQ352	-	М	М	М	М
FG484	-	C, I, M	C, I, M	C, I, M	-
CG624	_	_	_	М	М
FG676	-	_	C, I, M	C, I, M	-
BG729	-	-	-	C, I, M	-
FG896	_	_	-	C, I, M	C, I, M
FG1152	_	_	_	_	C, I, M

C = Commercial

I = Industrial

M = Military

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std	-1	-2
С	\checkmark	\checkmark	\checkmark
1	\checkmark	\checkmark	\checkmark
Μ	\checkmark	\checkmark	-

C = Commercial

I = Industrial

M = Military

Microsemi

Axcelerator Family FPGAs

Packaging Data

Refer to the following documents located on the Microsemi SoC Products Group website for additional packaging information.

Package Mechanical Drawings

Package Thermal Characteristics and Weights

Hermatic Package Mechanical Information

Contact your local Microsemi representative for device availability.



Package Pin Assignments

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CG624		CG624		CG624	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
Bank 0		IO27NB0F2	H10	IO51NB1F4	E15
IO00NB0F0	D7*	IO27PB0F2	H9	IO51PB1F4	F15
IO00PB0F0	E7*	IO28NB0F2	A9	IO52NB1F4	A17
IO01NB0F0	G7	IO28PB0F2	B9	IO55NB1F5	G16
IO01PB0F0	G6	IO30NB0F2	B11	IO55PB1F5	H16
IO02NB0F0	B5	IO30PB0F2	B10	IO56NB1F5	A20
IO02PB0F0	B4	IO31NB0F2	E11	IO56PB1F5	A19
IO04PB0F0	C7	IO31PB0F2	F11	IO57NB1F5	D16
IO05NB0F0	F8	IO33NB0F2	D12	IO57PB1F5	D15
IO05PB0F0	F7	IO33PB0F2	D11	IO58NB1F5	A22
IO06NB0F0	H8	IO34NB0F3	A11	IO58PB1F5	A21
IO06PB0F0	H7	IO34PB0F3	A10	IO59NB1F5	F16
IO11NB0F0	J8	IO37NB0F3	J13	IO61NB1F5	G17
IO11PB0F0	J7	IO37PB0F3	K13	IO61PB1F5	H17
IO12PB0F1	B6	IO38NB0F3	H11	IO62NB1F5	B17
IO13NB0F1	E9*	IO38PB0F3	G11	IO62PB1F5	B16
IO13PB0F1	D8*	IO40PB0F3	B12	IO63NB1F5	H18
IO15NB0F1	C9	IO41NB0F3/HCLKAN	G13	IO65NB1F6	C17
IO15PB0F1	C8	IO41PB0F3/HCLKAP	G12	IO66PB1F6	B18
IO16NB0F1	A5	IO42NB0F3/HCLKBN	C13	IO67NB1F6	J18
IO16PB0F1	A4	IO42PB0F3/HCLKBP	C12	IO67PB1F6	J19
IO17NB0F1	D10	Bank 1	Bank 1		B20
IO17PB0F1	D9	IO43NB1F4/HCLKCN	G15	IO68PB1F6	B19
IO18NB0F1	A7	IO43PB1F4/HCLKCP	G14	IO69NB1F6	E17
IO18PB0F1	A6	IO44NB1F4/HCLKDN	B14	IO69PB1F6	F17
IO19NB0F1	G9	IO44PB1F4/HCLKDP	B13	IO70NB1F6	B22
IO19PB0F1	G8	IO45NB1F4	H13	IO70PB1F6	B21
IO20PB0F1	B7	IO47NB1F4	D14	IO71PB1F6	G18
IO23NB0F2	F10	IO47PB1F4	C14	IO73NB1F6	G19
IO23PB0F2	F9	IO48NB1F4	A16	IO74NB1F6	C19
IO26NB0F2	C11*	IO48PB1F4	A15	IO74PB1F6	C18
IO26PB0F2	B8*	IO49PB1F4	H15	IO75NB1F6	D18
Note: *Not routed on t	the same	Note: *Not routed on the	e same	Note: *Not routed on th	e same

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O. e: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

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