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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4224 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 55296 |
| Number of I/O | 138 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ax250-fgg256 |

## User-Defined Supply Pins

**VREF** **Supply Voltage**

Reference voltage for I/O banks. VREF pins are configured by the user from regular I/O pins; VREF pins are not in fixed locations. There can be one or more VREF pins in an I/O bank.

## Global Pins

**HCLKA/B/C/D** **Dedicated (Hardwired) Clocks A, B, C and D**

These pins are the clock inputs for sequential modules or north PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When the HCLK pins are unused, it is recommended that they are tied to ground.

**CLKE/F/G/H** **Routed Clocks E, F, G, and H**

These pins are clock inputs for clock distribution networks or south PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. The clock input is buffered prior to clocking the R-cells. When the CLK pins are unused, Microsemi recommends that they are tied to ground.

## JTAG/Probe Pins

**PRA/B/C/D** **Probe A, B, C and D**

The Probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins' probe capabilities can be permanently disabled to protect programmed design confidentiality. The probe pins are of LVTTL output levels.

**TCK** **Test Clock**

Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

**TDI** **Test Data Input**

Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal 10 kΩ pull-up resistor.

**TDO** **Test Data Output**

Serial output for JTAG boundary-scan testing.

**TMS** **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, TRST). TMS is equipped with an internal 10 kΩ pull-up resistor.

**TRST** **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a 10 kΩ pull-up resistor.

## Special Functions

**LP** **Low Power Pin**

The LP pin controls the low power mode of Axcelerator devices. The device is placed in the low power mode by connecting the LP pin to logic high. To exit the low power mode, the LP pin must be set Low. Additionally, the LP pin must be set Low during chip powering-up or chip powering-down operations. See "Low Power Mode" on page 2-106 for more details.

**NC** **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

## User I/O Naming Conventions

Due to the complex and flexible nature of the Axcelerator family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (Figure 2-7).

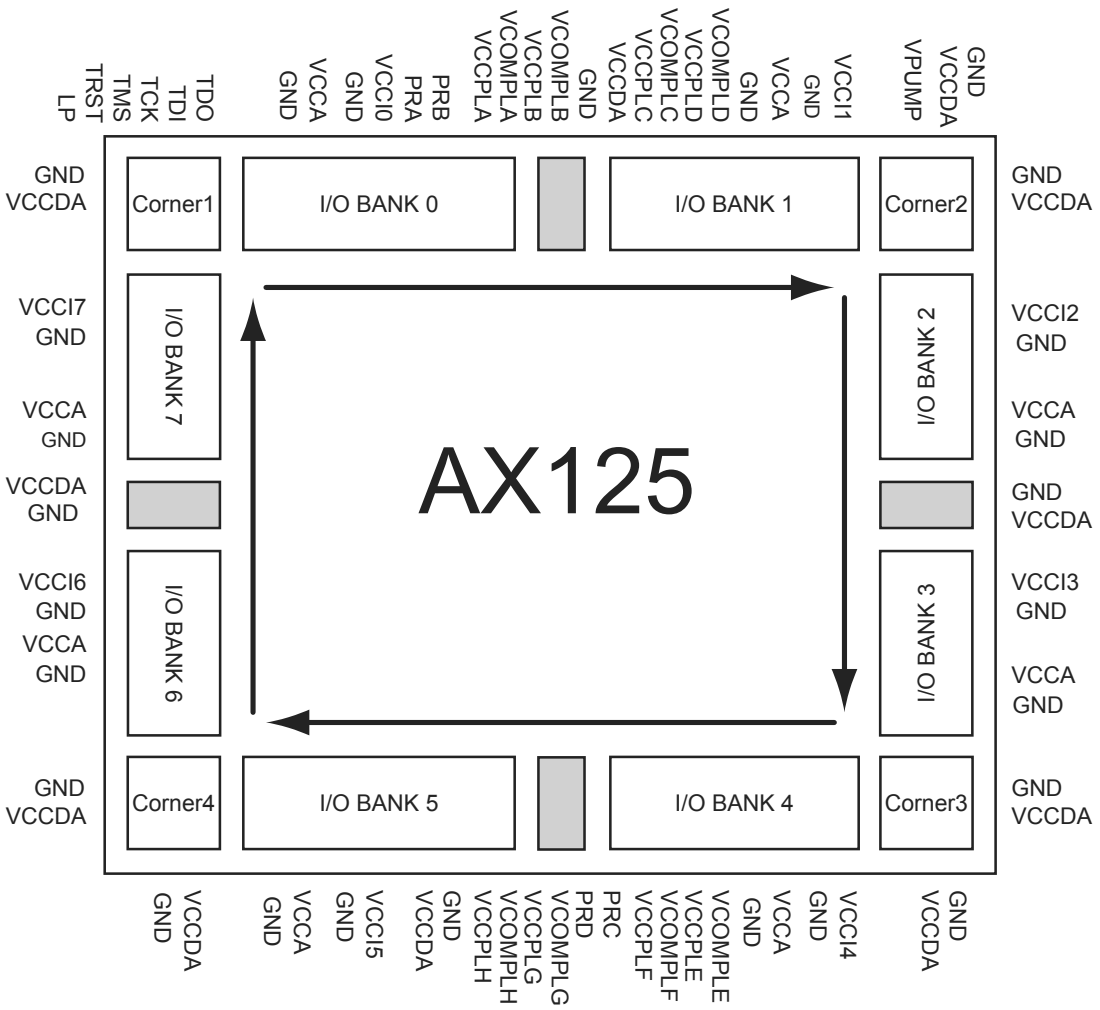
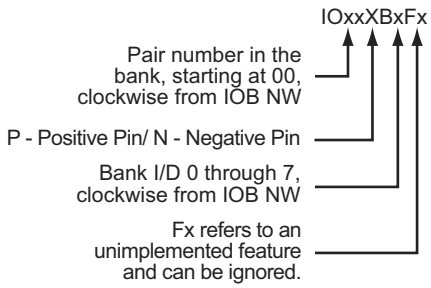



***Figure 2-7 •*** **I/O Bank and Dedicated Pin Layout**




**Examples:**

**IO12PB1F1** is the positive pin of the thirteenth pair of the first I/O bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair.

*For those I/Os that can be employed either as a user I/O or as a special function, the following nomenclature is used:*

**IOxxXBxFx/special_function_name**

**IOxxPB1Fx/xCLKx** this pin can be configured as a clock input or as a user I/O.

***Figure 2-8 •*** **General Naming Schemes**

***Table 2-22* • 3.3 V LVTTL I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C (continued)**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **LVTTL Output Drive Strength =3 (16 mA) / High Slew Rate** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.68 | | 1.92 | | 2.26 | ns |
| $t_{PY}$ | Output Buffer | | 3.12 | | 3.56 | | 4.18 | ns |
| $t_{ENZL}$ | Enable to Pad Delay through the Output Buffer—Z to Low | | 3.54 | | 4.04 | | 4.75 | ns |
| $t_{ENZH}$ | Enable to Pad Delay through the Output Buffer—Z to High | | 2.78 | | 3.17 | | 3.72 | ns |
| $t_{ENLZ}$ | Enable to Pad Delay through the Output Buffer—Low to Z | | 1.91 | | 1.93 | | 1.93 | ns |
| $t_{ENHZ}$ | Enable to Pad Delay through the Output Buffer—High to Z | | 2.58 | | 2.59 | | 2.60 | ns |
| $t_{IOCLKQ}$ | Sequential Clock-to-Q for the I/O Input Register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{IOCLKY}$ | Clock-to-output Y for the I/O Output Register and the I/O Enable Register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |

## SSTL2

Stub Series Terminated Logic for 2.5 V is a general-purpose 2.5 V memory bus standard (JESD8-9). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

### Class I

***Table 2-44* • DC Input and Output Levels**

| VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|
| **Min., V** | **Max., V** | **Min., V** | **Max., V** | **Max., V** | **Min., V** | **mA** | **mA** |
| –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | VREF – 0.57 | VREF + 0.57 | 7.6 | –7.6 |

### AC Loadings

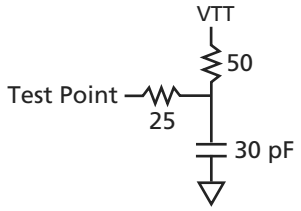



***Figure 2-21* • AC Test Loads**

***Table 2-45* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ) (V) | $C_{load}$ (pF) |
|---|---|---|---|---|
| VREF – 0.75 | VREF + 0.75 | VREF | 1.25 | 30 |

*Note: * Measuring Point = VTRIP*

### Timing Characteristics

***Table 2-46* • 2.5 V SSTL2 Class I I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **2.5 V SSTL2 Class I I/O Module Timing** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.83 | | 2.08 | | 2.45 | ns |
| $t_{PY}$ | Output Buffer | | 2.39 | | 2.72 | | 3.20 | ns |
| $t_{ICLKQ}$ | Clock-to-Q for the I/O input register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{OCLKQ}$ | Clock-to-Q for the I/O output register and the I/O enable register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |

## SSTL3

Stub Series Terminated Logic for 3.3 V is a general-purpose 3.3 V memory bus standard (JESD8-8). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

### Class I

***Table 2-50* • DC Input and Output Levels**

| VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|
| **Min., V** | **Max., V** | **Min., V** | **Max., V** | **Max., V** | **Min., V** | **mA** | **mA** |
| -0.3 | VREF – 0.2 | VREF +0.2 | 3.6 | VREF – 0.6 | VREF + 0.6 | 8 | –8 |

### AC Loadings

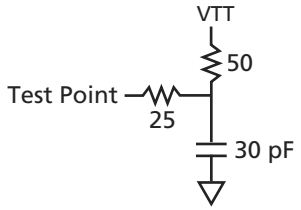



***Figure 2-23* • AC Test Loads**

***Table 2-51* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ) (V) | $C_{load}$ (pF) |
|---|---|---|---|---|
| VREF – 1.0 | VREF + 1.0 | VREF | 1.50 | 30 |

*Note: *Measuring Point = VTRIP*

### Timing Characteristics

***Table 2-52* • 3.3 V SSTL3 Class I I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **3.3 V SSTL3 Class I I/O Module Timing** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.78 | | 2.03 | | 2.39 | ns |
| $t_{PY}$ | Output Buffer | | 2.17 | | 2.47 | | 2.91 | ns |
| $t_{ICLKQ}$ | Clock-to-Q for the I/O input register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{OCLKQ}$ | Clock-to-Q for the I/O output register and the I/O enable register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |

### Class II

**Table 2-53 • DC Input and Output Levels**

| VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|
| Min., V | Max., V | Min., V | Max., V | Max., V | Min., V | mA | mA |
| -0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | VREF – 0.8 | VREF + 0.8 | 16 | –16 |

## AC Loadings

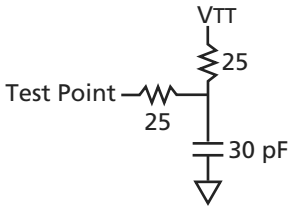



**Figure 2-24 • AC Test Loads**

**Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ) (V) | $C_{load}$ (pF) |
|---|---|---|---|---|
| VREF – 1.0 | VREF + 1.0 | VREF | 1.50 | 30 |

*Note: * Measuring Point = VTRIP*

## Timing Characteristics

**Table 2-55 • 3.3 V SSTL3 Class II I/O Module**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| **3.3 V SSTL3 Class II I/O Module Timing** | | | | | | | | |
| $t_{DP}$ | Input Buffer | | 1.85 | | 2.10 | | 2.47 | ns |
| $t_{PY}$ | Output Buffer | | 2.17 | | 2.47 | | 2.91 | ns |
| $t_{ICLKQ}$ | Clock-to-Q for the I/O input register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{OCLKQ}$ | Clock-to-Q for the I/O output register and the I/O enable register | | 0.67 | | 0.77 | | 0.90 | ns |
| $t_{SUD}$ | Data Input Set-Up | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{SUE}$ | Enable Input Set-Up | | 0.26 | | 0.30 | | 0.35 | ns |
| $t_{HD}$ | Data Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{HE}$ | Enable Input Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CPWHL}$ | Clock Pulse Width High to Low | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{CPWLH}$ | Clock Pulse Width Low to High | 0.39 | | 0.39 | | 0.39 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 0.37 | | 0.37 | | 0.37 | | ns |
| $t_{REASYN}$ | Asynchronous Recovery Time | | 0.13 | | 0.15 | | 0.17 | ns |
| $t_{HASYN}$ | Asynchronous Removal Time | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 0.23 | | 0.27 | | 0.31 | ns |

## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

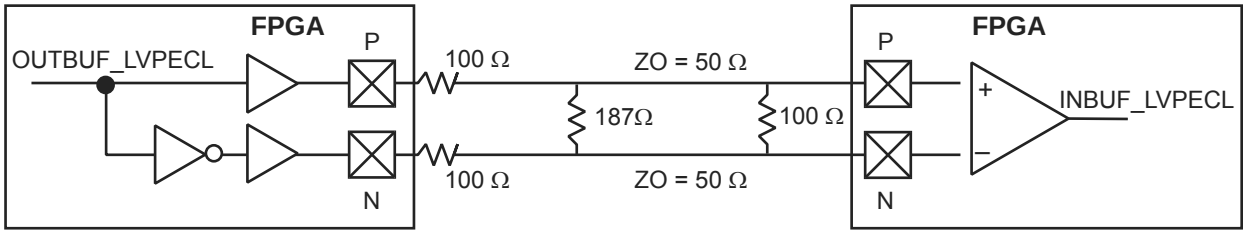



***Figure 2-26 •*** **LVPECL Board-Level Implementation**

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS since the output voltage levels are different. Please note that the VOH levels are 200 mV below the standard LVPECL levels.

***Table 2-59 •*** **DC Input and Output Levels**

| | Min. | | Typ. | | Max. | | |
|---|---|---|---|---|---|---|---|
| **DC Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| VCCI | 3 | | 3.3 | | 3.6 | | V |
| VOH | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VOL | 0.96 | 1.27 | 1.06 | 1.43 | 1.3 | 1.57 | V |
| VIH | 1.49 | 2.72 | 1.49 | 2.72 | 1.49 | 2.72 | V |
| VIL | 0.86 | 2.125 | 0.86 | 2.125 | 0.86 | 2.125 | V |
| Differential Input Voltage | 0.3 | | 0.3 | | 0.3 | | V |

***Table 2-60 •*** **AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) |
|---|---|---|
| 1.6 – 0.3 | 1.6 + 0.3 | 1.6 |

*Note: * Measuring Point = VTRIP*

# Axcelerator Clock Management System

## Introduction

Each member of the Axcelerator family[6] contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20µs

## Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 µF and 10 µF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

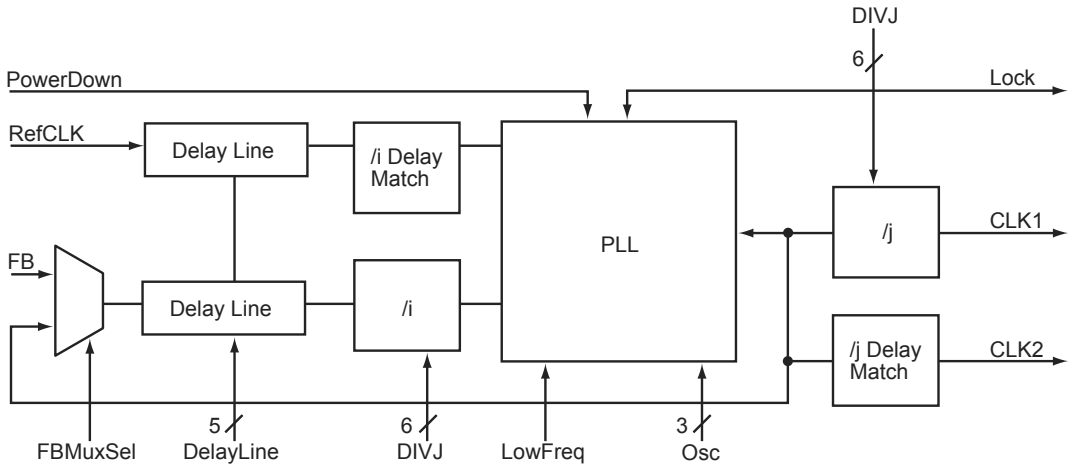



***Figure 2-48 •*** **PLL Block Diagram**

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

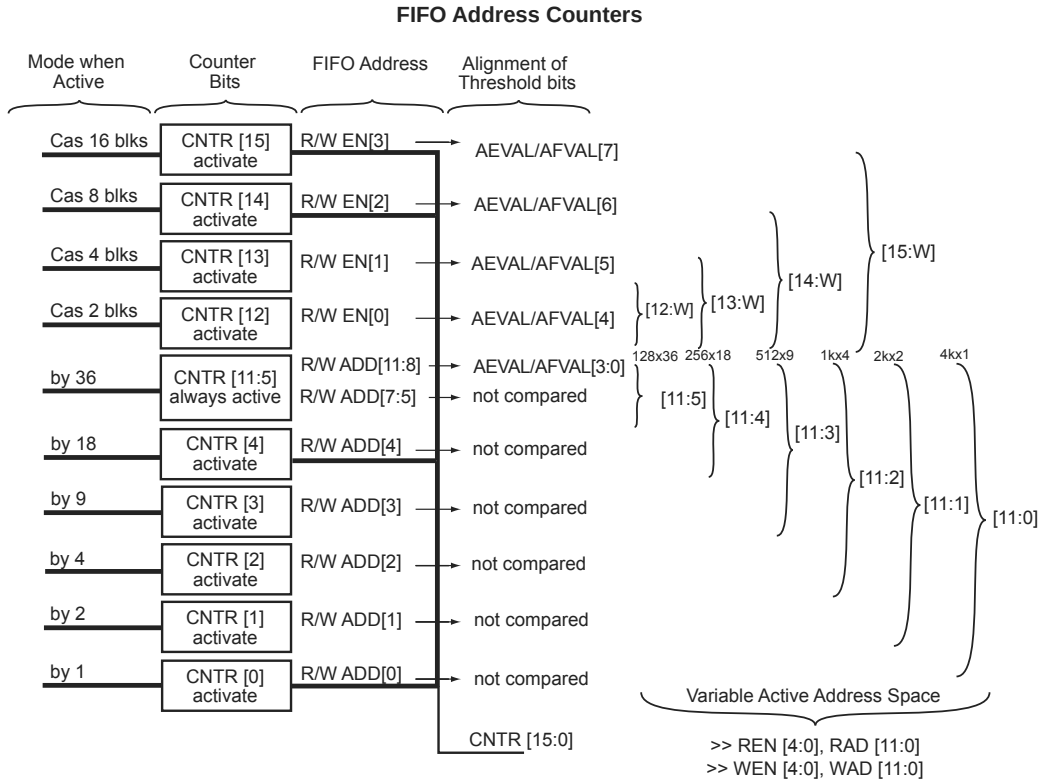
6. *AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.*

## FIFO Flag Logic

The FIFO is user configurable into various DEPTHs and WIDTHs. Figure 2-62 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.




*Note: Inactive counter bits are set to zero.*

***Figure 2-62 •*** **FIFO Address Counters**

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-94).

***Table 2-94 •*** **FIFO Flag Logic**

| Mode | Inactive AEVAL/AFVAL Bits | Inactive DIFF Bits (set to 0) | DIFF Comparison to AFVAL/AEVAL |
|---|---|---|---|
| Non-cascade | [7:4] | [15:12] | DIFF[11:8] withAE/FVAL[3:0] |
| Cascade 2 blocks | [7:5] | [15:13] | DIFF[12:8] withAE/FVAL[4:0] |
| Cascade 4 blocks | [7:6] | [15:14] | DIFF[13:8] withAE/FVAL[5:0] |
| Cascade 8 blocks | [7] | [15] | DIFF[14:8] withAE/FVAL[6:0] |
| Cascade 16 blocks | None | None | DIFF[15:8] withAE/FVAL[7:0] |

***Table 2-98* • One FIFO Block**
**Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, $T_J$ = 70°C**

| | | –2 Speed | | –1 Speed | | Std Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **FIFO Module Timing** | | | | | | | | |
| $t_{WSU}$ | Write Setup | | 11.40 | | 12.98 | | 15.26 | ns |
| $t_{WHD}$ | Write Hold | | 0.22 | | 0.25 | | 0.30 | ns |
| $t_{WCKH}$ | WCLK High | | 0.75 | | 0.75 | | 0.75 | ns |
| $t_{WCKL}$ | WCLK Low | | 0.88 | | 0.88 | | 0.88 | ns |
| $t_{WCKP}$ | Minimum WCLK Period | 1.63 | | 1.63 | | 1.63 | | ns |
| $t_{RSU}$ | Read Setup | | 11.63 | | 13.25 | | 15.58 | ns |
| $t_{RHD}$ | Read Hold | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{RCKH}$ | RCLK High | | 0.77 | | 0.77 | | 0.77 | ns |
| $t_{RCKL}$ | RCLK Low | | 0.93 | | 0.93 | | 0.93 | ns |
| $t_{RCKP}$ | Minimum RCLK period | 1.70 | | 1.70 | | 1.70 | | ns |
| $t_{CLRHF}$ | Clear High | | 0.00 | | 0.00 | | 0.00 | ns |
| $t_{CLR2FF}$ | Clear-to-flag (EMPTY/FULL) | | 1.92 | | 2.18 | | 2.57 | ns |
| $t_{CLR2AF}$ | Clear-to-flag (AEMPTY/AFULL) | | 4.39 | | 5.00 | | 5.88 | ns |
| $t_{CK2FF}$ | Clock-to-flag (EMPTY/FULL) | | 2.13 | | 2.42 | | 2.85 | ns |
| $t_{CK2AF}$ | Clock-to-flag (AEMPTY/AFULL) | | 5.04 | | 5.75 | | 6.75 | ns |
| $t_{RCK2RD1}$ | RCLK-To-OUT (Pipelined) | | 1.32 | | 1.51 | | 1.77 | ns |
| $t_{RCK2RD2}$ | RCLK-To-OUT (Non-Pipelined) | | 2.16 | | 2.46 | | 2.90 | ns |

*Note: Timing data for this single block FIFO has a depth of 4,096. For all other combinations, use Microsemi's timing software.*

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|---|---|
| **AX250 Function** | **Pin Number** |
| **Bank 0** | |
| IO00NB0F0 | D7 |
| IO00PB0F0 | D6 |
| IO01NB0F0 | E7 |
| IO01PB0F0 | E6 |
| IO02NB0F0 | C5 |
| IO02PB0F0 | C4 |
| IO03NB0F0 | C7 |
| IO03PB0F0 | C6 |
| IO04NB0F0 | E9 |
| IO04PB0F0 | E8 |
| IO05NB0F0 | D9 |
| IO05PB0F0 | D8 |
| IO06NB0F0 | B7 |
| IO06PB0F0 | B6 |
| IO07NB0F0 | C9 |
| IO07PB0F0 | C8 |
| IO08NB0F0 | A7 |
| IO08PB0F0 | A6 |
| IO09NB0F0 | B9 |
| IO09PB0F0 | B8 |
| IO10NB0F0 | A9 |
| IO10PB0F0 | A8 |
| IO11NB0F0 | B10 |
| IO11PB0F0 | A10 |
| IO12NB0F0/HCLKAN | E11 |
| IO12PB0F0/HCLKAP | E10 |
| IO13NB0F0/HCLKBN | D12 |
| IO13PB0F0/HCLKBP | D11 |
| **Bank 1** | |
| IO14NB1F1/HCLKCN | F13 |
| IO14PB1F1/HCLKCP | F12 |
| IO15NB1F1/HCLKDN | E14 |
| IO15PB1F1/HCLKDP | E13 |
| IO16NB1F1 | C13 |
| IO16PB1F1 | C12 |

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|---|---|
| **AX250 Function** | **Pin Number** |
| IO17NB1F1 | B14 |
| IO17PB1F1 | B13 |
| IO18NB1F1 | A14 |
| IO18PB1F1 | A13 |
| IO19NB1F1 | A16 |
| IO19PB1F1 | A15 |
| IO20NB1F1 | B16 |
| IO20PB1F1 | B15 |
| IO21NB1F1 | C17 |
| IO21PB1F1 | C16 |
| IO22NB1F1 | F15 |
| IO22PB1F1 | F14 |
| IO23NB1F1 | D16 |
| IO23PB1F1 | D15 |
| IO24NB1F1 | E16 |
| IO24PB1F1 | E15 |
| IO25NB1F1 | F18 |
| IO25PB1F1 | F17 |
| IO26NB1F1 | D18 |
| IO26PB1F1 | E17 |
| IO27NB1F1 | G16 |
| IO27PB1F1 | G15 |
| **Bank 2** | |
| IO28NB2F2 | F19 |
| IO28PB2F2 | E19 |
| IO29NB2F2 | J16 |
| IO29PB2F2 | H16 |
| IO30NB2F2 | E20 |
| IO30PB2F2 | D20 |
| IO31NB2F2 | J17 |
| IO31PB2F2 | H17 |
| IO32NB2F2 | G20 |
| IO32PB2F2 | F20 |
| IO33NB2F2 | H19 |
| IO33PB2F2 | G19 |
| IO34NB2F2 | E22 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| IO34PB2F2 | D22 |
| IO35NB2F2 | J18 |
| IO35PB2F2 | H18 |
| IO36NB2F2 | G21 |
| IO36PB2F2 | F21 |
| IO37NB2F2 | K19 |
| IO37PB2F2 | J19 |
| IO38NB2F2 | J20 |
| IO38PB2F2 | H20 |
| IO39NB2F2 | L16 |
| IO39PB2F2 | K16 |
| IO40NB2F2 | J21 |
| IO40PB2F2 | H21 |
| IO41NB2F2 | L17 |
| IO41PB2F2 | K17 |
| IO42NB2F2 | J22 |
| IO42PB2F2 | H22 |
| IO43NB2F2 | L18 |
| IO43PB2F2 | K18 |
| IO44NB2F2 | L20 |
| IO44PB2F2 | K20 |
| **Bank 3** | |
| IO45NB3F3 | M19 |
| IO45PB3F3 | L19 |
| IO46NB3F3 | M21 |
| IO46PB3F3 | L21 |
| IO47NB3F3 | N17 |
| IO47PB3F3 | M17 |
| IO48NB3F3 | N18 |
| IO48PB3F3 | N19 |
| IO49NB3F3 | N16 |
| IO49PB3F3 | M16 |
| IO50NB3F3 | N20 |
| IO50PB3F3 | M20 |
| IO51NB3F3 | P21 |
| IO51PB3F3 | N21 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| IO52NB3F3 | P18 |
| IO52PB3F3 | P19 |
| IO53NB3F3 | R20 |
| IO53PB3F3 | P20 |
| IO54NB3F3 | T21 |
| IO54PB3F3 | R21 |
| IO55NB3F3 | R17 |
| IO55PB3F3 | P17 |
| IO56NB3F3 | U20 |
| IO56PB3F3 | T20 |
| IO57NB3F3 | T18 |
| IO57PB3F3 | R18 |
| IO58NB3F3 | U19 |
| IO58PB3F3 | T19 |
| IO59NB3F3 | R16 |
| IO59PB3F3 | P16 |
| IO60NB3F3 | W20 |
| IO60PB3F3 | V20 |
| IO61NB3F3 | U18 |
| IO61PB3F3 | V19 |
| **Bank 4** | |
| IO62NB4F4 | T15 |
| IO62PB4F4 | T16 |
| IO63NB4F4 | W17 |
| IO63PB4F4 | V17 |
| IO64NB4F4 | V15 |
| IO64PB4F4 | V16 |
| IO65NB4F4 | Y19 |
| IO65PB4F4 | W18 |
| IO66NB4F4 | AB18 |
| IO66PB4F4 | AB19 |
| IO67NB4F4 | W15 |
| IO67PB4F4 | W16 |
| IO68NB4F4 | U14 |
| IO68PB4F4 | U15 |
| IO69NB4F4 | AA16 |

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|---|---|
| **AX250 Function** | **Pin Number** |
| IO69PB4F4 | AA17 |
| IO70NB4F4 | AB14 |
| IO70PB4F4 | AB15 |
| IO71NB4F4 | Y14 |
| IO71PB4F4 | W14 |
| IO72NB4F4 | AA14 |
| IO72PB4F4 | AA15 |
| IO73NB4F4 | AA13 |
| IO73PB4F4 | AB13 |
| IO74NB4F4/CLKEN | V12 |
| IO74PB4F4/CLKEP | V13 |
| IO75NB4F4/CLKFN | W11 |
| IO75PB4F4/CLKFP | W12 |
| **Bank 5** | |
| IO76NB5F5/CLKGN | U10 |
| IO76PB5F5/CLKGP | U11 |
| IO77NB5F5/CLKHN | V9 |
| IO77PB5F5/CLKHP | V10 |
| IO78NB5F5 | AA9 |
| IO78PB5F5 | AA10 |
| IO79NB5F5 | AB9 |
| IO79PB5F5 | AB10 |
| IO80NB5F5 | AA7 |
| IO80PB5F5 | AA8 |
| IO81NB5F5 | W8 |
| IO81PB5F5 | W9 |
| IO82NB5F5 | AB5 |
| IO82PB5F5 | AB6 |
| IO83NB5F5 | AA5 |
| IO83PB5F5 | AA6 |
| IO84NB5F5 | U8 |
| IO84PB5F5 | U9 |
| IO85NB5F5 | Y6 |
| IO85PB5F5 | Y7 |
| IO86NB5F5 | W6 |
| IO86PB5F5 | W7 |

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|---|---|
| **AX250 Function** | **Pin Number** |
| IO87NB5F5 | Y4 |
| IO87PB5F5 | Y5 |
| IO88NB5F5 | V6 |
| IO88PB5F5 | V7 |
| IO89NB5F5 | T7 |
| IO89PB5F5 | T8 |
| **Bank 6** | |
| IO90NB6F6 | V4 |
| IO90PB6F6 | W5 |
| IO91NB6F6 | P7 |
| IO91PB6F6 | R7 |
| IO92NB6F6 | U5 |
| IO92PB6F6 | T5 |
| IO93NB6F6 | P6 |
| IO93PB6F6 | R6 |
| IO94NB6F6 | T4 |
| IO94PB6F6 | U4 |
| IO95NB6F6 | P5 |
| IO95PB6F6 | R5 |
| IO96NB6F6 | T3 |
| IO96PB6F6 | U3 |
| IO97NB6F6 | P3 |
| IO97PB6F6 | R3 |
| IO98NB6F6 | R2 |
| IO98PB6F6 | T2 |
| IO99NB6F6 | P4 |
| IO99PB6F6 | R4 |
| IO100NB6F6 | P1 |
| IO100PB6F6 | R1 |
| IO101NB6F6 | M7 |
| IO101PB6F6 | N7 |
| IO102NB6F6 | N2 |
| IO102PB6F6 | P2 |
| IO103NB6F6 | M6 |
| IO103PB6F6 | N6 |
| IO104NB6F6 | M4 |

| FG676 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| IO153PB7F14 | M6 |
| IO154NB7F14 | K2 |
| IO154PB7F14 | L2 |
| IO155NB7F14 | K3 |
| IO155PB7F14 | L3 |
| IO156NB7F14 | L5 |
| IO156PB7F14 | L4 |
| IO157NB7F14 | L6 |
| IO157PB7F14 | L7 |
| IO158NB7F15 | J1 |
| IO158PB7F15 | K1 |
| IO159NB7F15 | J4 |
| IO159PB7F15 | K4 |
| IO160NB7F15 | H2 |
| IO160PB7F15 | J2 |
| IO161NB7F15 | K6 |
| IO161PB7F15 | K5 |
| IO162NB7F15 | H3 |
| IO162PB7F15 | J3 |
| IO163NB7F15 | G2 |
| IO163PB7F15 | G1 |
| IO164NB7F15 | G4 |
| IO164PB7F15 | H4 |
| IO165NB7F15 | F3 |
| IO165PB7F15 | G3 |
| IO166NB7F15 | E2 |
| IO166PB7F15 | F2 |
| IO167NB7F15 | F5 |
| IO167PB7F15 | G5 |
| **Dedicated I/O** | |
| GND | A1 |
| GND | A13 |
| GND | A14 |
| GND | A19 |
| GND | A26 |

| FG676 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| GND | A8 |
| GND | AC23 |
| GND | AC4 |
| GND | AD24 |
| GND | AD3 |
| GND | AE2 |
| GND | AE25 |
| GND | AF1 |
| GND | AF13 |
| GND | AF14 |
| GND | AF19 |
| GND | AF26 |
| GND | AF8 |
| GND | B2 |
| GND | B25 |
| GND | B26 |
| GND | C24 |
| GND | C3 |
| GND | G20 |
| GND | G7 |
| GND | H1 |
| GND | H19 |
| GND | H26 |
| GND | H8 |
| GND | J18 |
| GND | J9 |
| GND | K10 |
| GND | K11 |
| GND | K12 |
| GND | K13 |
| GND | K14 |
| GND | K15 |
| GND | K16 |
| GND | K17 |
| GND | L10 |

| FG676 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| GND | L11 |
| GND | L12 |
| GND | L13 |
| GND | L14 |
| GND | L15 |
| GND | L16 |
| GND | L17 |
| GND | M10 |
| GND | M11 |
| GND | M12 |
| GND | M13 |
| GND | M14 |
| GND | M15 |
| GND | M16 |
| GND | M17 |
| GND | N1 |
| GND | N10 |
| GND | N11 |
| GND | N12 |
| GND | N13 |
| GND | N14 |
| GND | N15 |
| GND | N16 |
| GND | N17 |
| GND | N26 |
| GND | P1 |
| GND | P10 |
| GND | P11 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | P15 |
| GND | P16 |
| GND | P17 |
| GND | P26 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| IO259NB6F24 | AF7 |
| IO259PB6F24 | AG7 |
| IO260NB6F24 | AH3 |
| IO260PB6F24 | AH4 |
| IO261NB6F24 | AH5 |
| IO261PB6F24 | AJ5 |
| IO262NB6F24 | AE6 |
| IO262PB6F24 | AF6 |
| IO263NB6F24 | AF5 |
| IO263PB6F24 | AG5 |
| IO264NB6F24 | AD8 |
| IO264PB6F24 | AE8 |
| IO265NB6F24 | AF3 |
| IO265PB6F24 | AG3 |
| IO266NB6F24 | AC10 |
| IO266PB6F24 | AD10 |
| IO267NB6F25 | AD7 |
| IO267PB6F25 | AE7 |
| IO268NB6F25 | AD5 |
| IO268PB6F25 | AE5 |
| IO269NB6F25 | AE4 |
| IO269PB6F25 | AF4 |
| IO270NB6F25 | AB9 |
| IO270PB6F25 | AC9 |
| IO271NB6F25 | AC6 |
| IO271PB6F25 | AD6 |
| IO272NB6F25 | AB8 |
| IO272PB6F25 | AC8 |
| IO273NB6F25 | AE1 |
| IO273PB6F25 | AE2 |
| IO274NB6F25 | AA10 |
| IO274PB6F25 | AB10 |
| IO275NB6F25 | AB7 |
| IO275PB6F25 | AC7 |
| IO276NB6F25 | AD1 |

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|---|---|
| AX2000 Function | Pin Number |
| IO276PB6F25 | AD2 |
| IO277NB6F25 | AC4 |
| IO277PB6F25 | AC3 |
| IO278NB6F26 | AA8 |
| IO278PB6F26 | AA9 |
| IO279NB6F26 | AB5 |
| IO279PB6F26 | AB6 |
| IO280NB6F26 | Y10 |
| IO280PB6F26 | Y11 |
| IO281NB6F26 | AB3 |
| IO281PB6F26 | AB4 |
| IO282NB6F26 | Y7 |
| IO282PB6F26 | AA7 |
| IO283NB6F26 | AC2 |
| IO283PB6F26 | AC1 |
| IO284NB6F26 | Y9 |
| IO284PB6F26 | Y8 |
| IO285NB6F26 | AA5 |
| IO285PB6F26 | AA6 |
| IO286NB6F26 | W10 |
| IO286PB6F26 | W11 |
| IO287NB6F26 | AA3 |
| IO287PB6F26 | AA4 |
| IO288NB6F26 | W9 |
| IO288PB6F26 | W8 |
| IO289NB6F27 | AA1 |
| IO289PB6F27 | AA2 |
| IO290NB6F27 | W6 |
| IO290PB6F27 | Y6 |
| IO291NB6F27 | W5 |
| IO291PB6F27 | Y5 |
| IO292NB6F27 | V7 |
| IO292PB6F27 | W7 |
| IO293NB6F27 | W4 |
| IO293PB6F27 | Y4 |

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|---|---|
| AX2000 Function | Pin Number |
| IO294NB6F27 | V10 |
| IO294PB6F27 | V11 |
| IO295NB6F27 | Y1 |
| IO295PB6F27 | Y2 |
| IO296NB6F27 | W1 |
| IO296PB6F27 | W2 |
| IO297NB6F27 | V1 |
| IO297PB6F27 | V2 |
| IO298NB6F27 | V9 |
| IO298PB6F27 | V8 |
| IO299NB6F27 | U4 |
| IO299PB6F27 | V4 |
| **Bank 7** | |
| IO300NB7F28 | U10 |
| IO300PB7F28 | U11 |
| IO301NB7F28 | U2 |
| IO301PB7F28 | U1 |
| IO302NB7F28 | U6 |
| IO302PB7F28 | U7 |
| IO303NB7F28 | T3 |
| IO303PB7F28 | U3 |
| IO304NB7F28 | U9 |
| IO304PB7F28 | U8 |
| IO305NB7F28 | R2 |
| IO305PB7F28 | R1 |
| IO306NB7F28 | R4 |
| IO306PB7F28 | T4 |
| IO307NB7F28 | R5 |
| IO307PB7F28 | T5 |
| IO308NB7F28 | T11 |
| IO308PB7F28 | T10 |
| IO309NB7F28 | T6 |
| IO309PB7F28 | T7 |
| IO310NB7F29 | T9 |
| IO310PB7F29 | T8 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | AK12 |
| GND | AK17 |
| GND | AK18 |
| GND | AK23 |
| GND | AK30 |
| GND | AK5 |
| GND | AL1 |
| GND | AL11 |
| GND | AL2 |
| GND | AL24 |
| GND | AL3 |
| GND | AL31 |
| GND | AL32 |
| GND | AL33 |
| GND | AL34 |
| GND | AL4 |
| GND | AM1 |
| GND | AM10 |
| GND | AM15 |
| GND | AM2 |
| GND | AM20 |
| GND | AM25 |
| GND | AM3 |
| GND | AM31 |
| GND | AM32 |
| GND | AM33 |
| GND | AM34 |
| GND | AM4 |
| GND | AN1 |
| GND | AN2 |
| GND | AN26 |
| GND | AN3 |
| GND | AN31 |
| GND | AN32 |
| GND | AN33 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | AN34 |
| GND | AN4 |
| GND | AN9 |
| GND | AP13 |
| GND | AP2 |
| GND | AP22 |
| GND | AP27 |
| GND | AP3 |
| GND | AP31 |
| GND | AP32 |
| GND | AP33 |
| GND | AP4 |
| GND | AP8 |
| GND | B1 |
| GND | B2 |
| GND | B26 |
| GND | B3 |
| GND | B31 |
| GND | B32 |
| GND | B33 |
| GND | B34 |
| GND | B4 |
| GND | B9 |
| GND | C1 |
| GND | C10 |
| GND | C15 |
| GND | C2 |
| GND | C20 |
| GND | C25 |
| GND | C3 |
| GND | C31 |
| GND | C32 |
| GND | C33 |
| GND | C34 |
| GND | C4 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| GND | D1 |
| GND | D11 |
| GND | D2 |
| GND | D24 |
| GND | D3 |
| GND | D31 |
| GND | D32 |
| GND | D33 |
| GND | D34 |
| GND | D4 |
| GND | E12 |
| GND | E17 |
| GND | E18 |
| GND | E23 |
| GND | E30 |
| GND | E5 |
| GND | F29 |
| GND | F30 |
| GND | F6 |
| GND | G28 |
| GND | G7 |
| GND | H1 |
| GND | H34 |
| GND | J2 |
| GND | J33 |
| GND | K3 |
| GND | K32 |
| GND | L11 |
| GND | L24 |
| GND | L31 |
| GND | L4 |
| GND | M12 |
| GND | M23 |
| GND | M30 |
| GND | M5 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| NC | AP9 |
| NC | B17 |
| NC | B22 |
| NC | B27 |
| NC | B8 |
| NC | D10 |
| NC | D20 |
| NC | D23 |
| NC | D25 |
| NC | F3 |
| NC | F32 |
| NC | F33 |
| NC | F34 |
| NC | F4 |
| NC | G1 |
| NC | G32 |
| NC | G33 |
| NC | G34 |
| NC | H31 |
| NC | H33 |
| NC | J1 |
| NC | J3 |
| NC | J34 |
| NC | M1 |
| NC | M4 |
| NC | P1 |
| NC | P2 |
| NC | R31 |
| NC | T1 |
| NC | T2 |
| NC | V3 |
| NC | V34 |
| NC | W3 |
| NC | W34 |
| PRA | J17 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| PRB | F18 |
| PRC | AD18 |
| PRD | AH18 |
| TCK | J9 |
| TDI | F7 |
| TDO | L10 |
| TMS | H8 |
| TRST | E6 |
| VCCA | AA13 |
| VCCA | AA22 |
| VCCA | AB14 |
| VCCA | AB15 |
| VCCA | AB16 |
| VCCA | AB17 |
| VCCA | AB18 |
| VCCA | AB19 |
| VCCA | AB20 |
| VCCA | AB21 |
| VCCA | AF8 |
| VCCA | AK28 |
| VCCA | G30 |
| VCCA | G5 |
| VCCA | N14 |
| VCCA | N15 |
| VCCA | N16 |
| VCCA | N17 |
| VCCA | N18 |
| VCCA | N19 |
| VCCA | N20 |
| VCCA | N21 |
| VCCA | P13 |
| VCCA | P22 |
| VCCA | R13 |
| VCCA | R22 |
| VCCA | T13 |

| FG1152 | |
|---|---|
| AX2000 Function | Pin Number |
| VCCA | T22 |
| VCCA | U13 |
| VCCA | U22 |
| VCCA | V13 |
| VCCA | V22 |
| VCCA | W13 |
| VCCA | W22 |
| VCCA | Y13 |
| VCCA | Y22 |
| VCCDA | AF26 |
| VCCDA | AF9 |
| VCCDA | AG17 |
| VCCDA | AG18 |
| VCCDA | AH14 |
| VCCDA | AH15 |
| VCCDA | AH17 |
| VCCDA | AH20 |
| VCCDA | AH21 |
| VCCDA | AK29 |
| VCCDA | AK6 |
| VCCDA | E15 |
| VCCDA | E29 |
| VCCDA | E7 |
| VCCDA | F15 |
| VCCDA | F21 |
| VCCDA | F5 |
| VCCDA | G20 |
| VCCDA | H17 |
| VCCDA | H18 |
| VCCDA | H28 |
| VCCDA | J18 |
| VCCDA | V27 |
| VCCDA | V6 |
| VCCIB0 | A5 |
| VCCIB0 | B5 |

| PQ208 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| IO150PB7F14 | 19 |
| IO152NB7F14 | 16 |
| IO152PB7F14 | 17 |
| IO161NB7F15 | 12 |
| IO161PB7F15 | 13 |
| IO163NB7F15 | 10 |
| IO163PB7F15 | 11 |
| IO165PB7F15 | 7 |
| IO166NB7F15 | 5 |
| IO166PB7F15 | 6 |
| IO167NB7F15 | 3 |
| IO167PB7F15 | 4 |
| **Dedicated I/O** | |
| $V_{CCDA}$ | 1 |
| $V_{CCDA}$ | 26 |
| $V_{CCDA}$ | 53 |
| $V_{CCDA}$ | 63 |
| $V_{CCDA}$ | 78 |
| $V_{CCDA}$ | 95 |
| $V_{CCDA}$ | 105 |
| $V_{CCDA}$ | 130 |
| $V_{CCDA}$ | 157 |
| $V_{CCDA}$ | 167 |
| $V_{CCDA}$ | 182 |
| $V_{CCDA}$ | 202 |
| GND | 104 |
| GND | 9 |
| GND | 15 |
| GND | 21 |
| GND | 32 |
| GND | 39 |
| GND | 46 |
| GND | 51 |
| GND | 59 |
| GND | 65 |
| GND | 69 |
| GND | 90 |

| PQ208 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| GND | 94 |
| GND | 99 |
| GND | 113 |
| GND | 119 |
| GND | 125 |
| GND | 143 |
| GND | 136 |
| GND | 150 |
| GND | 155 |
| GND | 164 |
| GND | 169 |
| GND | 173 |
| GND | 194 |
| GND | 196 |
| GND | 201 |
| GND/LP | 208 |
| PRA | 184 |
| PRB | 183 |
| PRC | 80 |
| PRD | 79 |
| TCK | 205 |
| TDI | 204 |
| TDO | 203 |
| TMS | 206 |
| TRST | 207 |
| VCCA | 2 |
| VCCA | 14 |
| VCCA | 38 |
| VCCA | 52 |
| VCCA | 64 |
| VCCA | 93 |
| VCCA | 118 |
| VCCA | 142 |
| VCCA | 156 |
| VCCA | 168 |
| VCCA | 195 |
| VCCPLA | 189 |

| PQ208 | |
|---|---|
| **AX500 Function** | **Pin Number** |
| VCCPLB | 187 |
| VCCPLC | 178 |
| VCCPLD | 176 |
| VCCPLE | 85 |
| VCCPLF | 83 |
| VCCPLG | 74 |
| VCCPLH | 72 |
| VCCIB0 | 200 |
| VCCIB0 | 193 |
| VCCIB1 | 172 |
| VCCIB1 | 163 |
| VCCIB2 | 149 |
| VCCIB2 | 135 |
| VCCIB3 | 124 |
| VCCIB3 | 112 |
| VCCIB4 | 98 |
| VCCIB4 | 89 |
| VCCIB5 | 68 |
| VCCIB5 | 58 |
| VCCIB6 | 45 |
| VCCIB6 | 31 |
| VCCIB7 | 20 |
| VCCIB7 | 8 |
| VCOMPLA | 190 |
| VCOMPLB | 188 |
| VCOMPLC | 179 |
| VCOMPLD | 177 |
| VCOMPLE | 86 |
| VCOMPLF | 84 |
| VCOMPLG | 75 |
| VCOMPLH | 73 |
| VPUMP | 158 |

| CQ352 | |
|---|---|
| AX250 Function | Pin Number |
| GND | 21 |
| GND | 27 |
| GND | 33 |
| GND | 39 |
| GND | 45 |
| GND | 51 |
| GND | 57 |
| GND | 63 |
| GND | 69 |
| GND | 75 |
| GND | 81 |
| GND | 88 |
| GND | 89 |
| GND | 97 |
| GND | 103 |
| GND | 109 |
| GND | 115 |
| GND | 121 |
| GND | 133 |
| GND | 145 |
| GND | 151 |
| GND | 157 |
| GND | 163 |
| GND | 169 |
| GND | 176 |
| GND | 177 |
| GND | 186 |
| GND | 192 |
| GND | 198 |
| GND | 204 |
| GND | 210 |
| GND | 216 |
| GND | 222 |
| GND | 228 |
| GND | 234 |

| CQ352 | |
|---|---|
| AX250 Function | Pin Number |
| GND | 240 |
| GND | 246 |
| GND | 252 |
| GND | 258 |
| GND | 264 |
| GND | 265 |
| GND | 274 |
| GND | 280 |
| GND | 286 |
| GND | 292 |
| GND | 298 |
| GND | 310 |
| GND | 322 |
| GND | 330 |
| GND | 334 |
| GND | 340 |
| GND | 345 |
| GND | 352 |
| NC | 91 |
| NC | 117 |
| NC | 130 |
| NC | 131 |
| NC | 148 |
| NC | 174 |
| NC | 268 |
| NC | 294 |
| NC | 307 |
| NC | 308 |
| NC | 327 |
| NC | 328 |
| PRA | 312 |
| PRB | 311 |
| PRC | 135 |
| PRD | 134 |
| TCK | 349 |

| CQ352 | |
|---|---|
| AX250 Function | Pin Number |
| TDI | 348 |
| TDO | 347 |
| TMS | 350 |
| TRST | 351 |
| VCCA | 3 |
| VCCA | 14 |
| VCCA | 32 |
| VCCA | 56 |
| VCCA | 74 |
| VCCA | 87 |
| VCCA | 102 |
| VCCA | 114 |
| VCCA | 150 |
| VCCA | 162 |
| VCCA | 175 |
| VCCA | 191 |
| VCCA | 209 |
| VCCA | 233 |
| VCCA | 251 |
| VCCA | 263 |
| VCCA | 279 |
| VCCA | 291 |
| VCCA | 329 |
| VCCA | 339 |
| VCCDA | 2 |
| VCCDA | 44 |
| VCCDA | 90 |
| VCCDA | 116 |
| VCCDA | 132 |
| VCCDA | 149 |
| VCCDA | 178 |
| VCCDA | 221 |
| VCCDA | 266 |
| VCCDA | 293 |
| VCCDA | 309 |

| CQ352 | |
|---|---|
| AX500 Function | Pin Number |
| GND | 21 |
| GND | 27 |
| GND | 33 |
| GND | 39 |
| GND | 45 |
| GND | 51 |
| GND | 57 |
| GND | 63 |
| GND | 69 |
| GND | 75 |
| GND | 81 |
| GND | 88 |
| GND | 89 |
| GND | 97 |
| GND | 103 |
| GND | 109 |
| GND | 115 |
| GND | 121 |
| GND | 133 |
| GND | 145 |
| GND | 151 |
| GND | 157 |
| GND | 163 |
| GND | 169 |
| GND | 176 |
| GND | 177 |
| GND | 186 |
| GND | 192 |
| GND | 198 |
| GND | 204 |
| GND | 210 |
| GND | 216 |
| GND | 222 |
| GND | 228 |
| GND | 234 |

| CQ352 | |
|---|---|
| AX500 Function | Pin Number |
| GND | 240 |
| GND | 246 |
| GND | 252 |
| GND | 258 |
| GND | 264 |
| GND | 265 |
| GND | 274 |
| GND | 280 |
| GND | 286 |
| GND | 292 |
| GND | 298 |
| GND | 310 |
| GND | 322 |
| GND | 330 |
| GND | 334 |
| GND | 340 |
| GND | 345 |
| GND/LP | 352 |
| NC | 91 |
| NC | 117 |
| NC | 130 |
| NC | 131 |
| NC | 148 |
| NC | 174 |
| NC | 268 |
| NC | 294 |
| NC | 307 |
| NC | 308 |
| NC | 327 |
| NC | 328 |
| PRA | 312 |
| PRB | 311 |
| PRC | 135 |
| PRD | 134 |
| TCK | 349 |

| CQ352 | |
|---|---|
| AX500 Function | Pin Number |
| TDI | 348 |
| TDO | 347 |
| TMS | 350 |
| TRST | 351 |
| VCCA | 3 |
| VCCA | 14 |
| VCCA | 32 |
| VCCA | 56 |
| VCCA | 74 |
| VCCA | 87 |
| VCCA | 102 |
| VCCA | 114 |
| VCCA | 150 |
| VCCA | 162 |
| VCCA | 175 |
| VCCA | 191 |
| VCCA | 209 |
| VCCA | 233 |
| VCCA | 251 |
| VCCA | 263 |
| VCCA | 279 |
| VCCA | 291 |
| VCCA | 329 |
| VCCA | 339 |
| VCCDA | 2 |
| VCCDA | 44 |
| VCCDA | 90 |
| VCCDA | 116 |
| VCCDA | 132 |
| VCCDA | 149 |
| VCCDA | 178 |
| VCCDA | 221 |
| VCCDA | 266 |
| VCCDA | 293 |
| VCCDA | 309 |

# Datasheet Categories

## Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Axcelerator Family Device Status" table on page iii, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### *Product Brief*

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### *Advance*

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### *Preliminary*

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### *Production*

This version contains information that is considered to be final.

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