Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	248
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-fgg484

Design Environment

The Axcelerator family of FPGAs is fully supported by both Microsemi's Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE Flow* diagram located on the Microsemi SoC Products Group website). Libero IDE includes Synplify® Actel Edition (AE) from Synplicity®, ViewDraw® AE from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, and Designer software from Microsemi.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor which support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Microsemi's back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Programming support is provided through Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. In addition, BP Microsystems offers multi-site programmers that provide qualified support for Microsemi devices. Factory programming is available for high-volume production needs.

In-System Diagnostic and Debug Capabilities

The Axcelerator family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation (Figure 1-9).

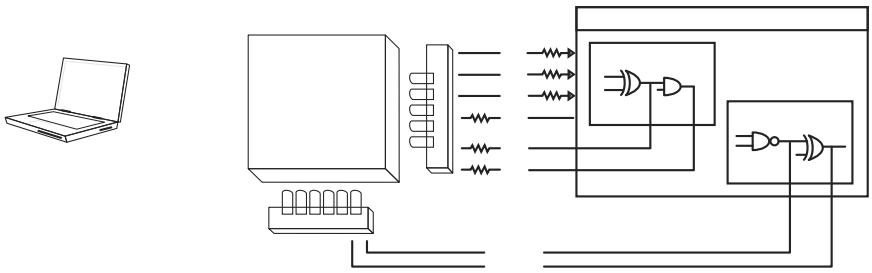


Figure 1-9 • **Probe Setup**

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 4 (24mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		2.99		3.41		4.01	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.49		2.51		2.51	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.59		2.95		3.46	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.91		1.93		1.93	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.56		4.06		4.77	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

2.5 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

***Table 2-23* • DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
-0.3	0.7	1.7	3.6	0.4	2.0	12	–12

AC Loadings

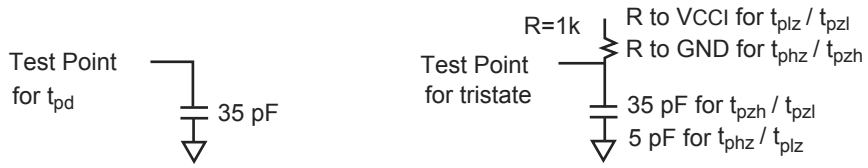


***Figure 2-16* • AC Test Loads**

***Table 2-24* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
0	2.5	1.25	N/A	35

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-35* • 3.3 V PCI I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V PCI Output Module Timing								
t_{DP}	Input Buffer		1.57		1.79		2.10	ns
t_{PY}	Output Buffer		1.91		2.18		2.56	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-40* • 3.3 V GTL+ I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V GTL+I/O Module Timing								
t_{DP}	Input Buffer		1.71		1.95		2.29	ns
t_{PY}	Output Buffer		1.13		1.29		1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-38).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-39).

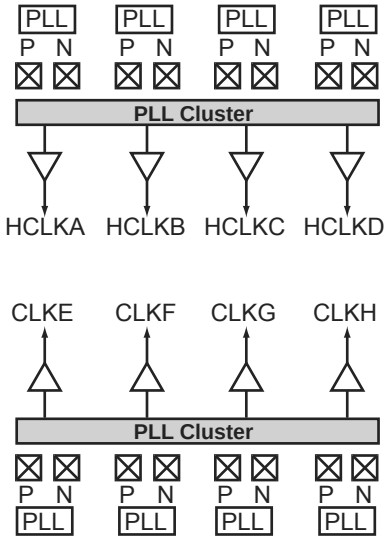


Figure 2-38 • **PLL Group**

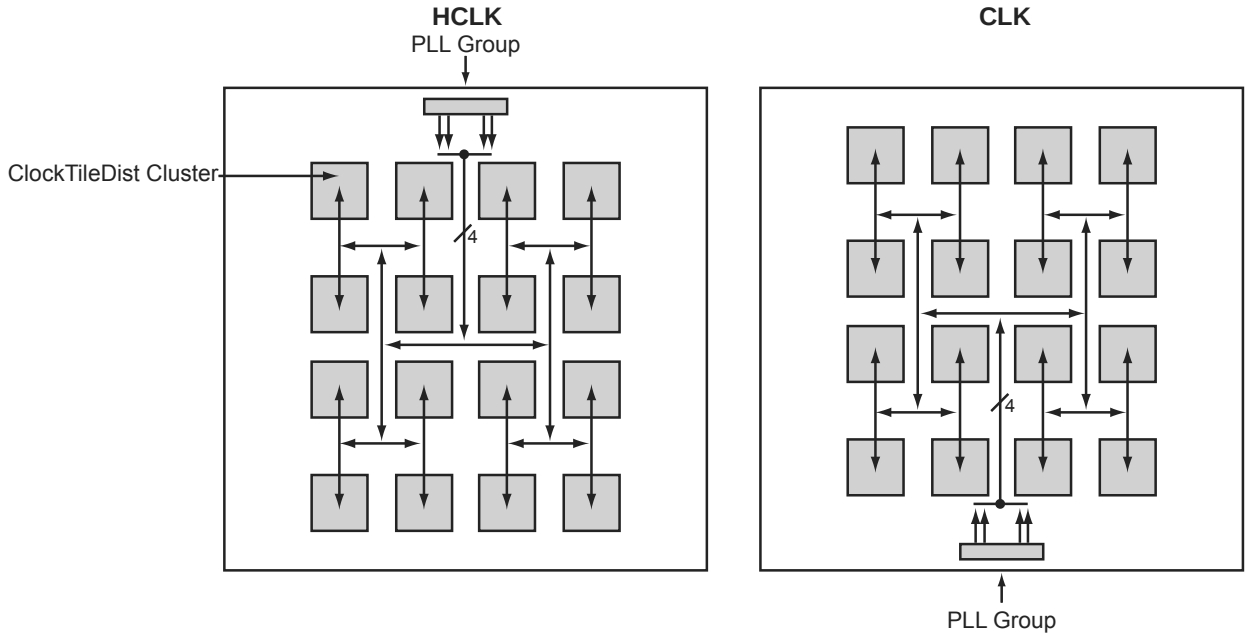


Figure 2-39 • **Example of HCLK and CLK Distributions on the AX2000**

PLL Configurations

The following rules apply to the different PLL inputs and outputs:

Reference Clock

The RefCLK can be driven by (Figure 2-50):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. CLK1 output of an adjacent PLL
3. [H]CLKxP (single-ended or voltage-referenced)
4. [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Feedback Clock

The feedback clock can be driven by (Figure 2-51 on page 2-78):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
3. An internal signal from the PLL block

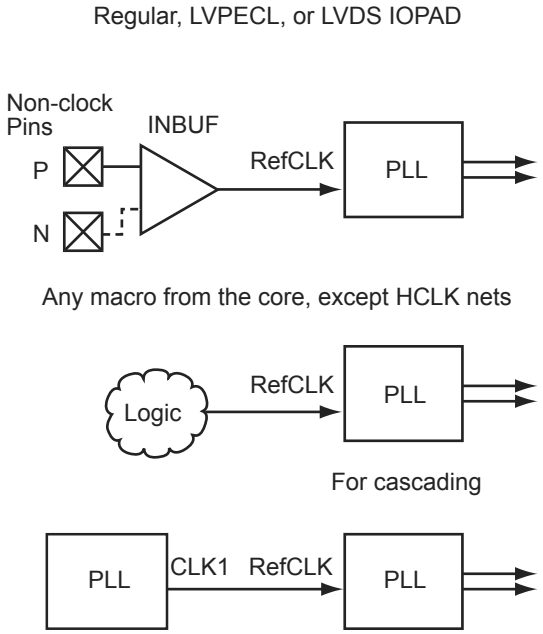


Figure 2-50 • **Reference Clock Connections**

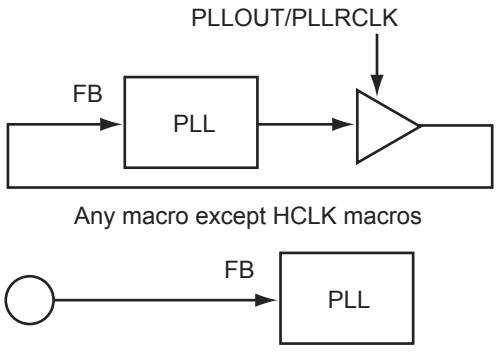


Figure 2-51 • **Feedback Clock Connections**

Programming

Device programming is supported through the Silicon Sculptor II, a single-site, robust and compact device programmer for the PC. Up to four Silicon Sculptor IIs can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor II to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor II also provides a self-test to test its own hardware extensively.

Programming an Axcelerator device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

1. Load the *.AFM file.
2. Select the device to be programmed.
3. Begin programming.

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via our In-House Programming Center.

In addition, BP Microsystems offers multi-site programmers that provide qualified support for Axcelerator devices.

For more details on programming the Axcelerator devices, please refer to the *Silicon Sculptor II User's Guide*.

BG729	
AX1000 Function	**Pin Number**
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16

BG729	
AX1000 Function	**Pin Number**
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

FG256-Pin FBGA	
AX125 Function	**Pin Number**
Bank 6	
IO60NB6F6	L4
IO60PB6F6	M4
IO61NB6F6	L3
IO61PB6F6	M3
IO63NB6F6	P2
IO63PB6F6	N2
IO64NB6F6	J4
IO64PB6F6	K4
IO65NB6F6	N1
IO65PB6F6	P1
IO67NB6F6	L2
IO67PB6F6	M2
IO69NB6F6	L1
IO69PB6F6	M1
IO70NB6F6	J3
IO70PB6F6	K3
IO71NB6F6	J2
IO71PB6F6	K2
Bank 7	
IO72NB7F7	J1
IO72PB7F7	K1
IO73NB7F7	G2
IO73PB7F7	H2
IO74NB7F7	G3
IO74PB7F7	H3
IO75NB7F7	E1
IO75PB7F7	F1
IO76NB7F7	G1
IO77NB7F7	E2
IO77PB7F7	F2
IO78NB7F7	G4
IO78PB7F7	H4
IO79NB7F7	C1
IO79PB7F7	D1

FG256-Pin FBGA	
AX125 Function	**Pin Number**
IO81NB7F7	C2
IO81PB7F7	B1
IO82NB7F7	D2
IO82PB7F7	D3
IO83NB7F7	E3
IO83PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6

FG256-Pin FBGA	
AX125 Function	**Pin Number**
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
NC	A11
NC	R11
NC	R5
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6

FG256	
AX250 Function	Pin Number
Bank 0	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO05NB0F0	B6
IO05PB0F0	B5
IO07NB0F0	A6
IO07PB0F0	A5
IO12NB0F0/HCLKAN	B8
IO12PB0F0/HCLKAP	B7
IO13NB0F0/HCLKBN	A9
IO13PB0F0/HCLKBP	A8
Bank 1	
IO14NB1F1/HCLKCN	C10
IO14PB1F1/HCLKCP	C9
IO15NB1F1/HCLKDN	B11
IO15PB1F1/HCLKDP	B10
IO17NB1F1	A13
IO17PB1F1	A12
IO19NB1F1	B13
IO19PB1F1	B12
IO21NB1F1	C12
IO21PB1F1	C11
IO23NB1F1	A15
IO23PB1F1	B14
IO26NB1F1	C15
IO26PB1F1	C14
IO27NB1F1	D13
IO27PB1F1	D12
Bank 2	
IO29NB2F2	F13
IO29PB2F2	E13
IO30NB2F2	F14
IO30PB2F2	E14

FG256	
AX250 Function	Pin Number
IO32NB2F2	C16
IO32PB2F2	B16
IO33NB2F2	F15
IO33PB2F2	E15
IO35NB2F2	H13
IO35PB2F2	G13
IO36NB2F2	E16
IO36PB2F2	D16
IO38NB2F2	H15
IO38PB2F2	G15
IO39NB2F2	H14
IO39PB2F2	G14
IO40NB2F2	G16
IO40PB2F2	F16
IO43NB2F2	K15
IO43PB2F2	K16
IO44NB2F2	J16
IO44PB2F2	H16
Bank 3	
IO45NB3F3	K13
IO45PB3F3	J13
IO46NB3F3	K14
IO46PB3F3	J14
IO52NB3F3	L15
IO52PB3F3	L16
IO54NB3F3	P16
IO54PB3F3	N16
IO55PB3F3	M16
IO56NB3F3	P15
IO56PB3F3	R16
IO58NB3F3	N15
IO58PB3F3	M15
IO59NB3F3	M13
IO59PB3F3	L13
IO61NB3F3	M14

FG256	
AX250 Function	Pin Number
IO61PB3F3	L14
Bank 4	
IO62NB4F4	N12
IO62PB4F4	N13
IO63NB4F4	T14
IO63PB4F4	R14
IO66PB4F4	T15
IO67NB4F4	R12
IO67PB4F4	R13
IO69NB4F4	P11
IO69PB4F4	P12
IO70PB4F4	T11
IO73NB4F4	T12
IO73PB4F4	T13
IO74NB4F4/CLKEN	R9
IO74PB4F4/CLKEP	R10
IO75NB4F4/CLKFN	T8
IO75PB4F4/CLKFP	T9
Bank 5	
IO76NB5F5/CLKGN	P7
IO76PB5F5/CLKGP	P8
IO77NB5F5/CLKHN	R6
IO77PB5F5/CLKHP	R7
IO79NB5F5	T5
IO79PB5F5	T6
IO81NB5F5	P5
IO81PB5F5	P6
IO83NB5F5	T3
IO83PB5F5	T4
IO85NB5F5	R3
IO85PB5F5	R4
IO88NB5F5	R1
IO88PB5F5	T2
IO89NB5F5	N4
IO89PB5F5	N5

FG324	
AX125 Function	Pin Number
Bank 0	
IO00NB0F0	C5
IO00PB0F0	C4
IO01NB0F0	A3
IO01PB0F0	A2
IO02NB0F0	C7
IO02PB0F0	C6
IO03NB0F0	B5
IO03PB0F0	B4
IO04NB0F0	A5
IO04PB0F0	A4
IO05NB0F0	A7
IO05PB0F0	A6
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0/HCLKAN	C9
IO07PB0F0/HCLKAP	C8
IO08NB0F0/HCLKBN	B10
IO08PB0F0/HCLKBP	B9
Bank 1	
IO09NB1F1/HCLKCN	D11
IO09PB1F1/HCLKCP	D10
IO10NB1F1/HCLKDN	C12
IO10PB1F1/HCLKDP	C11
IO11NB1F1	A15
IO11PB1F1	A14
IO12NB1F1	B14
IO12PB1F1	B13
IO13NB1F1	A17
IO13PB1F1	A16
IO14NB1F1	D13
IO14PB1F1	D12
IO15NB1F1	C14
IO15PB1F1	C13
IO16NB1F1	B16

FG324	
AX125 Function	Pin Number
IO16PB1F1	C15
IO17NB1F1	E14
IO17PB1F1	E13
Bank 2	
IO18NB2F2	G14
IO18PB2F2	F14
IO19NB2F2	D16
IO19PB2F2	D15
IO20NB2F2	C18
IO20PB2F2	B18
IO21NB2F2	D17
IO21PB2F2	C17
IO22NB2F2	F17
IO22PB2F2	E17
IO23NB2F2	G16
IO23PB2F2	F16
IO24NB2F2	E18
IO24PB2F2	D18
IO25NB2F2	G18
IO25PB2F2	F18
IO26NB2F2	H17
IO26PB2F2	G17
IO27NB2F2	J16
IO27PB2F2	H16
IO28NB2F2	J18
IO28PB2F2	H18
IO29NB2F2	K17
IO29PB2F2	J17
Bank 3	
IO30NB3F3	N18
IO30PB3F3	M18
IO31NB3F3	L18
IO31PB3F3	K18
IO32NB3F3	L16
IO32PB3F3	L17

FG324	
AX125 Function	Pin Number
IO33NB3F3	R18
IO33PB3F3	P18
IO34NB3F3	N15
IO34PB3F3	M15
IO35NB3F3	M16
IO35PB3F3	M17
IO36NB3F3	P16
IO36PB3F3	N16
IO37NB3F3	R17
IO37PB3F3	P17
IO38NB3F3	N14
IO38PB3F3	M14
IO39NB3F3	U18
IO39PB3F3	T18
IO40NB3F3	R16
IO40PB3F3	T17
IO41NB3F3	P13
IO41PB3F3	P14
Bank 4	
IO42NB4F4	T13
IO42PB4F4	T14
IO43NB4F4	U15
IO43PB4F4	T15
IO44NB4F4	U13
IO44PB4F4	U14
IO45NB4F4	V15
IO45PB4F4	V16
IO46NB4F4	V13
IO46PB4F4	V14
IO47NB4F4	V12
IO47PB4F4	U12
IO48NB4F4	V10
IO48PB4F4	V11
IO49NB4F4/CLKEN	T10
IO49PB4F4/CLKEP	T11

FG324	
AX125 Function	**Pin Number**
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG484	
AX500 Function	**Pin Number**
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX500 Function	**Pin Number**
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX500 Function	**Pin Number**
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG676	
AX1000 Function	**Pin Number**
IO197PB6F18	Y6
IO198NB6F18	AD1
IO198PB6F18	AE1
IO199NB6F18	AA2
IO199PB6F18	AB2
IO200NB6F18	Y3
IO200PB6F18	AA3
IO201NB6F18	V5
IO201PB6F18	W5
IO202NB6F18	AB1
IO202PB6F18	AC1
IO203NB6F19	V4
IO203PB6F19	W4
IO204NB6F19	V3
IO204PB6F19	W3
IO205NB6F19	U6
IO205PB6F19	V6
IO206NB6F19	W2
IO206PB6F19	Y2
IO207NB6F19	U4
IO207PB6F19	U5
IO208NB6F19	Y1
IO208PB6F19	AA1
IO209NB6F19	T6
IO209PB6F19	T7
IO211NB6F19	T3
IO211PB6F19	U3
IO212NB6F19	V1
IO212PB6F19	V2
IO213NB6F19	T5
IO213PB6F19	T4
IO214NB6F20	U1
IO214PB6F20	U2
IO215NB6F20	R6
IO215PB6F20	R7
IO217NB6F20	R5

FG676	
AX1000 Function	**Pin Number**
IO217PB6F20	R4
IO218NB6F20	R2
IO218PB6F20	T2
IO219NB6F20	P3
IO219PB6F20	R3
IO220NB6F20	R1
IO220PB6F20	T1
IO221NB6F20	P6
IO221PB6F20	P7
IO223NB6F20	P5
IO223PB6F20	P4
Bank 7	
IO225NB7F21	N5
IO225PB7F21	N4
IO226NB7F21	N2
IO226PB7F21	N3
IO227NB7F21	N6
IO227PB7F21	N7
IO229NB7F21	M7
IO229PB7F21	M6
IO231NB7F21	M5
IO231PB7F21	M4
IO232NB7F21	L1
IO232PB7F21	M1
IO233NB7F21	M2
IO233PB7F21	M3
IO235NB7F21	K2
IO235PB7F21	L2
IO236NB7F22	L5
IO236PB7F22	L4
IO237NB7F22	L6
IO237PB7F22	L7
IO238NB7F22	K3
IO238PB7F22	L3
IO240NB7F22	J1
IO240PB7F22	K1

FG676	
AX1000 Function	**Pin Number**
IO241NB7F22	K6
IO241PB7F22	K5
IO242NB7F22	H2
IO242PB7F22	J2
IO243NB7F22	J4
IO243PB7F22	K4
IO244NB7F22	H3
IO244PB7F22	J3
IO245NB7F22	G2
IO245PB7F22	G1
IO247NB7F23	J6
IO247PB7F23	J5
IO248NB7F23	E1
IO248PB7F23	F1
IO249NB7F23	E2
IO249PB7F23	F2
IO250NB7F23	G4
IO250PB7F23	H4
IO251NB7F23	F3
IO251PB7F23	G3
IO253NB7F23	H6
IO253PB7F23	H5
IO254NB7F23	D2
IO254PB7F23	D1
IO255NB7F23	E4
IO255PB7F23	F4
IO256NB7F23	D3
IO256PB7F23	E3
IO257NB7F23	F5
IO257PB7F23	G5
Dedicated I/O	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26

FG676	
AX1000 Function	**Pin Number**
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12

FG676	
AX1000 Function	**Pin Number**
VCOMPLH	Y13
VPUMP	E22

CQ352	
AX500 Function	Pin Number
Bank 0	
IO00PB0F0	343
IO03NB0F0	341
IO03PB0F0	342
IO05NB0F0	337
IO05PB0F0	338
IO07NB0F0	335
IO07PB0F0	336
IO09NB0F0	331
IO09PB0F0	332
IO15NB0F1	325
IO15PB0F1	326
IO17NB0F1	323
IO17PB0F1	324
IO19NB0F1/HCLKAN	319
IO19PB0F1/HCLKAP	320
IO20NB0F1/HCLKBN	313
IO20PB0F1/HCLKBP	314
Bank 1	
IO21NB1F2/HCLKCN	305
IO21PB1F2/HCLKCP	306
IO22NB1F2/HCLKDN	299
IO22PB1F2/HCLKDP	300
IO23NB1F2	289
IO23PB1F2	290
IO24NB1F2	295
IO24PB1F2	296
IO25NB1F2	287
IO25PB1F2	288
IO27NB1F2	283
IO27PB1F2	284
IO29NB1F2	281
IO29PB1F2	282
IO31NB1F2	277
IO31PB1F2	278

CQ352	
AX500 Function	Pin Number
IO35NB1F3	275
IO35PB1F3	276
IO37NB1F3	271
IO37PB1F3	272
IO41NB1F3	269
IO41PB1F3	270
Bank 2	
IO43NB2F4	261
IO43PB2F4	262
IO45NB2F4	259
IO45PB2F4	260
IO47NB2F4	255
IO47PB2F4	256
IO49NB2F4	253
IO49PB2F4	254
IO50NB2F4	247
IO50PB2F4	248
IO51NB2F4	249
IO51PB2F4	250
IO53NB2F5	243
IO53PB2F5	244
IO54NB2F5	241
IO54PB2F5	242
IO55NB2F5	237
IO55PB2F5	238
IO57NB2F5	235
IO57PB2F5	236
IO58NB2F5	231
IO58PB2F5	232
IO59NB2F5	229
IO59PB2F5	230
IO61NB2F5	225
IO61PB2F5	226
IO62NB2F5	223
IO62PB2F5	224

CQ352	
AX500 Function	Pin Number
Bank 3	
IO63NB3F6	217
IO63PB3F6	218
IO64NB3F6	219
IO64PB3F6	220
IO65NB3F6	213
IO65PB3F6	214
IO67NB3F6	207
IO67PB3F6	208
IO68NB3F6	211
IO68PB3F6	212
IO69NB3F6	205
IO69PB3F6	206
IO71NB3F6	201
IO71PB3F6	202
IO73NB3F6	199
IO73PB3F6	200
IO75NB3F7	193
IO75PB3F7	194
IO76NB3F7	195
IO76PB3F7	196
IO77NB3F7	189
IO77PB3F7	190
IO79NB3F7	187
IO79PB3F7	188
IO80NB3F7	183
IO80PB3F7	184
IO81NB3F7	181
IO81PB3F7	182
IO83NB3F7	179
IO83PB3F7	180
Bank 4	
IO85NB4F8	172
IO85PB4F8	173
IO87NB4F8	170

CQ352	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282

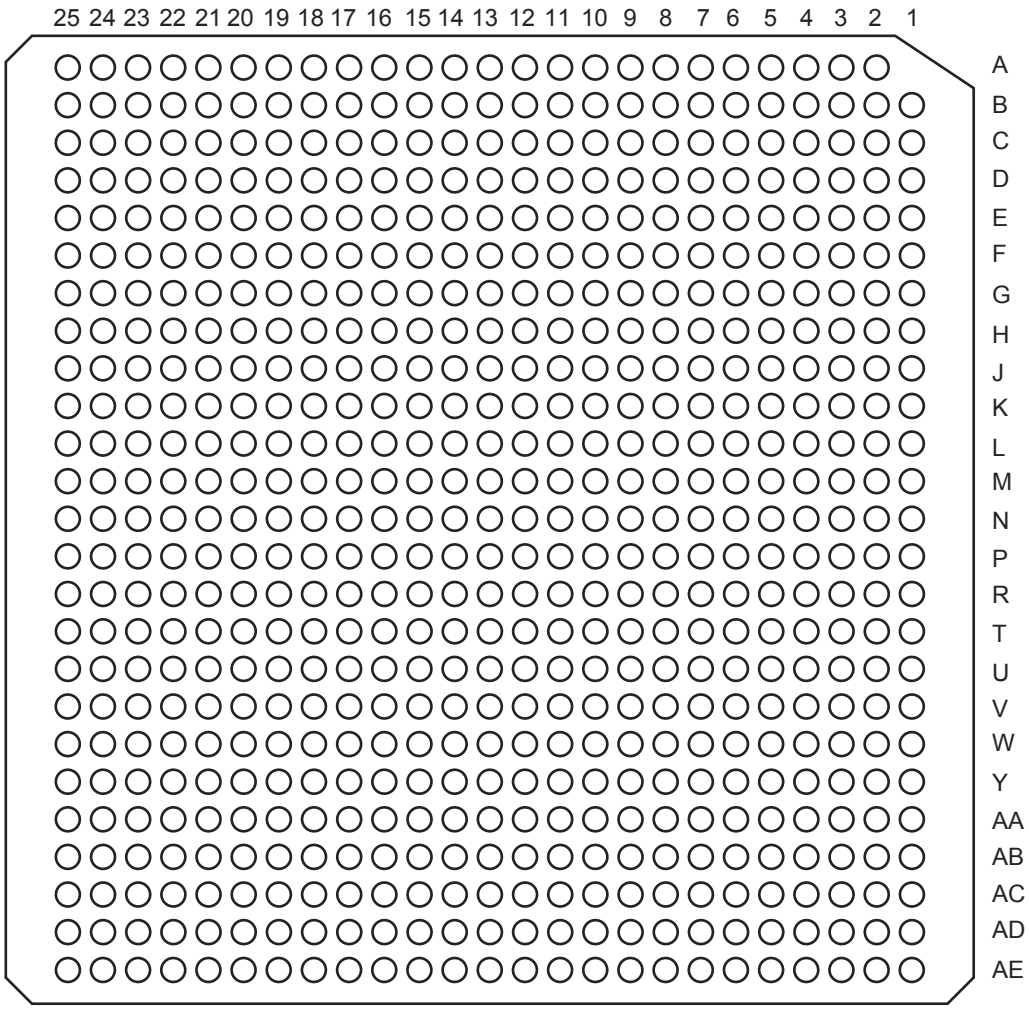
CQ352	
AX2000 Function	Pin Number
IO71NB1F6	277
IO71PB1F6	278
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224

CQ352	
AX2000 Function	Pin Number
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170

CQ352	
AX2000 Function	**Pin Number**
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX2000 Function	**Pin Number**
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.