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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	115
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax250-pq208m

Two C-cells, a single R-cell, two Transmit (TX), and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

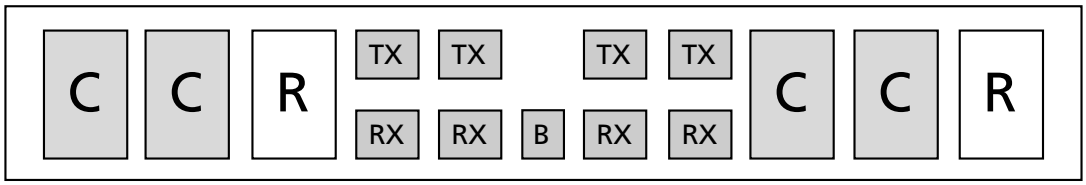


Figure 1-4 • **AX SuperCluster**

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

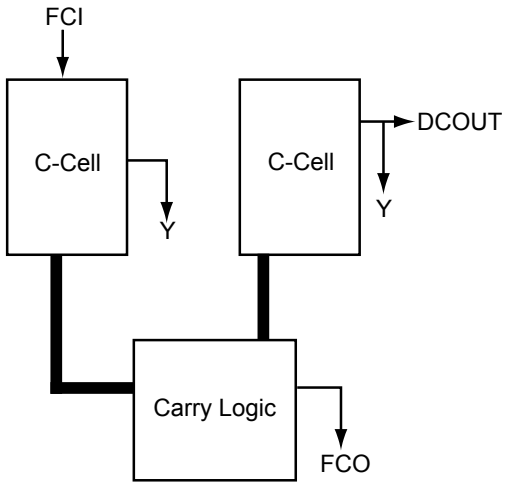


Figure 1-5 • **AX 2-Bit Carry Logic**

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the AX1000 is composed of a 3x3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1). Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the AX250).

Table 1-1 • **Number of Core Tiles per Device**

Device	Number of Core Tiles
AX125	1 regular tile
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

Calculating Power Dissipation

Table 2-3 • **Standby Current**

Device	Temperature	ICCA	ICCDA	ICCBANK		ICCPLL	ICCCP[1]		IIH, IIL, IOZ[2]	Units
		Standby Current (Core)	Standby Current, Differential I/O	Standby Current per I/O Bank		Standby Current per PLL	Standby Current, Charge Pump			
				2.5 V VCCI	3.3 V VCCI		Active	Bypassed Mode		
AX125	Typical at 25°C	1.5	1.5	0.2	0.3	0.2	0.3	0.01	±0.01	mA
	70°C	15	6	0.5	0.75	1	0.4	0.01	±0.01	mA
	85°C	25	6	0.6	0.8	1	0.4	0.2	±0.01	mA
	125°C	50	8	1	1.5	2	0.4	0.5	±0.01	mA
AX250	Typical at 25°C	1.5	1.4	0.25	0.4	0.2	0.3	0.01	±0.01	mA
	70°C	30	7	0.8	0.9	1	0.4	0.01	±0.01	mA
	85°C	40	7	0.8	1	1	0.4	0.2	±0.01	mA
	125°C	70	9	1.3	1.8	2	0.4	0.5	±0.01	mA
AX500	Typical at 25°C	5	1.4	0.4	0.75	0.2	0.3	0.01	±0.01	mA
	70°C	60	7	1	1.5	1	0.4	0.01	±0.01	mA
	85°C	80	7	1	1.9	1	0.4	0.2	±0.01	mA
	125°C	180	9	1.75	2.5	1.5	0.4	0.5	±0.01	mA
AX1000	Typical at 25°C	7.5	1.5	0.5	1.25	0.2	0.3	0.01	±0.01	mA
	70°C	80	8	1.5	3	1	0.4	0.01	±0.01	mA
	85°C	120	8	1.5	3.4	1	0.4	0.2	±0.01	mA
	125°C	200	10	3	4	1.5	0.4	0.5	±0.01	mA
AX2000	Typical at 25°C	20	1.6	0.7	1.5	0.2	0.3	0.01	±0.01	mA
	70°C	160	10	2	7	1	0.4	0.01	±0.01	mA
	85°C	200	10	3	8	1	0.4	0.2	±0.01	mA
	125°C	500	15	4	10	1.5	0.4	0.5	±0.01	mA

Notes:

1. *ICCCP Active is the ICCDA or the Internal Charge Pump current. ICCCP Bypassed mode is the External Charge Pump current IIH (VPUMP pin).*
2. *IIH, IIL, or IOZ values are measured with inputs at the same level as VCCI for IIH and GND for IIL and IOZ.*

5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

EQ 3

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

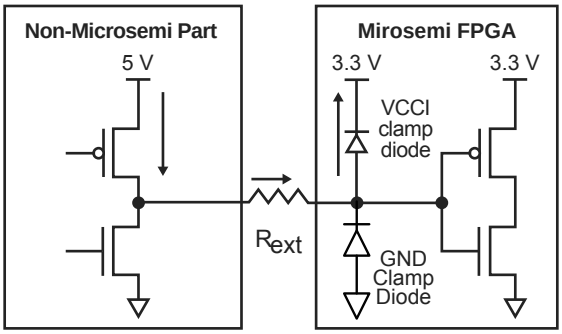


Figure 2-3 • **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

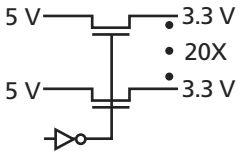


Figure 2-4 • **Bus Switch IDTQS32X2384**

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

3. The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.

Timing Characteristics

***Table 2-28* • 1.8V LVCMOS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.7 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVCMOS18 Output Module Timing								
t_{DP}	Input Buffer		3.26		3.71		4.37	ns
t_{PY}	Output Buffer		4.55		5.18		6.09	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.82		2.83		2.84	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.43		3.45		3.46	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.01		6.85		8.05	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.73		7.67		9.01	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

***Table 2-35* • 3.3 V PCI I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V PCI Output Module Timing								
t_{DP}	Input Buffer		1.57		1.79		2.10	ns
t_{PY}	Output Buffer		1.91		2.18		2.56	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Class II

Table 2-53 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16

AC Loadings

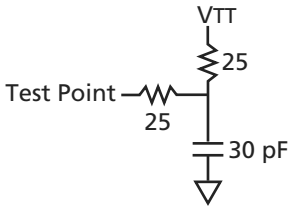


Figure 2-24 • AC Test Loads

Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

*Note: * Measuring Point = VTRIP*

Timing Characteristics

Table 2-55 • 3.3 V SSTL3 Class II I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V SSTL3 Class II I/O Module Timing								
t_{DP}	Input Buffer		1.85		2.10		2.47	ns
t_{PY}	Output Buffer		2.17		2.47		2.91	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-57* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.2 – 0.125	1.2 + 0.125	1.2

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-58* • LVDS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVDS Output Module Timing								
t_{DP}	Input Buffer		1.80		2.05		2.41	ns
t_{PY}	Output Buffer		2.32		2.64		3.11	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-37 on page 2-62). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 2-37). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

Figure 2-36 • **FastConnect Routing**

Figure 2-37 • **Horizontal and Vertical Tracks**

***Table 2-83* • South PLL Connections**

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).

***Table 2-93* • Sixteen RAM Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		16.54		18.84		22.15	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	13.40		13.40		13.40		ns
t_{WCKP}	WCLK Minimum Period	14.15		14.15		14.15		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		18.13		20.65		24.27	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		18.13		20.65		24.27	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		12.83		14.62		17.18	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	14.41		14.41		14.41		ns
t_{RCKP}	RCLK Minimum Period	15.14		15.14		15.14		ns

Note: Timing data for these sixteen cascaded RAM blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

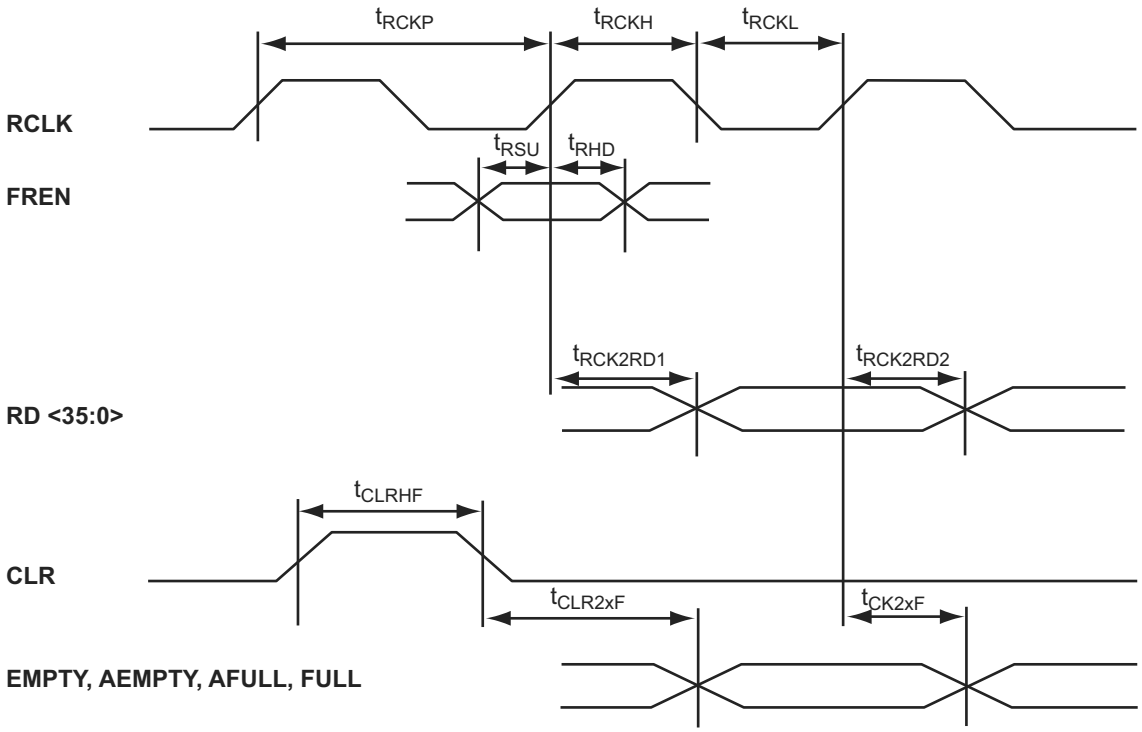
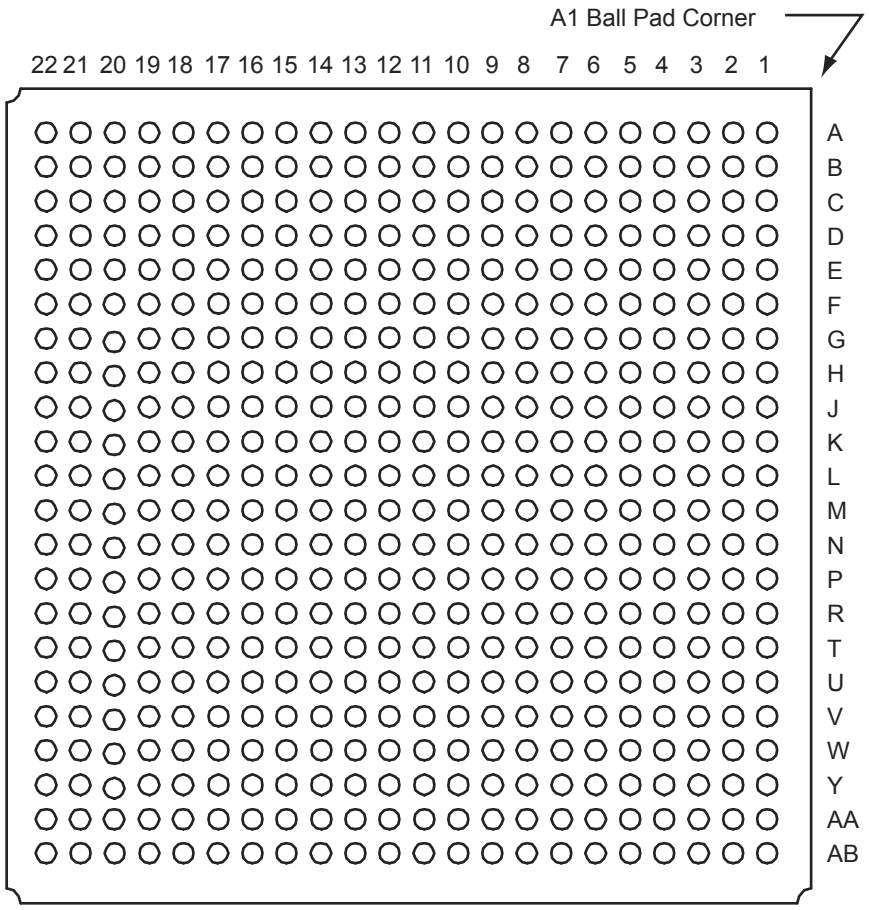


Figure 2-68 • **FIFO Read Timing**

FG484



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG484	
AX250 Function	**Pin Number**
Bank 0	
IO00NB0F0	D7
IO00PB0F0	D6
IO01NB0F0	E7
IO01PB0F0	E6
IO02NB0F0	C5
IO02PB0F0	C4
IO03NB0F0	C7
IO03PB0F0	C6
IO04NB0F0	E9
IO04PB0F0	E8
IO05NB0F0	D9
IO05PB0F0	D8
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0	C9
IO07PB0F0	C8
IO08NB0F0	A7
IO08PB0F0	A6
IO09NB0F0	B9
IO09PB0F0	B8
IO10NB0F0	A9
IO10PB0F0	A8
IO11NB0F0	B10
IO11PB0F0	A10
IO12NB0F0/HCLKAN	E11
IO12PB0F0/HCLKAP	E10
IO13NB0F0/HCLKBN	D12
IO13PB0F0/HCLKBP	D11
Bank 1	
IO14NB1F1/HCLKCN	F13
IO14PB1F1/HCLKCP	F12
IO15NB1F1/HCLKDN	E14
IO15PB1F1/HCLKDP	E13
IO16NB1F1	C13
IO16PB1F1	C12

FG484	
AX250 Function	**Pin Number**
IO17NB1F1	B14
IO17PB1F1	B13
IO18NB1F1	A14
IO18PB1F1	A13
IO19NB1F1	A16
IO19PB1F1	A15
IO20NB1F1	B16
IO20PB1F1	B15
IO21NB1F1	C17
IO21PB1F1	C16
IO22NB1F1	F15
IO22PB1F1	F14
IO23NB1F1	D16
IO23PB1F1	D15
IO24NB1F1	E16
IO24PB1F1	E15
IO25NB1F1	F18
IO25PB1F1	F17
IO26NB1F1	D18
IO26PB1F1	E17
IO27NB1F1	G16
IO27PB1F1	G15
Bank 2	
IO28NB2F2	F19
IO28PB2F2	E19
IO29NB2F2	J16
IO29PB2F2	H16
IO30NB2F2	E20
IO30PB2F2	D20
IO31NB2F2	J17
IO31PB2F2	H17
IO32NB2F2	G20
IO32PB2F2	F20
IO33NB2F2	H19
IO33PB2F2	G19
IO34NB2F2	E22

FG484	
AX250 Function	**Pin Number**
IO34PB2F2	D22
IO35NB2F2	J18
IO35PB2F2	H18
IO36NB2F2	G21
IO36PB2F2	F21
IO37NB2F2	K19
IO37PB2F2	J19
IO38NB2F2	J20
IO38PB2F2	H20
IO39NB2F2	L16
IO39PB2F2	K16
IO40NB2F2	J21
IO40PB2F2	H21
IO41NB2F2	L17
IO41PB2F2	K17
IO42NB2F2	J22
IO42PB2F2	H22
IO43NB2F2	L18
IO43PB2F2	K18
IO44NB2F2	L20
IO44PB2F2	K20
Bank 3	
IO45NB3F3	M19
IO45PB3F3	L19
IO46NB3F3	M21
IO46PB3F3	L21
IO47NB3F3	N17
IO47PB3F3	M17
IO48NB3F3	N18
IO48PB3F3	N19
IO49NB3F3	N16
IO49PB3F3	M16
IO50NB3F3	N20
IO50PB3F3	M20
IO51NB3F3	P21
IO51PB3F3	N21

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG896	
AX1000 Function	Pin Number
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

FG896	
AX1000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX1000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG1152	
AX2000 Function	Pin Number
GND	AK12
GND	AK17
GND	AK18
GND	AK23
GND	AK30
GND	AK5
GND	AL1
GND	AL11
GND	AL2
GND	AL24
GND	AL3
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL4
GND	AM1
GND	AM10
GND	AM15
GND	AM2
GND	AM20
GND	AM25
GND	AM3
GND	AM31
GND	AM32
GND	AM33
GND	AM34
GND	AM4
GND	AN1
GND	AN2
GND	AN26
GND	AN3
GND	AN31
GND	AN32
GND	AN33

FG1152	
AX2000 Function	Pin Number
GND	AN34
GND	AN4
GND	AN9
GND	AP13
GND	AP2
GND	AP22
GND	AP27
GND	AP3
GND	AP31
GND	AP32
GND	AP33
GND	AP4
GND	AP8
GND	B1
GND	B2
GND	B26
GND	B3
GND	B31
GND	B32
GND	B33
GND	B34
GND	B4
GND	B9
GND	C1
GND	C10
GND	C15
GND	C2
GND	C20
GND	C25
GND	C3
GND	C31
GND	C32
GND	C33
GND	C34
GND	C4

FG1152	
AX2000 Function	Pin Number
GND	D1
GND	D11
GND	D2
GND	D24
GND	D3
GND	D31
GND	D32
GND	D33
GND	D34
GND	D4
GND	E12
GND	E17
GND	E18
GND	E23
GND	E30
GND	E5
GND	F29
GND	F30
GND	F6
GND	G28
GND	G7
GND	H1
GND	H34
GND	J2
GND	J33
GND	K3
GND	K32
GND	L11
GND	L24
GND	L31
GND	L4
GND	M12
GND	M23
GND	M30
GND	M5

CQ352	
AX500 Function	Pin Number
IO87PB4F8	171
IO89NB4F8	166
IO89PB4F8	167
IO94NB4F9	164
IO94PB4F9	165
IO95NB4F9	160
IO95PB4F9	161
IO97NB4F9	158
IO97PB4F9	159
IO99NB4F9	154
IO99PB4F9	155
IO100NB4F9	146
IO100PB4F9	147
IO101NB4F9	152
IO101PB4F9	153
IO103NB4F9/CLKEN	142
IO103PB4F9/CLKEP	143
IO104NB4F9/CLKFN	136
IO104PB4F9/CLKFP	137
Bank 5	
IO105NB5F10/CLKGN	128
IO105PB5F10/CLKGP	129
IO106NB5F10/CLKHN	122
IO106PB5F10/CLKHP	123
IO107NB5F10	118
IO107PB5F10	119
IO114NB5F11	112
IO114PB5F11	113
IO115NB5F11	110
IO115PB5F11	111
IO116NB5F11	106
IO116PB5F11	107
IO117NB5F11	104
IO117PB5F11	105
IO119NB5F11	100

CQ352	
AX500 Function	Pin Number
IO119PB5F11	101
IO121NB5F11	98
IO121PB5F11	99
IO123NB5F11	94
IO123PB5F11	95
IO125NB5F11	92
IO125PB5F11	93
Bank 6	
IO126PB6F12	86
IO127NB6F12	84
IO127PB6F12	85
IO129NB6F12	82
IO129PB6F12	83
IO131NB6F12	78
IO131PB6F12	79
IO133NB6F12	76
IO133PB6F12	77
IO134NB6F12	72
IO134PB6F12	73
IO135NB6F12	70
IO135PB6F12	71
IO137NB6F13	66
IO137PB6F13	67
IO138NB6F13	64
IO138PB6F13	65
IO139NB6F13	60
IO139PB6F13	61
IO141NB6F13	54
IO141PB6F13	55
IO142NB6F13	58
IO142PB6F13	59
IO143NB6F13	52
IO143PB6F13	53
IO145NB6F13	48
IO145PB6F13	49

CQ352	
AX500 Function	Pin Number
IO146NB6F13	46
IO146PB6F13	47
Bank 7	
IO147NB7F14	40
IO147PB7F14	41
IO148NB7F14	42
IO148PB7F14	43
IO149NB7F14	36
IO149PB7F14	37
IO151NB7F14	30
IO151PB7F14	31
IO152NB7F14	34
IO152PB7F14	35
IO153NB7F14	28
IO153PB7F14	29
IO155NB7F14	24
IO155PB7F14	25
IO157NB7F14	22
IO157PB7F14	23
IO159NB7F15	16
IO159PB7F15	17
IO160NB7F15	18
IO160PB7F15	19
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165NB7F15	6
IO165PB7F15	7
IO167NB7F15	4
IO167PB7F15	5
Dedicated I/O	
GND	1
GND	9
GND	15

CQ352	
AX1000 Function	Pin Number
IO131PB4F12	171
IO132NB4F12	166
IO132PB4F12	167
IO133NB4F12	164
IO133PB4F12	165
IO134NB4F12	160
IO134PB4F12	161
IO136NB4F12	158
IO136PB4F12	159
IO137NB4F12	154
IO137PB4F12	155
IO138NB4F12	152
IO138PB4F12	153
IO153NB4F14	146
IO153PB4F14	147
IO159NB4F14/CLKEN	142
IO159PB4F14/CLKEP	143
IO160NB4F14/CLKFN	136
IO160PB4F14/CLKFP	137
Bank 5	
IO161NB5F15/CLKGN	128
IO161PB5F15/CLKGP	129
IO162NB5F15/CLKHN	122
IO162PB5F15/CLKHP	123
IO167NB5F15	118
IO167PB5F15	119
IO183NB5F17	110
IO183PB5F17	111
IO184NB5F17	112
IO184PB5F17	113
IO185NB5F17	104
IO185PB5F17	105
IO186NB5F17	106
IO186PB5F17	107
IO187NB5F17	98

CQ352	
AX1000 Function	Pin Number
IO187PB5F17	99
IO188NB5F17	100
IO188PB5F17	101
IO190NB5F17	94
IO190PB5F17	95
IO192NB5F17	92
IO192PB5F17	93
Bank 6	
IO193PB6F18	86
IO194NB6F18	84
IO194PB6F18	85
IO196NB6F18	78
IO196PB6F18	79
IO197NB6F18	82
IO197PB6F18	83
IO198NB6F18	76
IO198PB6F18	77
IO203NB6F19	72
IO203PB6F19	73
IO204NB6F19	70
IO204PB6F19	71
IO205NB6F19	66
IO205PB6F19	67
IO206NB6F19	64
IO206PB6F19	65
IO207NB6F19	60
IO207PB6F19	61
IO208NB6F19	58
IO208PB6F19	59
IO211NB6F19	54
IO211PB6F19	55
IO212NB6F19	52
IO212PB6F19	53
IO223NB6F20	48
IO223PB6F20	49

CQ352	
AX1000 Function	Pin Number
IO224NB6F20	46
IO224PB6F20	47
Bank 7	
IO225NB7F21	40
IO225PB7F21	41
IO226NB7F21	42
IO226PB7F21	43
IO237NB7F22	34
IO237PB7F22	35
IO238NB7F22	36
IO238PB7F22	37
IO240NB7F22	30
IO240PB7F22	31
IO241NB7F22	28
IO241PB7F22	29
IO242NB7F22	24
IO242PB7F22	25
IO244NB7F22	22
IO244PB7F22	23
IO245NB7F22	18
IO245PB7F22	19
IO246NB7F22	16
IO246PB7F22	17
IO249NB7F23	12
IO249PB7F23	13
IO250NB7F23	10
IO250PB7F23	11
IO256NB7F23	4
IO256PB7F23	5
IO257NB7F23	6
IO257PB7F23	7
Dedicated I/O	
GND	1
GND	9
GND	15

CQ352	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282

CQ352	
AX2000 Function	Pin Number
IO71NB1F6	277
IO71PB1F6	278
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224

CQ352	
AX2000 Function	Pin Number
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170

Revision	Changes	Page
Revision 12 (v2.4)	Revised ordering information and timing data to reflect phase out of –3 speed grade options.	
	Table 2-3 was updated.	2
Revision 11 (v2.3)	The "Packaging Data" section is new.	iv
	Table 2-2 was updated.	2-1
	"VCCDA Supply Voltage" was updated.	2-9
	"PRA/B/C/D Probe A, B, C and D" was updated.	2-10
	The "User I/Os" was updated.	2-11
Revision 10 (v2.2)	Figure 1-3 was updated.	1-2
	Table 2-2 was updated.	2-1
	The "Power-Up/Down Sequence" section was updated.	2-1
	Table 2-4 was updated.	2-3
	Table 2-5 was updated.	2-4
	The "Timing Characteristics" section was added.	2-7
	Table 2-7 was updated.	2-7
	Figure 2-1 was updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) equations in the "Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) in the "Routed Clock – Using LVTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The "Global Pins" section was updated.	2-10
	The "User I/Os" section was updated.	2-11
	Table 2-17 was updated.	2-19
	Figure 2-8 was updated.	2-20
	Figure 2-13 and Figure 2-14 were updated.	2-24
	The following timing parameters were renamed in I/O timing characteristic tables from Table 2-22 to Table 2-60: $t_{IOCLKQ} > t_{ICLKQ}$ $t_{IOCLKY} > t_{OCLKQ}$	2-26 to 2-52
	Timing numbers were updated from Table 2-22 to Table 2-78.	2-26 to 2-69
	The "R-Cell" section was updated.	2-58
	Figure 2-59 was updated.	2-89
	Figure 2-60 was updated.	2-89
	Figure 2-67 was updated.	2-100
	Figure 2-68 was updated.	2-101
	Table 2-89 to Table 2-93 were updated.	2-90 to 2-94
	Table 2-98 to Table 2-102 were updated.	2-102 to 2-106