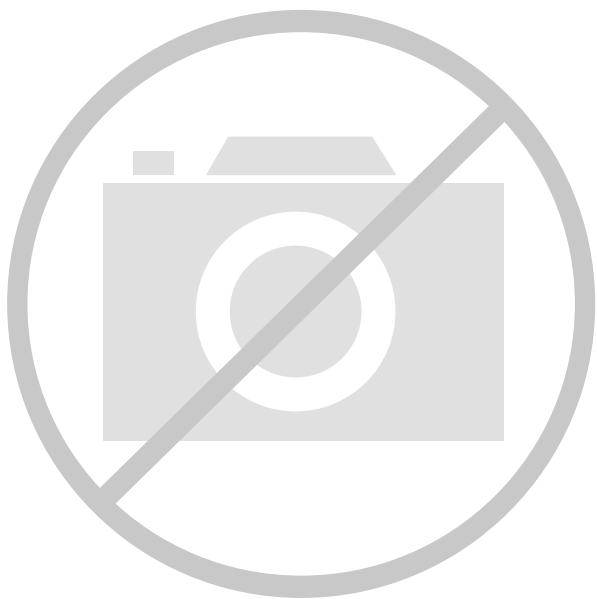




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

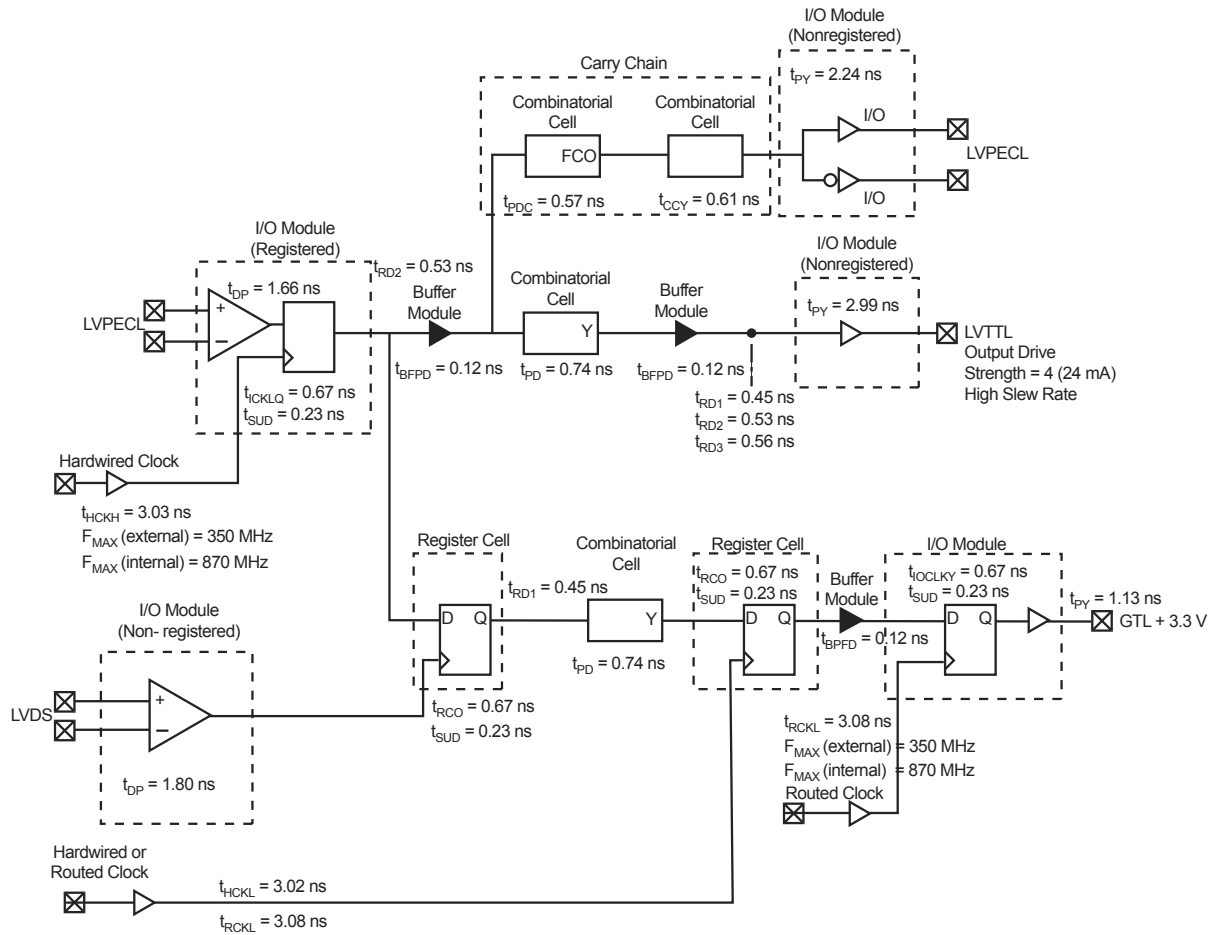
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4224
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	115
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ax250-pqg208i

Timing Model



Note: Worst case timing data for the AX1000, -2 speed grade

Figure 2-1 • Worst Case Timing Data

Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$$= (t_{DP} + t_{RD2} + t_{SUD}) - t_{HCKH}$$

$$= (1.72 + 0.53 + 0.23) - 3.02 = -0.54 \text{ ns}$$

Clock-to-Out (Pad-to-Pad)

$$= t_{HCKL} + t_{RCO} + t_{RD1} + t_{PY}$$

$$= 3.02 + 0.67 + 0.45 + 2.99 = 7.13 \text{ ns}$$

Routed Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$$= (t_{DP} + t_{RD2} + t_{SUD}) - t_{RCKH}$$

$$= (1.72 + 0.53 + 0.23) - 3.13 = -0.65 \text{ ns}$$

Clock-to-Out (Pad-to-Pad)

$$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$$

$$= 3.13 + 0.67 + 0.45 + 3.03 = 7.24 \text{ ns}$$

User I/Os²

Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-8 on page 2-12 contains the I/O standards supported by the Axcelerator family, and Table 2-10 on page 2-12 compares the features of the different I/O standards.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (Figure 2-6 on page 2-18). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules:

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.
- Dedicated I/O pins such as GND and VCCI are counted as part of the 16.
- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.
- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3 V.

A user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.
- Use generic I/O macros and then use Designer's PinEditor to specify the desired I/O standards (please note that this is not applicable to differential standards).
- A combination of the first two methods.

Refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

2. Do not use an external resistor to pull the I/O above V_{CCI} for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above V_{CCI} .

Table 2-13 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank.

Table 2-13 • Legal I/O Usage Matrix

I/O Standard	LVTTTL 3.3 V	LVC MOS 2.5 V	LVC MOS 1.8 V	LVC MOS 1.5 V (JESD8-11)	3.3V PCI/PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	HSTL Class I (1.5V)	SSTL2 Class I & II (2.5 V)	SSTL3 Class I & II (3.3 V)	LVDS (2.5 V)	LVPECL (3.3 V)
LVTTTL 3.3 V (VREF=1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVTTTL 3.3 V (VREF=1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVC MOS 2.5 V (VREF=1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVC MOS 2.5 V (VREF=1.25V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVC MOS 1.8 V	–	–	✓	–	–	–	–	–	–	–	–	–
LVC MOS 1.5 V (VREF = 1.75 V) (JESD8-11)	–	–	–	✓	–	–	–	✓	–	–	–	–
3.3 V PCI/PCI-X (VREF = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
3.3 V PCI/PCI-X (VREF= 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
GTL + (3.3 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
GTL + (2.5 V)	–	✓	–	–	–	–	✓	–	–	–	–	–
HSTL Class I	–	–	–	✓	–	–	–	✓	–	–	–	–
SSTL2 Class I & II	–	✓	–	–	–	–	–	–	✓	–	✓	–
SSTL3 Class I & II	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVDS (VREF = 1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVDS (VREF = 1.25 V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVPECL (VREF = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVPECL (VREF = 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓

Notes:

1. Note that GTL+ 2.5 V is not supported across the full military temperature range.
2. A "✓" indicates whether standards can be used within a bank at the same time.

Examples:

- a) LVTTTL can be used with 3.3V PCI and GTL+ (3.3V), when $V_{REF} = 1.0V$ (GTL+ requirement).
- b) LVTTTL can be used with 3.3V PCI and SSTL3 Class I and II, when $V_{REF} = 1.5V$ (SSTL3 requirement).

Note that two I/O standards are compatible if:

- Their VCCI values are identical.
- Their VREF standards are identical (if applicable).

For example, if LVTTTL 3.3 V (VREF= 1.0 V) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTTL 3.3 V PCI/PCI-X, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank.

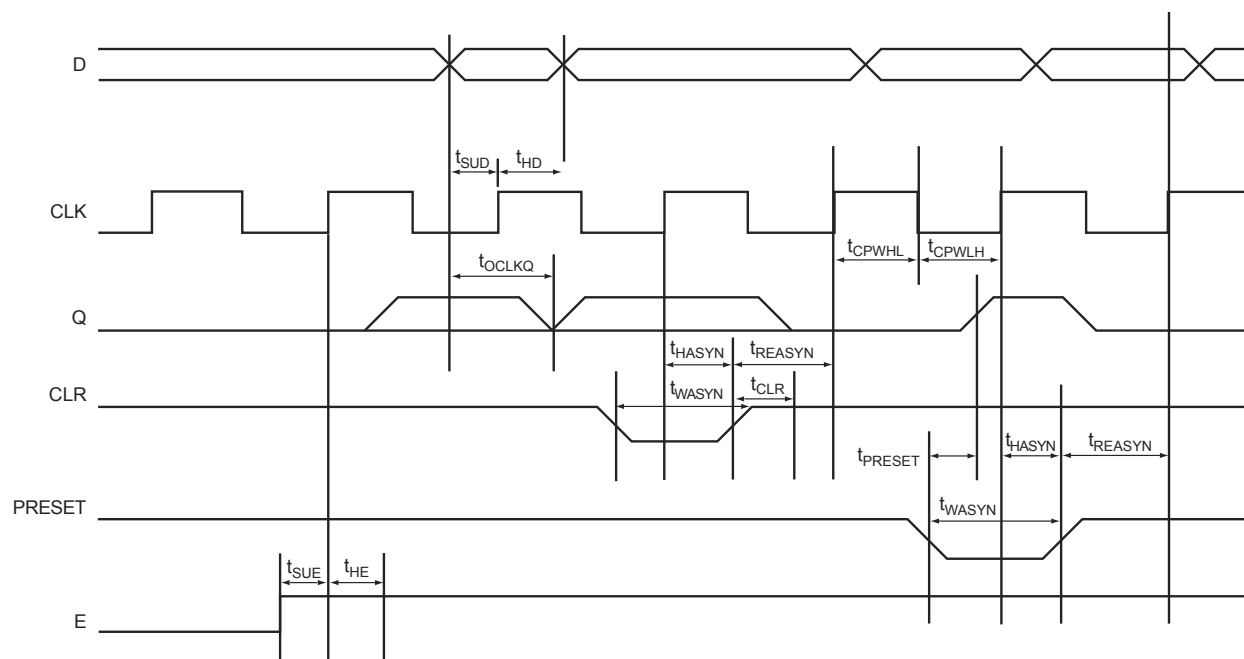


Figure 2-13 • Output Register Timing Characteristics

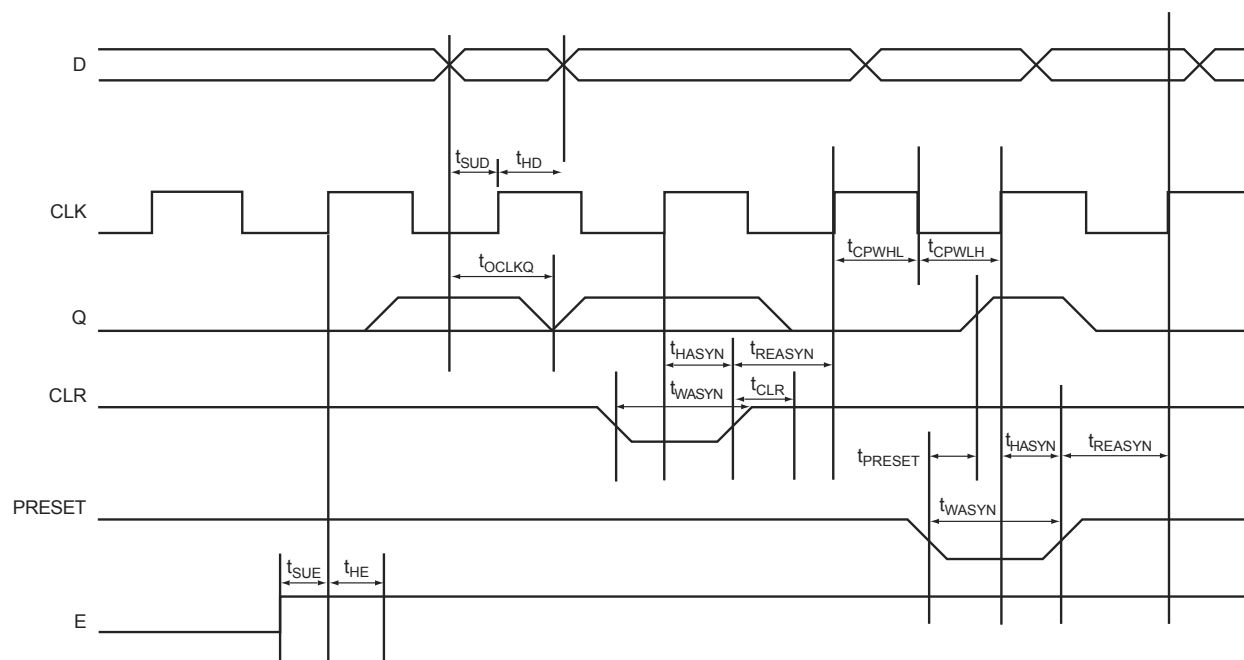


Figure 2-14 • Output Enable Register Timing Characteristics

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		12.14		13.83		16.26	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

1.8 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-26 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	0.2 VCCI	0.7 VCCI	3.6	0.2	VCCI - 0.2	8 mA	-8 mA

AC Loadings

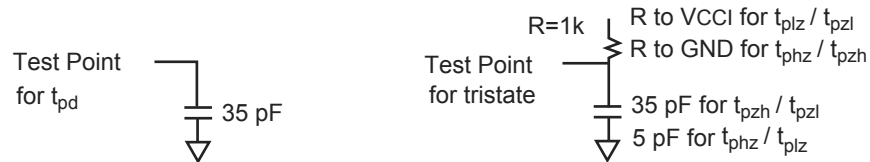


Figure 2-17 • AC Test Loads

Table 2-27 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	Cload (pF)
0	1.8	0.5 VCCI	N/A	35

Note: * Measuring Point = VTRIP

Table 2-36 • 3.3 V PCI-X I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V PCI-X Output Module Timing								
t _{DP}	Input Buffer	1.57		1.79		2.10		ns
t _{PY}	Output Buffer	2.10		2.40		2.82		ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low	1.61		1.62		1.63		ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High	1.59		1.60		1.61		ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z	2.65		3.02		3.55		ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z	3.11		3.55		4.17		ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register	0.67		0.77		0.90		ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time	0.13		0.15		0.17		ns
t _{HASYN}	Asynchronous Removal Time	0.00		0.00		0.00		ns
t _{CLR}	Asynchronous Clear-to-Q	0.23		0.27		0.31		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.23		0.27		0.31		ns

Class II

Table 2-53 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16

AC Loadings

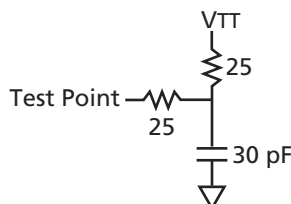


Figure 2-24 • AC Test Loads

Table 2-54 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-55 • 3.3 V SSTL3 Class II I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V SSTL3 Class II I/O Module Timing								
t _{DP}	Input Buffer		1.85		2.10		2.47	ns
t _{PY}	Output Buffer		2.17		2.47		2.91	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Axcelerator Clock Management System

Introduction

Each member of the Axcelerator family⁶ contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20 μ s

Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 μ F and 10 μ F decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

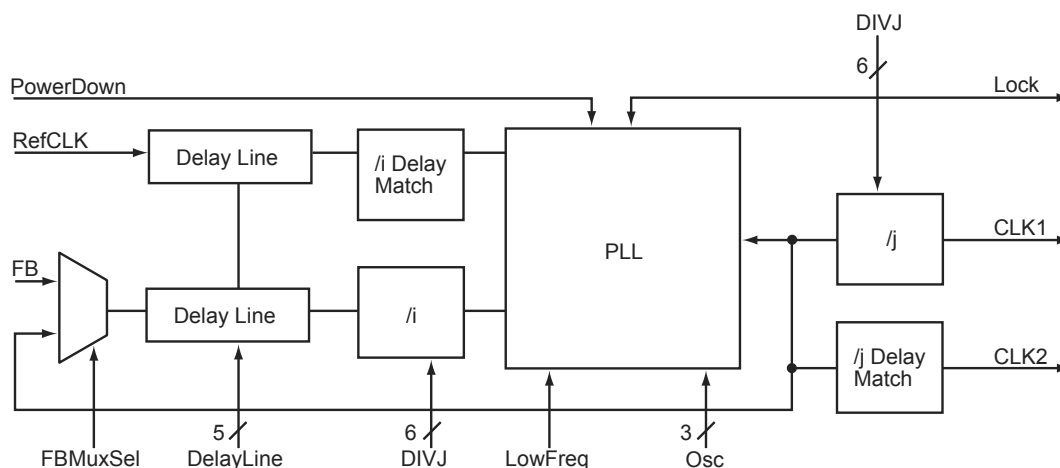


Figure 2-48 • PLL Block Diagram

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

6. AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.

Timing Characteristics

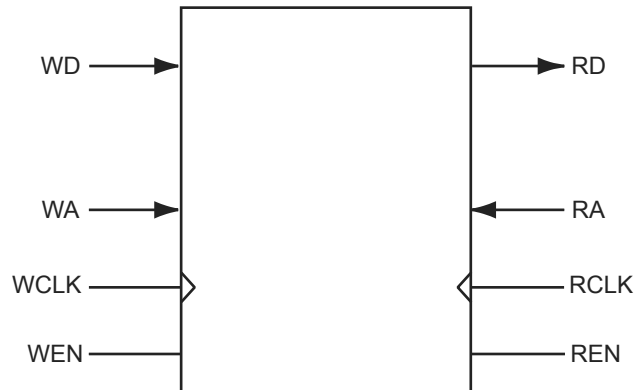


Figure 2-58 • SRAM Model

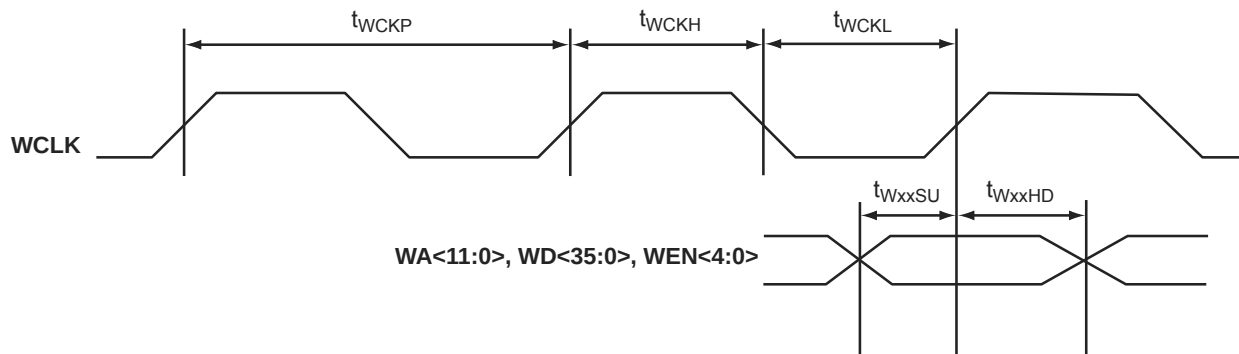


Figure 2-59 • RAM Write Timing Waveforms

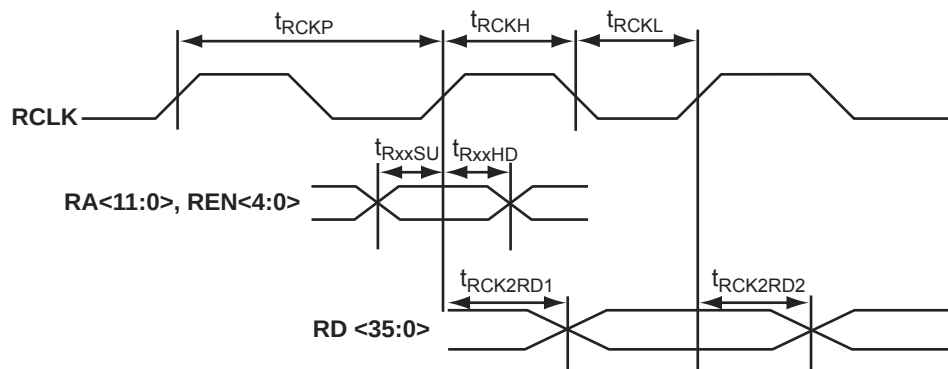


Figure 2-60 • RAM Read Timing Waveforms

Table 2-101 • Eight FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

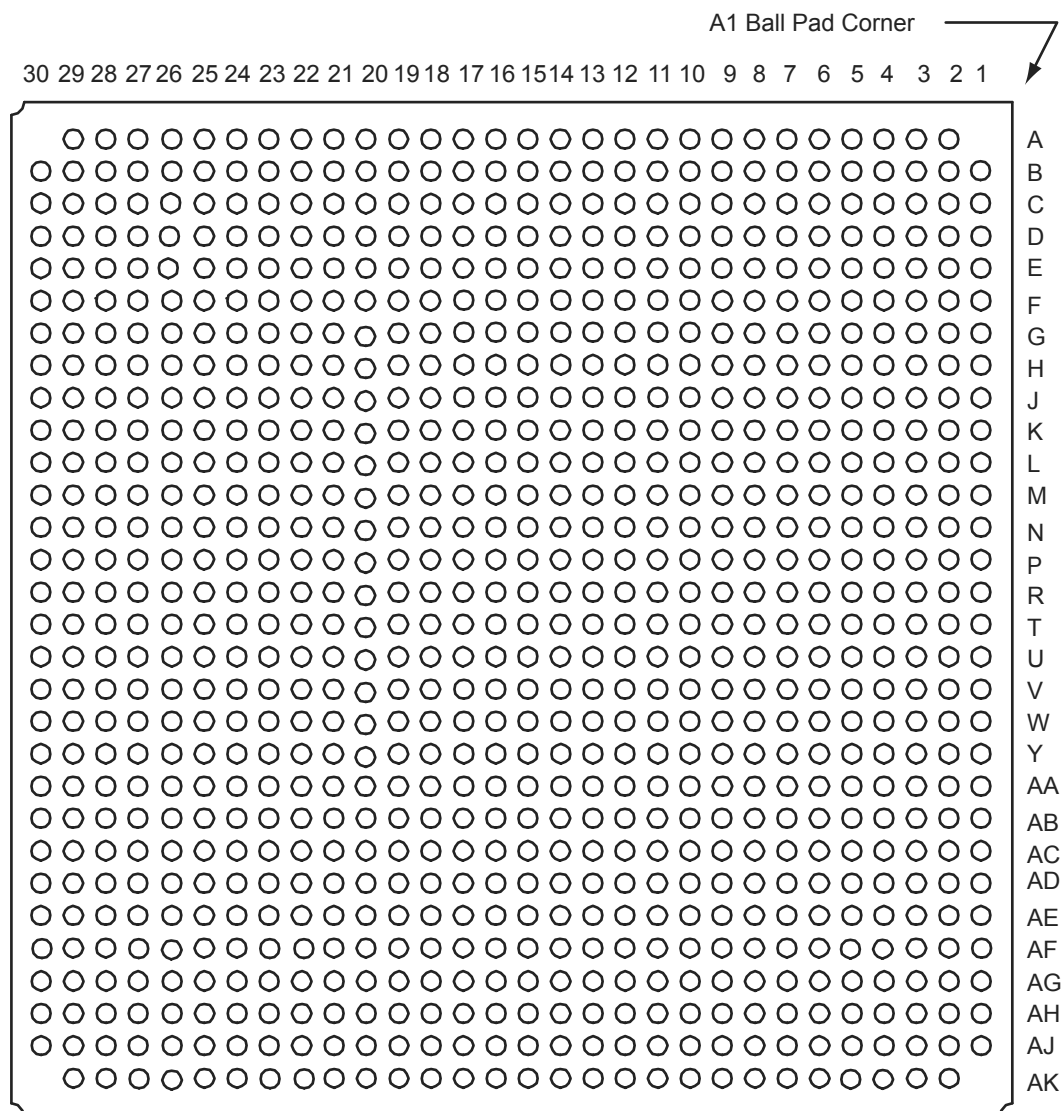
		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		15.46		17.61		20.70	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		5.13		5.13		5.13	ns
t _{WCKP}	Minimum WCLK Period	5.88		5.88		5.88		ns
t _{RSU}	Read Setup		16.22		18.47		21.72	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		5.77		5.77		5.77	ns
t _{RCKP}	Minimum RCLK period	6.50		6.50		6.50		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		3.39		3.86		4.54	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		4.93		5.62		6.61	ns

Note: Timing data for these eight cascaded FIFO blocks uses a depth of 32,768. For all other combinations, use Microsemi's timing software.

FG324		FG324		FG324	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
GND	R4	NC	N4	VCCA	M8
GND	T16	NC	N5	VCCA	M9
GND	T3	NC	R12	VCCA	P4
GND	U17	NC	R13	VCCA	R15
GND	U2	NC	R6	VCCPLA	D8
GND	V1	NC	R7	VCCPLB	E7
GND	V18	NC	T12	VCCPLC	B11
GND/LP	E5	NC	T6	VCCPLD	E11
NC	A10	NC	U16	VCCPLE	R11
NC	A11	NC	V17	VCCPLF	P12
NC	A12	PRA	E9	VCCPLG	U8
NC	A13	PRB	D9	VCCPLH	P8
NC	A8	PRC	P10	VCCDA	B3
NC	A9	PRD	R10	VCCDA	D14
NC	B12	TCK	E6	VCCDA	E10
NC	F15	TDI	D7	VCCDA	J2
NC	F4	TDO	D5	VCCDA	K16
NC	G15	TMS	D4	VCCDA	P15
NC	G4	TRST	D6	VCCDA	P9
NC	H14	VCCA	E15	VCCDA	R5
NC	H15	VCCA	G10	VCCIB0	F7
NC	H5	VCCA	G11	VCCIB0	F8
NC	J1	VCCA	G5	VCCIB0	F9
NC	J14	VCCA	G8	VCCIB1	F10
NC	J15	VCCA	G9	VCCIB1	F11
NC	J5	VCCA	H12	VCCIB1	F12
NC	K14	VCCA	H7	VCCIB2	G13
NC	K15	VCCA	J12	VCCIB2	H13
NC	K5	VCCA	J7	VCCIB2	J13
NC	L14	VCCA	K12	VCCIB3	K13
NC	L15	VCCA	K7	VCCIB3	L13
NC	L5	VCCA	L12	VCCIB3	M13
NC	M4	VCCA	L7	VCCIB4	N10
NC	M5	VCCA	M10	VCCIB4	N11
NC	N17	VCCA	M11	VCCIB4	N12

FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
NC	J5	VCCA	J10	VCCDA	AD10
NC	J6	VCCA	J11	VCCDA	AD13
NC	P22	VCCA	J12	VCCDA	AD17
NC	R20	VCCA	J13	VCCDA	B1
NC	R21	VCCA	J14	VCCDA	B17
NC	R22	VCCA	J15	VCCDA	D24
NC	R4	VCCA	J16	VCCDA	E14
NC	R5	VCCA	J17	VCCDA	P2
NC	T22	VCCA	K18	VCCDA	P23
NC	T24	VCCA	K9	VCCIB0	G10
NC	U22	VCCA	L18	VCCIB0	G8
NC	U24	VCCA	L9	VCCIB0	G9
NC	V22	VCCA	M18	VCCIB0	H10
NC	V5	VCCA	M9	VCCIB0	H11
NC	W21	VCCA	N18	VCCIB0	H12
NC	W22	VCCA	N9	VCCIB0	H13
NC	W5	VCCA	P18	VCCIB0	H9
NC	W6	VCCA	P9	VCCIB1	G17
NC	Y21	VCCA	R18	VCCIB1	G18
NC	Y4	VCCA	R9	VCCIB1	G19
NC	Y5	VCCA	T18	VCCIB1	H14
NC	Y6	VCCA	T9	VCCIB1	H15
PRA	E13	VCCA	U18	VCCIB1	H16
PRB	B14	VCCA	U9	VCCIB1	H17
PRC	Y14	VCCA	V10	VCCIB1	H18
PRD	AD14	VCCA	V11	VCCIB2	H20
TCK	E5	VCCA	V12	VCCIB2	J19
TDI	B3	VCCA	V13	VCCIB2	J20
TDO	G6	VCCA	V14	VCCIB2	K19
TMS	D4	VCCA	V15	VCCIB2	K20
TRST	A2	VCCA	V16	VCCIB2	L19
VCCA	AB4	VCCA	V17	VCCIB2	M19
VCCA	AF24	VCCDA	A3	VCCIB2	N19
VCCA	C1	VCCDA	AB22	VCCIB3	P19
VCCA	C26	VCCDA	AB5	VCCIB3	R19

FG896



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG896	
AX2000 Function	Pin Number
IO65PB1F6	H20
IO66NB1F6	B23
IO66PB1F6	B21
IO67NB1F6	H21
IO67PB1F6	G21
IO68NB1F6	D22
IO68PB1F6	C22
IO69NB1F6	A25
IO69PB1F6	A24
IO70NB1F6	F22
IO70PB1F6	E22
IO71NB1F6	F21
IO71PB1F6	E21
IO73NB1F6	C24
IO73PB1F6	C23
IO74NB1F6	D24
IO74PB1F6	D23
IO75NB1F6	H23
IO75PB1F6	H22
IO76NB1F7	B25
IO76PB1F7	B24
IO78NB1F7	B26
IO78PB1F7	A26
IO79NB1F7	F23
IO79PB1F7	E23
IO80NB1F7	D25
IO80PB1F7	C25
IO81NB1F7	G23
IO81PB1F7	G22
IO82NB1F7	B27
IO82PB1F7	A27
IO83NB1F7	F24
IO83PB1F7	E24
IO84NB1F7	D26
IO84PB1F7	C26

FG896	
AX2000 Function	Pin Number
IO85NB1F7	F25
IO85PB1F7	E25
Bank 2	
IO86NB2F8	G26
IO86PB2F8	G25
IO87NB2F8	K23
IO87PB2F8	J23
IO88NB2F8	J24
IO88PB2F8	H24
IO89NB2F8	E29
IO89PB2F8	D29
IO90NB2F8	F27
IO90PB2F8	E27
IO91NB2F8	H26
IO91PB2F8	H25
IO92NB2F8	G28
IO92PB2F8	F28
IO93NB2F8	J26
IO93PB2F8	J25
IO94NB2F8	H27
IO94PB2F8	G27
IO95NB2F8	H29
IO95PB2F8	G29
IO96NB2F9	G30
IO96PB2F9	F30
IO97NB2F9	K25
IO97PB2F9	K24
IO98NB2F9	J28
IO98PB2F9	H28
IO99NB2F9	L23
IO99PB2F9	L24
IO100NB2F9	K27
IO100PB2F9	J27
IO101PB2F9	J30
IO102NB2F9	E30

FG896	
AX2000 Function	Pin Number
IO102PB2F9	D30
IO103NB2F9	L26
IO103PB2F9	K26
IO104NB2F9	F29
IO105NB2F9	M25
IO105PB2F9	L25
IO106NB2F9	K30
IO106PB2F9	K29
IO107NB2F10	M23
IO107PB2F10	M24
IO109NB2F10	M27
IO109PB2F10	L27
IO110NB2F10	M28
IO110PB2F10	L28
IO111NB2F10	N22
IO111PB2F10	N23
IO112NB2F10	M29
IO112PB2F10	L29
IO113NB2F10	N26
IO113PB2F10	M26
IO114NB2F10	M30
IO114PB2F10	L30
IO115NB2F10	N28
IO115PB2F10	N27
IO117NB2F10	N25
IO117PB2F10	N24
IO118NB2F11	N29
IO119NB2F11	P22
IO119PB2F11	P23
IO121NB2F11	P25
IO121PB2F11	P24
IO122NB2F11	P28
IO122PB2F11	P27
IO123NB2F11	R26
IO123PB2F11	P26

FG896	
AX2000 Function	Pin Number
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	Pin Number
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	N1	GND	U19	NC	A26
GND	N13	GND	U20	NC	AB2
GND	N22	GND	U21	NC	AB33
GND	N34	GND	U30	NC	AC34
GND	P14	GND	U5	NC	AD3
GND	P15	GND	V14	NC	AD34
GND	P16	GND	V15	NC	AE31
GND	P17	GND	V16	NC	AE33
GND	P18	GND	V17	NC	AE34
GND	P19	GND	V18	NC	AF1
GND	P20	GND	V19	NC	AF34
GND	P21	GND	V20	NC	AG2
GND	R14	GND	V21	NC	AG4
GND	R15	GND	V30	NC	AH1
GND	R16	GND	V5	NC	AH2
GND	R17	GND	W14	NC	AH31
GND	R18	GND	W15	NC	AH32
GND	R19	GND	W16	NC	AH34
GND	R20	GND	W17	NC	AJ1
GND	R21	GND	W18	NC	AJ2
GND	R3	GND	W19	NC	AJ3
GND	R32	GND	W20	NC	AJ31
GND	T14	GND	W21	NC	AJ32
GND	T15	GND	Y14	NC	AJ33
GND	T16	GND	Y15	NC	AJ34
GND	T17	GND	Y16	NC	AJ4
GND	T18	GND	Y17	NC	AL29
GND	T19	GND	Y18	NC	AM19
GND	T20	GND	Y19	NC	AM7
GND	T21	GND	Y20	NC	AN13
GND	U14	GND	Y21	NC	AN17
GND	U15	GND	Y3	NC	AN25
GND	U16	GND	Y32	NC	AN27
GND	U17	GND/LP	G6	NC	AN8
GND	U18	NC	A17	NC	AP17

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	A8	GND/LP	E8	GND	V1
GND	AA10	GND	H1	GND	V25
GND	AA16	GND	H21	GND	V5
GND	AA18	GND	H25	NC	A14
GND	AA21	GND	K21	NC	AA20
GND	AA5	GND	K23	NC	AB13
GND	AB22	GND	K3	NC	AD4
GND	AB4	GND	L11	NC	AE12
GND	AC10	GND	L12	NC	F21
GND	AC16	GND	L13	NC	G10
GND	AC23	GND	L14	PRA	F13
GND	AC3	GND	L15	PRB	A13
GND	AD1	GND	M11	PRC	AB12
GND	AD2	GND	M12	PRD	AE13
GND	AD24	GND	M13	TCK	F5
GND	AD25	GND	M14	TDI	C5
GND	AE1	GND	M15	TDO	F6
GND	AE18	GND	N11	TMS	D6
GND	AE2	GND	N12	TRST	E6
GND	AE24	GND	N13	VCCA	AB20
GND	AE25	GND	N14	VCCA	F22
GND	AE8	GND	N15	VCCA	F4
GND	B1	GND	P11	VCCA	J17
GND	B2	GND	P12	VCCA	J9
GND	B24	GND	P13	VCCA	K10
GND	B25	GND	P14	VCCA	K11
GND	C10	GND	P15	VCCA	K15
GND	C16	GND	R11	VCCA	K16
GND	C23	GND	R12	VCCA	L10
GND	C3	GND	R13	VCCA	L16
GND	D22	GND	R14	VCCA	R10
GND	D4	GND	R15	VCCA	R16
GND	E10	GND	T21	VCCA	T10
GND	E16	GND	T23	VCCA	T11
GND	E21	GND	T3	VCCA	T15
GND	E5	GND	T5	VCCA	T16

CG624	
AX2000 Function	Pin Number
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22*
IO169PB3F15	W23*
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20*
IO171PB4F16	AC21*
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

Revision	Changes	Page
Revision 3 (continued)	The timing characteristics tables from pages 2-26 to 2-60 were updated.	2-26 to 2-60
	The "Global Resources" section was updated.	2-66
	The timing characteristics tables from pages 2-102 to 2-103 were updated.	2-102 to 2-103
	The "PQ208", "FG256", and "FG324" tables are new.	3-9,3-16, 3-84