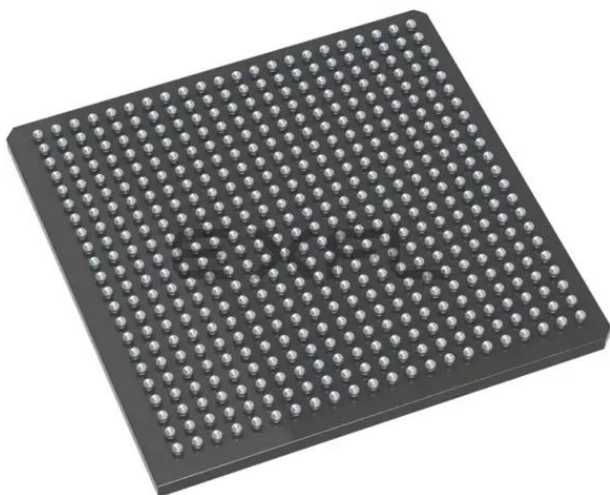




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	317
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-1fg484m

Two C-cells, a single R-cell, two Transmit (TX), and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

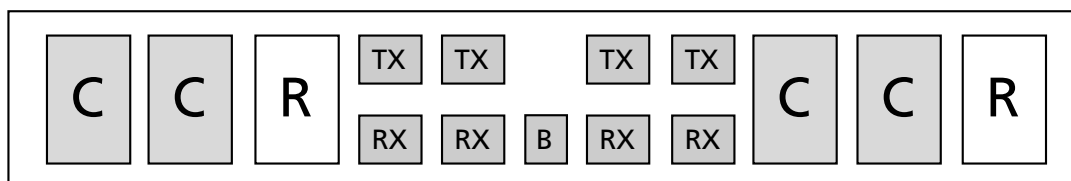


Figure 1-4 • AX SuperCluster

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

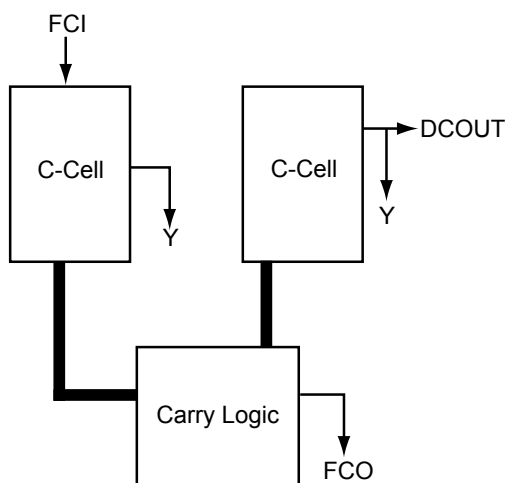


Figure 1-5 • AX 2-Bit Carry Logic

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the AX1000 is composed of a 3x3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1). Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the AX250).

Table 1-1 • Number of Core Tiles per Device

Device	Number of Core Tiles
AX125	1 regular tile
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 k Ω). These are weak transistors with the gates tied on, so the on resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors; they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8 mA, 12 mA, 16 mA, or 24 mA – that can be specified in Designer.⁵

Table 2-14 • Bank-Wide Delay Values

Bits Setting	Delay (ns)	Bits Setting	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

5. These values are minimum drive strengths.

Table 2-15, Table 2-16, and Table 2-17 list all the available macro names differentiated by I/O standard, type, slew rate, and drive strength.

Table 2-15 • Macros for Single-Ended I/O Standards

Standard	VCCI	Macro Names
LVTTTL	3.3 V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_H_8, OUTBUF_H_12, OUTBUF_H_16, OUTBUF_H_24, TRIBUF, TRIBUF_S_8, TRIBUF_S_12, TRIBUF_S_16, TRIBUF_S_24, TRIBUF_H_8, TRIBUF_H_12, TRIBUF_H_16, TRIBUF_H_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_H_8, BIBUF_H_12, BIBUF_H_16, BIBUF_H_24
3.3 V PCI	3.3 V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUF_PCI, BIBUF_PCI
3.3 V PCI-X	3.3 V	CLKBUF_PCI-X, HCLKBUF_PCI-X, INBUF_PCI-X, OUTBUF_PCI-X, TRIBUF_PCI-X, BIBUF_PCI-X
LVC MOS25	2.5 V	CLKBUF_LVC MOS25, HCLKBUF_LVC MOS25, INBUF_LVC MOS25, OUTBUF_LVC MOS25, TRIBUF_LVC MOS25, BIBUF_LVC MOS25
LVC MOS18	1.8 V	CLKBUF_LVC MOS18, HCLKBUF_LVC MOS18, INBUF_LVC MOS18, OUTBUF_LVC MOS18, TRIBUF_LVC MOS18, BIBUF_LVC MOS18
LVC MOS15 (JESD8-11)	1.5 V	CLKBUF_LVC MOS15, HCLKBUF_LVC MOS15, INBUF_LVC MOS15, OUTBUF_LVC MOS15, TRIBUF_LVC MOS15, BIBUF_LVC MOS15

Table 2-16 • I/O Macros for Differential I/O Standards

Standard	VCCI	Macro Names
LVPECL	3.3 V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL
LVDS	2.5 V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS

Table 2-17 • I/O Macros for Voltage-Referenced I/O Standards

Standard	VCCI	VREF	Macro Names
GTL+	3.3 V	1.0 V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUF_GTP33, BIBUF_GTP33
GTL+	2.5 V	1.0 V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUF_GTP25, BIBUF_GTP25
SSTL2 Class I	2.5 V	1.25 V	CLKBUF_SSTL2_I, HCLKBUF_SSTL2_I, INBUF_SSTL2_I, OUTBUF_SSTL2_I, TRIBUF_SSTL2_I, BIBUF_SSTL2_I
SSTL2 Class II	2.5 V	1.25 V	CLKBUF_SSTL2_II, HCLKBUF_SSTL2_II, INBUF_SSTL2_II, OUTBUF_SSTL2_II, TRIBUF_SSTL2_II, BIBUF_SSTL2_II
SSTL3 Class I	3.3 V	1.5 V	CLKBUF_SSTL3_I, HCLKBUF_SSTL3_I, INBUF_SSTL3_I, OUTBUF_SSTL3_I, TRIBUF_SSTL3_I, BIBUF_SSTL3_I
SSTL3 Class II	3.3 V	1.5 V	CLKBUF_SSTL3_II, HCLKBUF_SSTL3_II, INBUF_SSTL3_II, OUTBUF_SSTL3_II, TRIBUF_SSTL3_II, BIBUF_SSTL3_II
HSTL Class I	1.5 V	0.75 V	CLKBUF_HSTL_I, HCLKBUF_HSTL_I, INBUF_HSTL_I, OUTBUF_HSTL_I, TRIBUF_HSTL_I, BIBUF_HSTL_I

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength =3 (16 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		11.03		12.56		14.77	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		11.42		13.01		15.29	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		11.04		12.58		14.79	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.86		1.88		1.88	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.50		2.51		2.52	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

1.8 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-26 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
−0.3	0.2 VCCI	0.7 VCCI	3.6	0.2	VCCI − 0.2	8 mA	−8 mA

AC Loadings

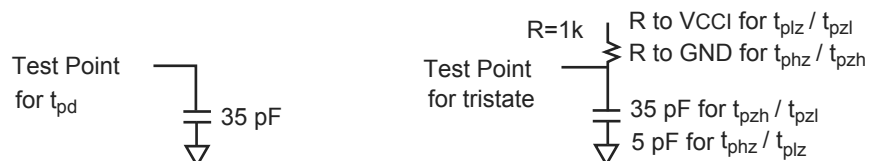


Figure 2-17 • AC Test Loads

Table 2-27 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
0	1.8	0.5 VCCI	N/A	35

Note: * Measuring Point = VTRIP

Table 2-57 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.2 – 0.125	1.2 + 0.125	1.2

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-58 • LVDS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
LVDS Output Module Timing								
t _{DP}	Input Buffer		1.80		2.05		2.41	ns
t _{PY}	Output Buffer		2.32		2.64		3.11	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Module Specifications

C-Cell

Introduction

The C-cell is one of the two logic module types in the AX architecture. It is the combinatorial logic resource in the Axcelerator device. The AX architecture implements a new combinatorial cell that is an extension of the C-cell implemented in the SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The C-cell features the following (Figure 2-27):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns.
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns.

This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with Microsemi's extensive macro library (please see the *Antifuse Macro Library Guide* for a complete listing of available Axcelerator macros).

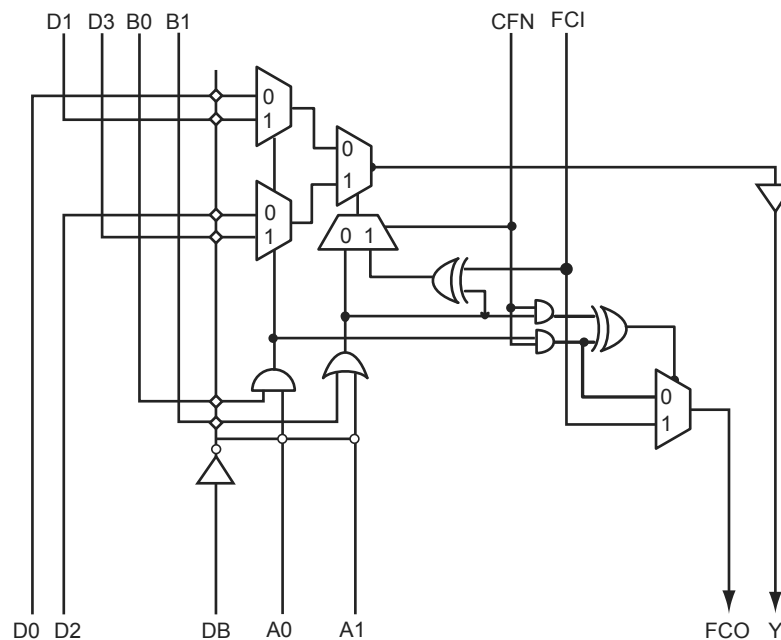


Figure 2-27 • C-Cell

Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-38).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-39).

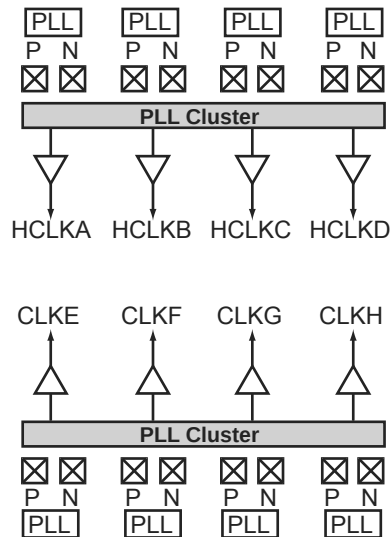


Figure 2-38 • PLL Group

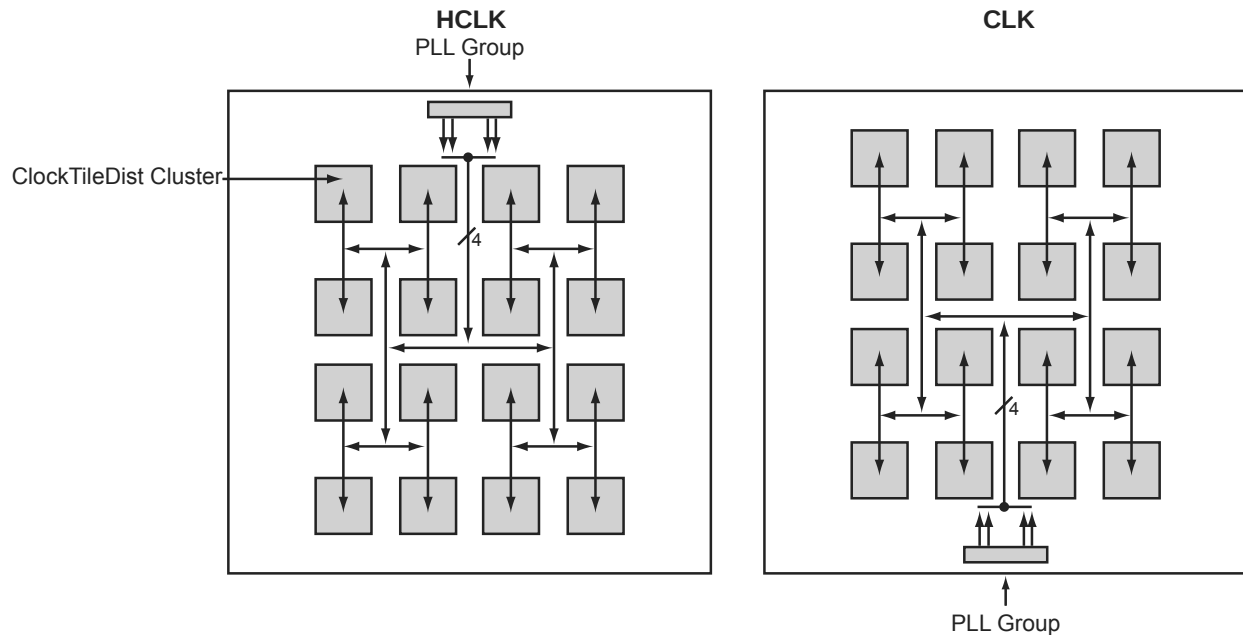


Figure 2-39 • Example of HCLK and CLK Distributions on the AX2000

PLLCLK and PLLHCLK

PLLCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 2-44).

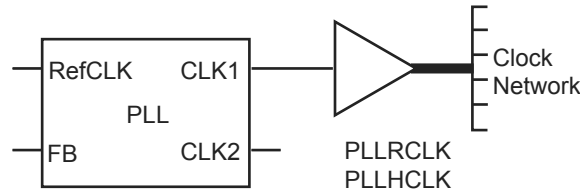


Figure 2-44 • PLLCLK and PLLHCLK

Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc. (Figure 2-45).

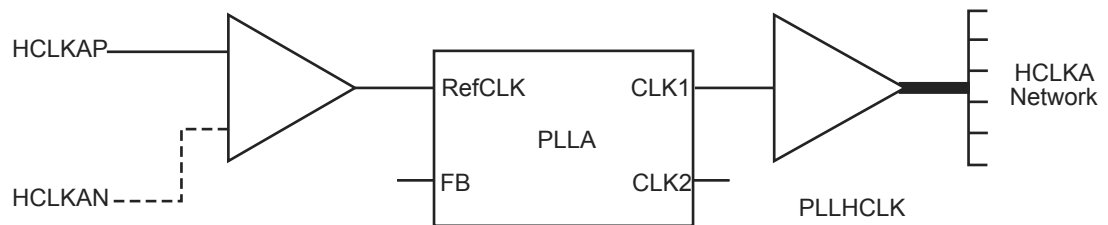


Figure 2-45 • Example of HCLKA Driven from a PLL with External Clock Source

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 2-46).

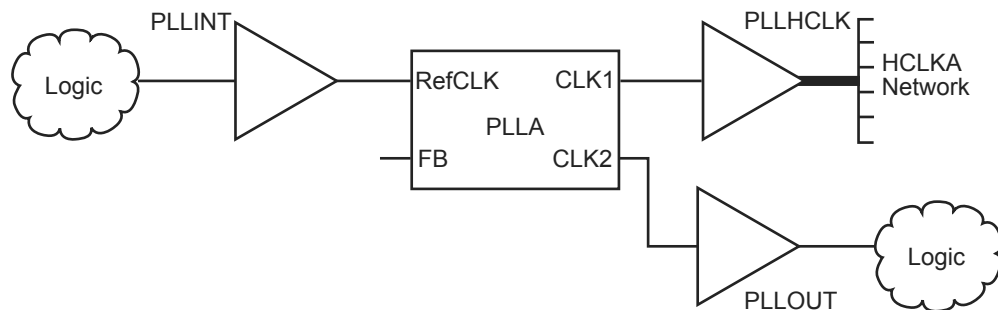


Figure 2-46 • Example of PLLINT and PLLOUT Usage

CLK1 and CLK2

Both PLL outputs, CLK1 and CLK2, can be used to drive a global resource, an adjacent PLL RefCLK input, or a net in the FPGA core. Not all drive combinations are possible (Table 2-81).

Table 2-81 • PLL General Connections Rules

CLK1	CLK2
HCLK	HCLK
CLK	CLK
HCLK	Routed net output
Routed net output	HCLK
HCLK	NONE
NONE	HCLK
CLK	NONE
NONE	CLK

Note: The PLL outputs remain Low when REFCLK is constant (either Low or High).

Restrictions on CLK1 and CLK2

- When both are driving global resources, they must be driving the same type of global resource (i.e. either HCLK or CLK).
- Only one can drive a routed net at any given time.

Table 2-82 and Table 2-83 specify all the possible CLK1 and CLK2 connections for the north and south PLLs. HCLK1 and HCLK2 are used to denote the different HCLK networks when two are being driven at the same time by a single PLL (Note that HCLK1 is the primary clock resource associated with the PLL, and HCLK2 is the clock resource associated with the adjacent PLL). Likewise, CLK1 and CLK2 are used to denote the different CLK networks when two are being driven at the same time by a single PLL (Figure 2-48 on page 2-75).

Table 2-82 • North PLL Connections

CLK1	CLK2
HCLK1	Routed net
HCLK1	Unused
HCLK2	HCLK1
HCLK2	Routed net
HCLK2	Both HCLK1 and routed net
HCLK2	Unused
Unused	HCLK1
Unused	Routed net
Unused	Both HCLK1 and routed net
Unused	Unused
Routed net	HCLK1
Routed net	Unused
Both HCLK1 and HCLK2	Routed net
Both HCLK1 and HCLK2	Unused
Both HCLK1 and routed net	Unusable
Both HCLK2 and routed net	HCLK1
Both HCLK2 and routed net	Unused
HCLK1, HCLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g. CLK1 driving HCLK1, and HCLK2 is not supported).

Table 2-99 • Two FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		13.75		15.66		18.41	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		1.76		1.76		1.76	ns
t _{WCKP}	Minimum WCLK Period	2.51		2.51		2.51		ns
t _{RSU}	Read Setup		14.33		16.32		19.19	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		1.89		1.89		1.89	ns
t _{RCKP}	Minimum RCLK period	2.62		2.62		2.62		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		1.43		1.63		1.92	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		2.26		2.58		3.03	ns

Note: Timing data for these two cascaded FIFO blocks uses a depth of 8,192. For all other combinations, use Microsemi's timing software.

Table 2-102 • Sixteen FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		16.32		18.60		21.86	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		13.40		13.40		13.40	ns
t _{WCKP}	Minimum WCLK Period	14.15		14.15		14.15		ns
t _{RSU}	Read Setup		17.16		19.54		22.97	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		14.41		14.41		14.41	ns
t _{RCKP}	Minimum RCLK period	15.14		15.14		15.14		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		12.83		14.62		17.18	ns

Note: Timing data for these sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen Core Generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (refer to the *SmartGen*, *FlashROM*, *Analog System Builder*, and *Flash Memory System Builder* User's Guide for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Low Power Mode

Although designed for high performance, the AX architecture also allows the user to place the device into a low power mode. Each I/O bank in an Axcelerator device can be configured individually, when in low power mode, to tristate all outputs, disable inputs, or both. The low power mode is activated by asserting the LP pin, which is grounded in normal operation.

While in the low power mode, the device is still fully functional and all internal logic states are preserved. This allows a user to disable all but a few signals and operate the part in a low-frequency, watchdog

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	B27	GND	R11	VCCA	K11
GND	B3	GND	R12	VCCA	K17
GND	C1	GND	R13	VCCA	K18
GND	C2	GND	R14	VCCA	L10
GND	C25	GND	R15	VCCA	L18
GND	C26	GND	R16	VCCA	U10
GND	C27	GND	R17	VCCA	U18
GND	C3	GND	T11	VCCA	V10
GND	E27	GND	T12	VCCA	V11
GND	L11	GND	T13	VCCA	V17
GND	L12	GND	T14	VCCA	V18
GND	L13	GND	T15	VCCPLA	A13
GND	L14	GND	T16	VCCPLB	J13
GND	L15	GND	T17	VCCPLC	B15
GND	L16	GND	U11	VCCPLD	C15
GND	L17	GND	U12	VCCPLE	AG14
GND	M11	GND	U13	VCCPLF	AF14
GND	M12	GND	U14	VCCPLG	AB13
GND	M13	GND	U15	VCCPLH	AG13
GND	M14	GND	U16	VCCDA	A11
GND	M15	GND	U17	VCCDA	AB12
GND	M16	GND/LP	J8	VCCDA	AC12
GND	M17	NC	U3	VCCDA	AC25
GND	N11	PRA	J14	VCCDA	AD16
GND	N12	PRB	D14	VCCDA	AD17
GND	N13	PRC	V14	VCCDA	E16
GND	N14	PRD	AB14	VCCDA	E2
GND	N15	TCK	E4	VCCDA	E24
GND	N16	TDI	D4	VCCDA	F12
GND	N17	TDO	J9	VCCDA	F16
GND	P11	TMS	H8	VCCDA	F7
GND	P12	TRST	E3	VCCDA	K14
GND	P13	VCCA	AA21	VCCDA	P10
GND	P14	VCCA	AD5	VCCDA	P18
GND	P15	VCCA	E1	VCCDA	W14
GND	P16	VCCA	G22	VCCDA	W9
GND	P17	VCCA	K10	VCCIB0	A4

FG484	
AX500 Function	Pin Number
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	Pin Number
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	Pin Number
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG484	
AX1000 Function	Pin Number
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	AB16
VCCDA	AB8
VCCDA	C10
VCCDA	C11
VCCDA	C14
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX1000 Function	Pin Number
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX1000 Function	Pin Number
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG896	
AX1000 Function	Pin Number
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3

FG896	
AX1000 Function	Pin Number
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG896	
AX2000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX2000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	Pin Number
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO103PB2F9	M28	IO121NB2F11	T27	IO138NB3F12	Y29
IO104NB2F9	M34	IO121PB2F11	T26	IO138PB3F12	W29
IO104PB2F9	L34	IO122NB2F11	T30	IO139NB3F13	Y27
IO105NB2F9	P27	IO122PB2F11	T29	IO139PB3F13	W27
IO105PB2F9	N27	IO123NB2F11	U28	IO140NB3F13	AA33
IO106NB2F9	M32	IO123PB2F11	T28	IO140PB3F13	Y33
IO106PB2F9	M31	IO124NB2F11	T31	IO141NB3F13	Y25
IO107NB2F10	P25	IO124PB2F11	T32	IO141PB3F13	Y24
IO107PB2F10	P26	IO125NB2F11	U24	IO142NB3F13	AA31
IO108NB2F10	N33	IO125PB2F11	U25	IO142PB3F13	Y31
IO108PB2F10	M33	IO126NB2F11	U33	IO143NB3F13	AA28
IO109NB2F10	P29	IO126PB2F11	U34	IO143PB3F13	Y28
IO109PB2F10	N29	IO127NB2F11	U26	IO144NB3F13	AA34
IO110NB2F10	P30	IO127PB2F11	U27	IO144PB3F13	Y34
IO110PB2F10	N30	IO128NB2F11	U31	IO145NB3F13	AA26
IO111NB2F10	R24	IO128PB2F11	U32	IO145PB3F13	Y26
IO111PB2F10	R25	Bank 3		IO146NB3F13	AA29
IO112NB2F10	P31	IO129NB3F12	V29	IO146PB3F13	AA30
IO112PB2F10	N31	IO129PB3F12	U29	IO147NB3F13	AB30
IO113NB2F10	R28	IO130NB3F12	V31	IO147PB3F13	AB29
IO113PB2F10	P28	IO130PB3F12	V32	IO148NB3F13	AB32
IO114NB2F10	P32	IO131NB3F12	V24	IO148PB3F13	AA32
IO114PB2F10	N32	IO131PB3F12	V25	IO149NB3F13	AB27
IO115NB2F10	R30	IO132NB3F12	W28	IO149PB3F13	AA27
IO115PB2F10	R29	IO132PB3F12	V28	IO150NB3F14	AC31
IO116NB2F10	P34	IO133NB3F12	W26	IO150PB3F14	AB31
IO116PB2F10	P33	IO133PB3F12	V26	IO151NB3F14	AD33
IO117NB2F10	R27	IO134NB3F12	W33	IO151PB3F14	AC33
IO117PB2F10	R26	IO134PB3F12	V33	IO152NB3F14	AC28
IO118NB2F11	R34	IO135NB3F12	W25	IO152PB3F14	AB28
IO118PB2F11	R33	IO135PB3F12	W24	IO153NB3F14	AB25
IO119NB2F11	T24	IO136NB3F12	W31	IO153PB3F14	AA25
IO119PB2F11	T25	IO136PB3F12	W32	IO154NB3F14	AD32
IO120NB2F11	T33	IO137NB3F12	Y30	IO154PB3F14	AC32
IO120PB2F11	T34	IO137PB3F12	W30	IO155NB3F14	AD29

PQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132

PQ208	
AX500 Function	Pin Number
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
Bank 4	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76

PQ208	
AX500 Function	Pin Number
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158