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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	317
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-1fgg484i

Figure 1-2 • **Axcelerator Family Interconnect Elements**

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

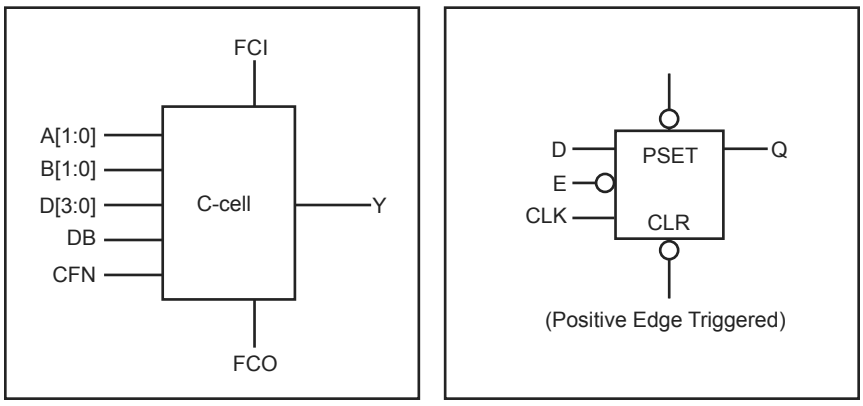
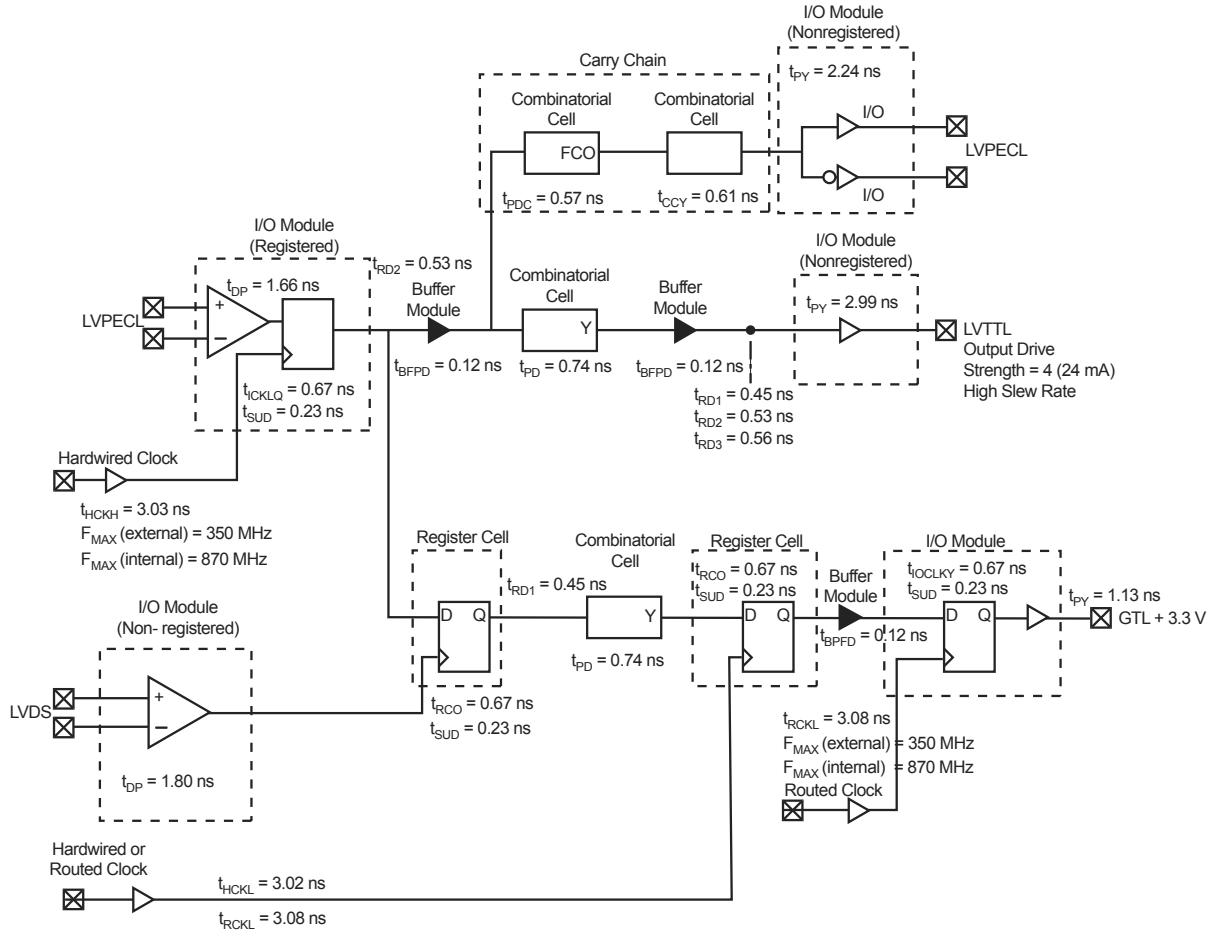


Figure 1-3 • **AX C-Cell and R-Cell**

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

Timing Model



Note: Worst case timing data for the AX1000, –2 speed grade

Figure 2-1 • **Worst Case Timing Data**

Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$= (t_{DP} + t_{RD2} + t_{SUD}) – t_{HCKL}$

$= (1.72 + 0.53 + 0.23) – 3.02 = –0.54$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{HCKL} + t_{RCO} + t_{RD1} + t_{PY}$

$= 3.02 + 0.67 + 0.45 + 2.99 = 7.13$ ns

Routed Clock – Using LVTTL 24 mA High Slew Clock I/O

External Setup

$= (t_{DP} + t_{RD2} + t_{SUD}) – t_{RCKH}$

$= (1.72 + 0.53 + 0.23) – 3.13 = –0.65$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$

$= 3.13 + 0.67 + 0.45 + 3.03 = 7.24$ ns

5 V Tolerance

There are two schemes to achieve 5 V tolerance:

1. 3.3 V PCI and 3.3 V PCI-X are the only I/O standards that directly allow 5 V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in EQ 3:

Vinput = VCCI + Vdiode = 3.3 V + 0.7 V = 4.0 V

EQ 3

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-3). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-19 on page 2-21). The GND clamp diode is available for all I/O standards and always enabled.

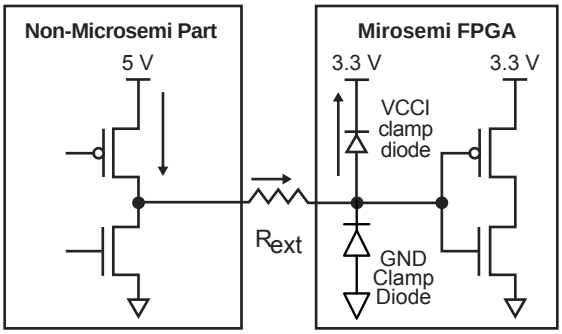


Figure 2-3 • **Use of an External Resistor for 5 V Tolerance**

2. 5 V tolerance can also be achieved with 3.3 V I/O standards (3.3 V PCI, 3.3 V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5 V signal to a 3.3 V signal with minimum delay (Figure 2-4).

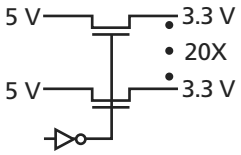


Figure 2-4 • **Bus Switch IDTQS32X2384**

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microsemi recommends that users not exceed eight simultaneous switching outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microsemi has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

3. The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.

Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Note that there are no tristated or bidirectional I/O buffers for differential standards.

Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users need to:

1. Instantiate an input buffer (with the required I/O standard)
2. Instantiate the DDR_REG macro (Figure 2-6)
3. Connect the output from the Input buffer to the input of the DDR macro

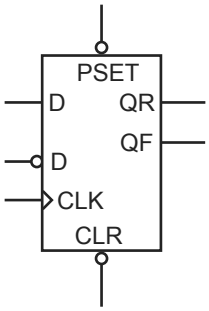


Figure 2-6 • **DDR Register**

Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required VCCI and VREF voltages for an I/O. The generic buffer macros require the LVTTL standard with slow slew rate and 24 mA-drive strength. LVTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (e.g. INBUF_LVDS) or a pair of differential outputs (e.g. OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (i.e. INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

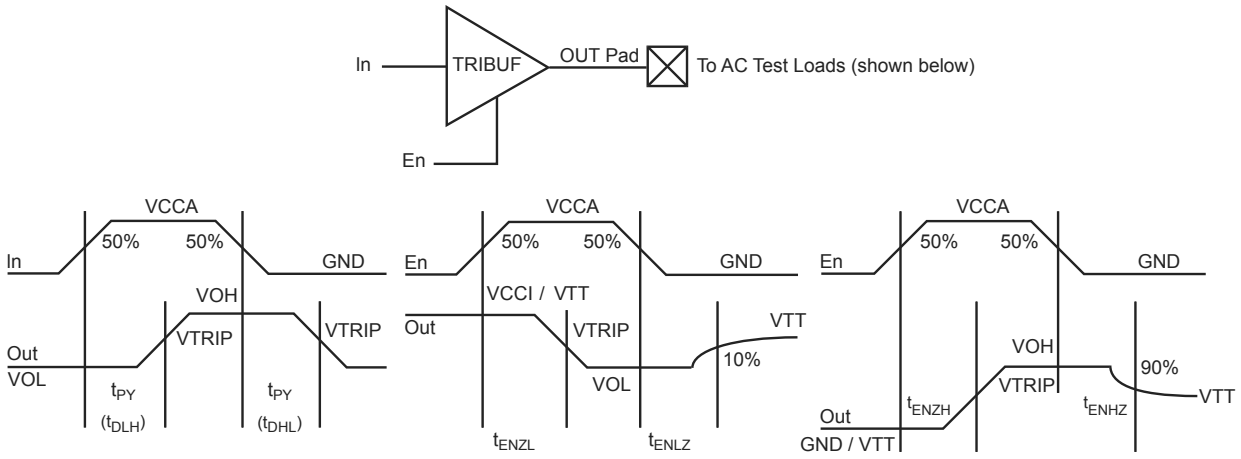


Figure 2-10 • **Output Buffer Delays**

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

***Table 2-41* • DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCC – 0.4	8	-8

AC Loadings

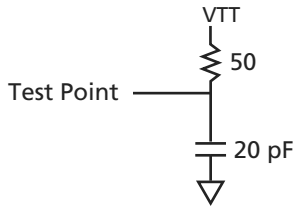


***Figure 2-20 •* AC Test Loads**

***Table 2-42* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
VREF –0.5	VREF + 0.5	VREF	0.75	20

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-43* • 1.5 V HSTL Class I I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.425 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
1.5 V HSTL Class I I/O Module Timing								
t_{DP}	Input Buffer		1.80		2.05		2.41	ns
t_{PY}	Output Buffer		4.90		5.58		6.56	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

R-Cell

Introduction

The R-cell, the sequential logic resource of the Axcelerator devices, is the second logic module type in the AX family architecture. It includes clock inputs for all eight global resources of the Axcelerator architecture as well as global presets and clears (Figure 2-31).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-Cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).
- Independent active-low asynchronous clear (CLR).
- Independent active-low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
  - One of the four high performance hardwired fast clocks (HCLKs)
  - One of the four routed clocks (CLKs)
  - User signals
- Global power-on clear (GCLR) and preset (GPSET), which drive each flip-flop on a chip-wide basis.
  - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET = 1 at device power-up. When the option is checked, GCLR = 1 and GPSET = 0. Both pins are pulled High when the device is in user mode. Refer to the "Simulation Support for GCLR/GPSET in Axcelerator" section of the *Antifuse Macro Library Guide* for information on simulation support for GCLR and GPSET.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Microsemi's extensive macro library (see the *Antifuse Macro Library Guide* for a complete listing of available AX macros).

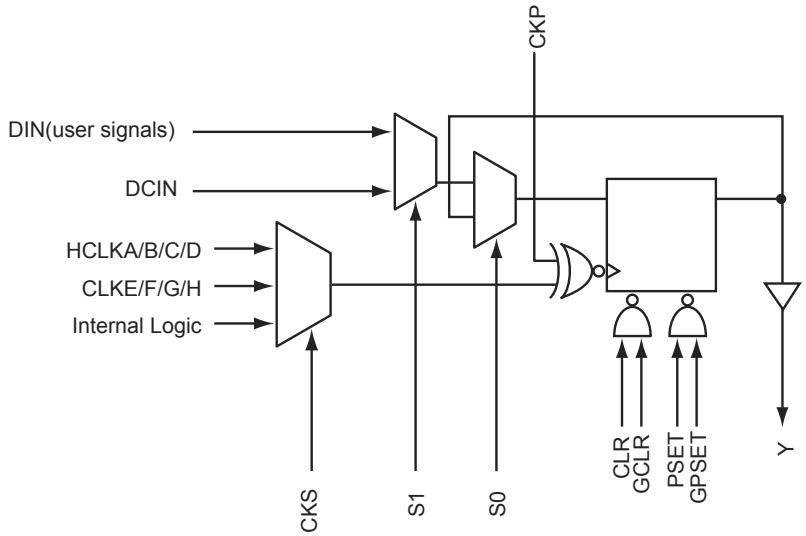


Figure 2-31 • **R-Cell**

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

***Table 2-70* • AX125 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-71* • AX250 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t_{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

BG729	
AX1000 Function	**Pin Number**
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16

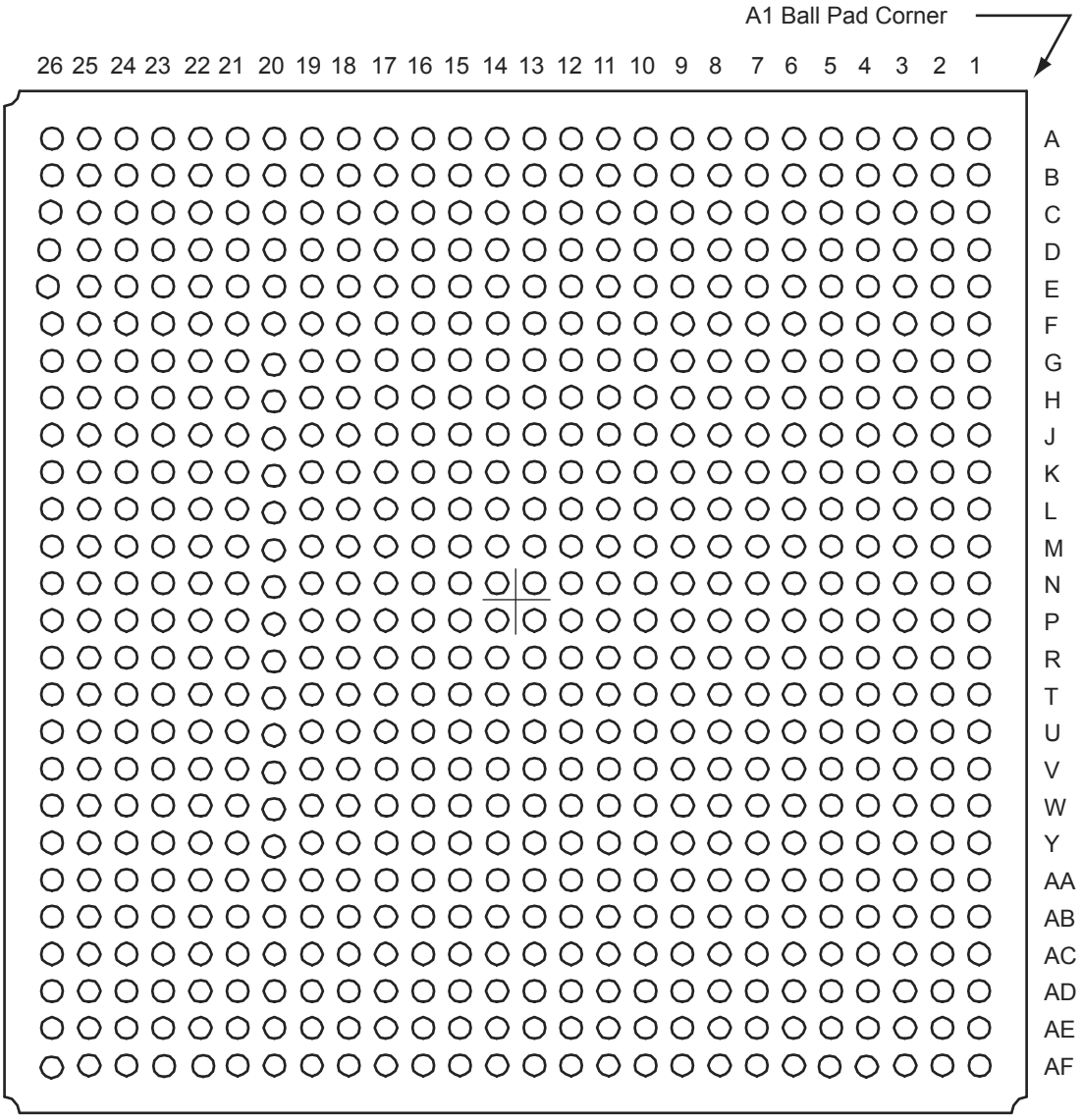
BG729	
AX1000 Function	**Pin Number**
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

FG484	
AX500 Function	**Pin Number**
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX500 Function	**Pin Number**
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX500 Function	**Pin Number**
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10

FG676



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG676	
AX500 Function	Pin Number
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A11
NC	A21

FG676	
AX500 Function	Pin Number
NC	A22
NC	A24
NC	A25
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
NC	AC25
NC	AD1
NC	AD11
NC	AD16
NC	AD25
NC	AE1
NC	AF2
NC	AF25
NC	B11
NC	B24
NC	B4
NC	C16

FG676	
AX500 Function	Pin Number
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
NC	G21
NC	G22
NC	H21
NC	H22
NC	H23
NC	H5
NC	H6

FG676	
AX1000 Function	**Pin Number**
Bank 0	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10

FG676	
AX1000 Function	**Pin Number**
IO21PB0F1	C10
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
Bank 1	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20

FG676	
AX1000 Function	**Pin Number**
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20
IO52PB1F4	C20
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
Bank 2	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG896	
AX2000 Function	Pin Number
GND	W19
GND	Y11
GND	Y20
GND/LP	E4
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20

FG896	
AX2000 Function	Pin Number
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCDA	AD24
VCCDA	AD7
VCCDA	AE15
VCCDA	AE16
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18
VCCDA	AF19
VCCDA	AH27
VCCDA	AH4
VCCDA	C13
VCCDA	C27
VCCDA	C5
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F15
VCCDA	F16
VCCDA	F26

FG896	
AX2000 Function	Pin Number
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

FG1152	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	D6
IO00PB0F0	C6
IO01NB0F0	H10
IO01PB0F0	H9
IO02NB0F0	F8
IO02PB0F0	G8
IO03NB0F0	A6
IO03PB0F0	B6
IO04NB0F0	C7
IO04PB0F0	D7
IO05NB0F0	K10
IO05PB0F0	J10
IO06NB0F0	F9
IO06PB0F0	G9
IO07NB0F0	F10
IO07PB0F0	G10
IO08NB0F0	E9
IO08PB0F0	E8
IO09NB0F0	J11
IO09PB0F0	K11
IO10NB0F0	C8
IO10PB0F0	D8
IO11NB0F0	K12
IO11PB0F0	J12
IO12NB0F1	G11
IO12PB0F1	H11
IO13NB0F1	G12
IO13PB0F1	H12
IO14NB0F1	A7
IO14PB0F1	B7
IO15NB0F1	H13
IO15PB0F1	J13
IO16NB0F1	C9
IO16PB0F1	D9

FG1152	
AX2000 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	F11
IO18NB0F1	E11
IO18PB0F1	E10
IO19NB0F1	F13
IO19PB0F1	G13
IO20NB0F1	A10
IO20PB0F1	A9
IO21NB0F1	K14
IO21PB0F1	K13
IO22NB0F2	B11
IO22PB0F2	B10
IO23NB0F2	C12
IO23PB0F2	C11
IO24NB0F2	A12
IO24PB0F2	A11
IO25NB0F2	H14
IO25PB0F2	J14
IO26NB0F2	D13
IO26PB0F2	D12
IO27NB0F2	F14
IO27PB0F2	G14
IO28NB0F2	E14
IO28PB0F2	E13
IO29NB0F2	B13
IO29PB0F2	B12
IO30NB0F2	C14
IO30PB0F2	C13
IO31NB0F2	H15
IO31PB0F2	J15
IO32NB0F2	A14
IO32PB0F2	B14
IO33NB0F2	K15
IO33PB0F2	L15
IO34NB0F3	D15

FG1152	
AX2000 Function	Pin Number
IO34PB0F3	D14
IO35NB0F3	A15
IO35PB0F3	B15
IO36NB0F3	B16
IO36PB0F3	A16
IO37NB0F3	G16
IO37PB0F3	G15
IO38NB0F3	D16
IO38PB0F3	C16
IO39NB0F3	K16
IO39PB0F3	L16
IO40NB0F3	D17
IO40PB0F3	C17
IO41NB0F3/HCLKAN	E16
IO41PB0F3/HCLKAP	F16
IO42NB0F3/HCLKBN	G17
IO42PB0F3/HCLKBP	F17
Bank 1	
IO43NB1F4/HCLKCN	G19
IO43PB1F4/HCLKCP	G18
IO44NB1F4/HCLKDN	E19
IO44PB1F4/HCLKDP	F19
IO45NB1F4	C18
IO45PB1F4	D18
IO46NB1F4	A18
IO46PB1F4	B18
IO47NB1F4	K19
IO47PB1F4	L19
IO48NB1F4	C19
IO48PB1F4	D19
IO49NB1F4	K20
IO49PB1F4	L20
IO50NB1F4	A19
IO50PB1F4	B19
IO51NB1F4	H20

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX250 Function	**Pin Number**
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	**Pin Number**
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CQ352	
AX500 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX500 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND/LP	352
NC	91
NC	117
NC	130
NC	131
NC	148
NC	174
NC	268
NC	294
NC	307
NC	308
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349

CQ352	
AX500 Function	Pin Number
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	132
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	309

CG624	
AX2000 Function	**Pin Number**
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20*
IO85PB1F7	D19*
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17*
IO89PB2F8	G22*
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23*
IO107PB2F10	N16*
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	**Pin Number**
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*