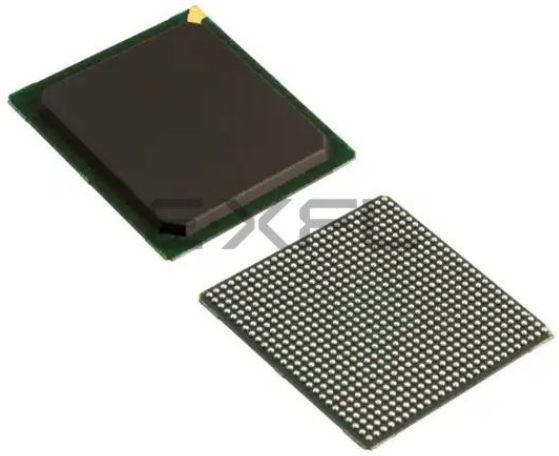

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	336
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-1fgg676

Figure 1-2 • **Axcelerator Family Interconnect Elements**

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

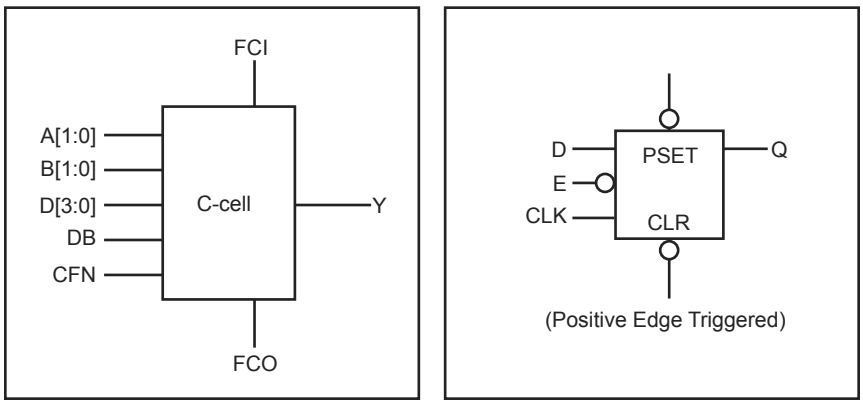

Figure 1-3 • **AX C-Cell and R-Cell**

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

User I/Os[2]

Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-8 on page 2-12 contains the I/O standards supported by the Axcelerator family, and Table 2-10 on page 2-12 compares the features of the different I/O standards.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3 V PCI and 3.3 V PCI-X, are capable of hot insertion. 3.3 V PCI and 3.3 V PCI-X are 5 V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (Figure 2-6 on page 2-18). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules:

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.
- Dedicated I/O pins such as GND and VCCI are counted as part of the 16.
- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.
- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3 V.

A user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.
- Use generic I/O macros and then use Designer's PinEditor to specify the desired I/O standards (please note that this is not applicable to differential standards).
- A combination of the first two methods.

Refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

2. *Do not use an external resister to pull the I/O above V_{CCI} for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above V_{CCI}.*

I/O Standard Electrical Specifications

***Table 2-18* • Input Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	VIN = 0, f = 1.0 MHz		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	VIN = 0, f = 1.0 MHz		10	pF

Table 2-19* • I/O Input Rise Time and Fall Time

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTL	No Requirement	50 ns
LVCMOS 2.5V	No Requirement	50 ns
LVCMOS 1.8V	No Requirement	50 ns
LVCMOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

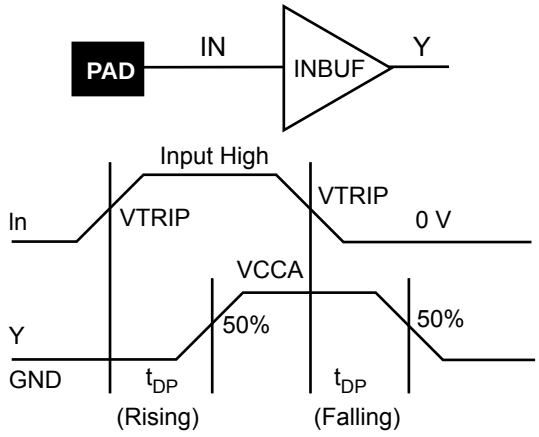

***Figure 2-9 •* Input Buffer Delays**

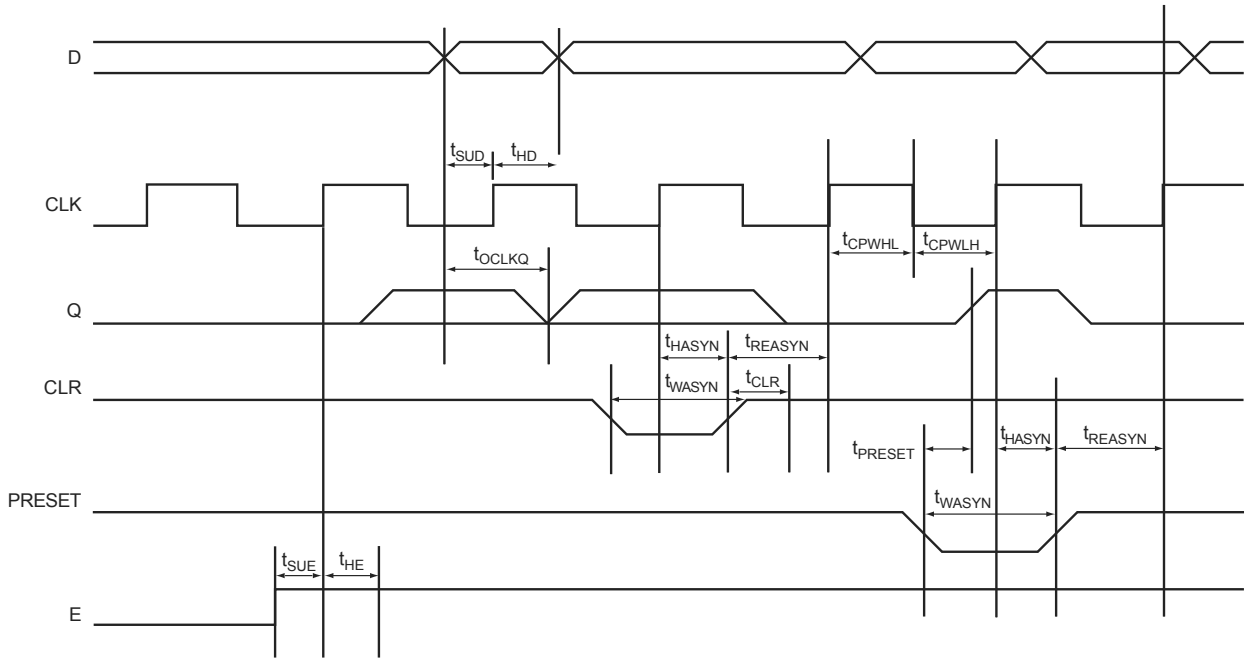

Figure 2-13 • **Output Register Timing Characteristics**

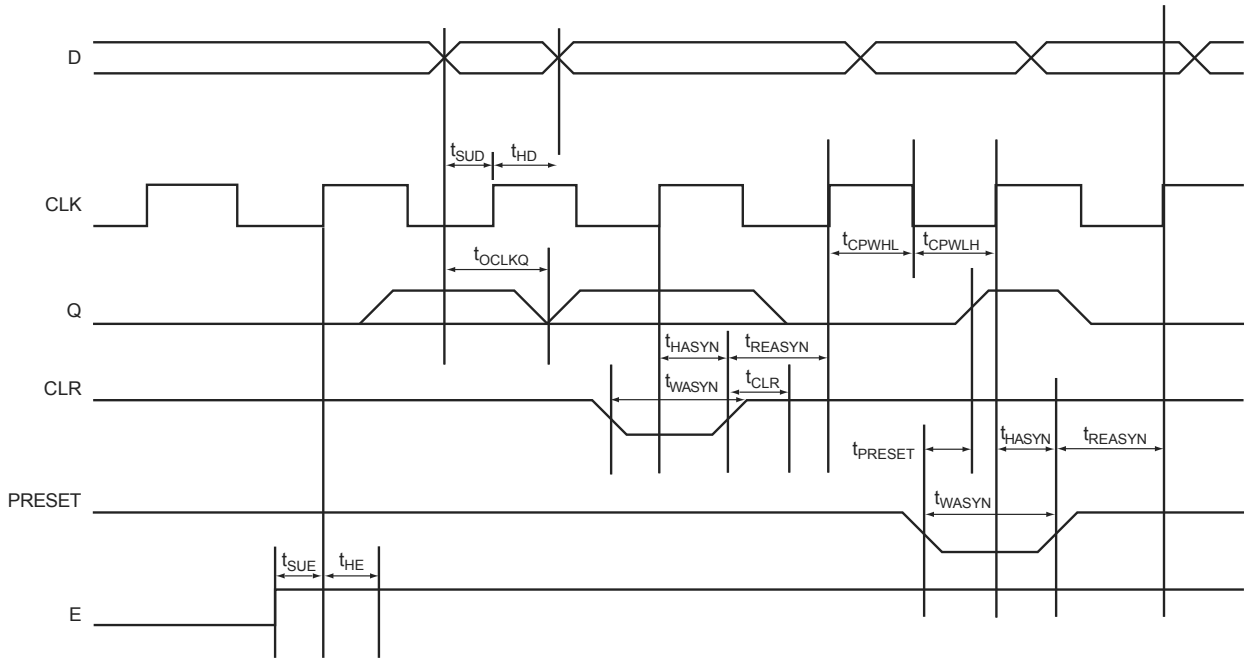

Figure 2-14 • **Output Enable Register Timing Characteristics**

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 4 (24 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		10.45		11.90		13.99	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		10.61		12.08		14.21	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		10.47		11.93		14.02	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.92		1.94		1.94	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.57		2.58		2.59	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

***Table 2-35* • 3.3 V PCI I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V PCI Output Module Timing								
t_{DP}	Input Buffer		1.57		1.79		2.10	ns
t_{PY}	Output Buffer		1.91		2.18		2.56	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

The HM and CM modules can select between:

- The HCLK or CLK source respectively
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module respectively
- A local signal routed on generic routing resources

The AX architecture is capable of supporting a large number of local clocks—24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Microsemi's Designer software's place-and-route takes advantage of the segmented clock structure found in Axcelerator devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption.

Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s), an internal net, or the output of a PLL. These connections can be made by using one of three types of macros: CLKBUF, CLKINT, and PLLCLK.

CLKBUF and HCLKBUF

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF_LVCMOS25, HCLKBUF_LVDS, etc.) (Figure 2-42).

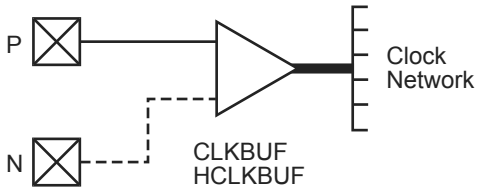

Figure 2-42 • **CLKBUF and HCLKBUF**

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

CLKINT and HCLKINT

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 2-43).

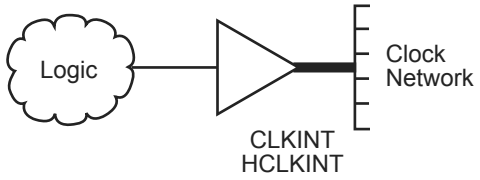

Figure 2-43 • **CLKINT and HCLKINT**

***Table 2-83* • South PLL Connections**

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).

***Table 2-91* • Four RAM Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	2.51		2.51		2.51		ns
t_{WCKP}	WCLK Minimum Period	3.26		3.26		3.26		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		3.08		3.51		4.13	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		3.08		3.51		4.13	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		2.83		3.23		3.79	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	2.96		2.96		2.96		ns
t_{RCKP}	RCLK Minimum Period	3.69		3.69		3.69		ns

Note: Timing data for these four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

BG729	
AX1000 Function	**Pin Number**
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16

BG729	
AX1000 Function	**Pin Number**
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

FG324	
AX125 Function	**Pin Number**
GND	R4
GND	T16
GND	T3
GND	U17
GND	U2
GND	V1
GND	V18
GND/LP	E5
NC	A10
NC	A11
NC	A12
NC	A13
NC	A8
NC	A9
NC	B12
NC	F15
NC	F4
NC	G15
NC	G4
NC	H14
NC	H15
NC	H5
NC	J1
NC	J14
NC	J15
NC	J5
NC	K14
NC	K15
NC	K5
NC	L14
NC	L15
NC	L5
NC	M4
NC	M5
NC	N17

FG324	
AX125 Function	**Pin Number**
NC	N4
NC	N5
NC	R12
NC	R13
NC	R6
NC	R7
NC	T12
NC	T6
NC	U16
NC	V17
PRA	E9
PRB	D9
PRC	P10
PRD	R10
TCK	E6
TDI	D7
TDO	D5
TMS	D4
TRST	D6
VCCA	E15
VCCA	G10
VCCA	G11
VCCA	G5
VCCA	G8
VCCA	G9
VCCA	H12
VCCA	H7
VCCA	J12
VCCA	J7
VCCA	K12
VCCA	K7
VCCA	L12
VCCA	L7
VCCA	M10
VCCA	M11

FG324	
AX125 Function	**Pin Number**
VCCA	M8
VCCA	M9
VCCA	P4
VCCA	R15
VCCPLA	D8
VCCPLB	E7
VCCPLC	B11
VCCPLD	E11
VCCPLE	R11
VCCPLF	P12
VCCPLG	U8
VCCPLH	P8
VCCDA	B3
VCCDA	D14
VCCDA	E10
VCCDA	J2
VCCDA	K16
VCCDA	P15
VCCDA	P9
VCCDA	R5
VCCIB0	F7
VCCIB0	F8
VCCIB0	F9
VCCIB1	F10
VCCIB1	F11
VCCIB1	F12
VCCIB2	G13
VCCIB2	H13
VCCIB2	J13
VCCIB3	K13
VCCIB3	L13
VCCIB3	M13
VCCIB4	N10
VCCIB4	N11
VCCIB4	N12

FG324	
AX125 Function	**Pin Number**
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG676	
AX1000 Function	**Pin Number**
IO197PB6F18	Y6
IO198NB6F18	AD1
IO198PB6F18	AE1
IO199NB6F18	AA2
IO199PB6F18	AB2
IO200NB6F18	Y3
IO200PB6F18	AA3
IO201NB6F18	V5
IO201PB6F18	W5
IO202NB6F18	AB1
IO202PB6F18	AC1
IO203NB6F19	V4
IO203PB6F19	W4
IO204NB6F19	V3
IO204PB6F19	W3
IO205NB6F19	U6
IO205PB6F19	V6
IO206NB6F19	W2
IO206PB6F19	Y2
IO207NB6F19	U4
IO207PB6F19	U5
IO208NB6F19	Y1
IO208PB6F19	AA1
IO209NB6F19	T6
IO209PB6F19	T7
IO211NB6F19	T3
IO211PB6F19	U3
IO212NB6F19	V1
IO212PB6F19	V2
IO213NB6F19	T5
IO213PB6F19	T4
IO214NB6F20	U1
IO214PB6F20	U2
IO215NB6F20	R6
IO215PB6F20	R7
IO217NB6F20	R5

FG676	
AX1000 Function	**Pin Number**
IO217PB6F20	R4
IO218NB6F20	R2
IO218PB6F20	T2
IO219NB6F20	P3
IO219PB6F20	R3
IO220NB6F20	R1
IO220PB6F20	T1
IO221NB6F20	P6
IO221PB6F20	P7
IO223NB6F20	P5
IO223PB6F20	P4
Bank 7	
IO225NB7F21	N5
IO225PB7F21	N4
IO226NB7F21	N2
IO226PB7F21	N3
IO227NB7F21	N6
IO227PB7F21	N7
IO229NB7F21	M7
IO229PB7F21	M6
IO231NB7F21	M5
IO231PB7F21	M4
IO232NB7F21	L1
IO232PB7F21	M1
IO233NB7F21	M2
IO233PB7F21	M3
IO235NB7F21	K2
IO235PB7F21	L2
IO236NB7F22	L5
IO236PB7F22	L4
IO237NB7F22	L6
IO237PB7F22	L7
IO238NB7F22	K3
IO238PB7F22	L3
IO240NB7F22	J1
IO240PB7F22	K1

FG676	
AX1000 Function	**Pin Number**
IO241NB7F22	K6
IO241PB7F22	K5
IO242NB7F22	H2
IO242PB7F22	J2
IO243NB7F22	J4
IO243PB7F22	K4
IO244NB7F22	H3
IO244PB7F22	J3
IO245NB7F22	G2
IO245PB7F22	G1
IO247NB7F23	J6
IO247PB7F23	J5
IO248NB7F23	E1
IO248PB7F23	F1
IO249NB7F23	E2
IO249PB7F23	F2
IO250NB7F23	G4
IO250PB7F23	H4
IO251NB7F23	F3
IO251PB7F23	G3
IO253NB7F23	H6
IO253PB7F23	H5
IO254NB7F23	D2
IO254PB7F23	D1
IO255NB7F23	E4
IO255PB7F23	F4
IO256NB7F23	D3
IO256PB7F23	E3
IO257NB7F23	F5
IO257PB7F23	G5
Dedicated I/O	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26

FG896	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	D6
IO00PB0F0	E6
IO01NB0F0	A5
IO01PB0F0	B5
IO02NB0F0	G9
IO02PB0F0	G8
IO03NB0F0	F8
IO03PB0F0	F7
IO04NB0F0	D7
IO04PB0F0	E7
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	H9
IO06PB0F0	H8
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	E9
IO08PB0F0	F9
IO09NB0F0	A7
IO09PB0F0	B7
IO10NB0F0	H10
IO10PB0F0	G10
IO11NB0F0	C9
IO11PB0F0	C8
IO12NB0F1	E10
IO12PB0F1	F10
IO13NB0F1	D10
IO13PB0F1	D9
IO14NB0F1	F11
IO14PB0F1	G11
IO15NB0F1	A10
IO15PB0F1	A9
IO16NB0F1	H12
IO16PB0F1	H11

FG896	
AX1000 Function	Pin Number
IO17NB0F1	B11
IO17PB0F1	B10
IO18NB0F1	D11
IO18PB0F1	E11
IO19NB0F1	C12
IO19PB0F1	C11
IO20NB0F1	F12
IO20PB0F1	G12
IO21NB0F1	D12
IO21PB0F1	E12
IO22NB0F2	H13
IO22PB0F2	J13
IO23NB0F2	A12
IO23PB0F2	A11
IO24NB0F2	F13
IO24PB0F2	G13
IO25NB0F2	B13
IO25PB0F2	B12
IO26NB0F2	E14
IO26PB0F2	E13
IO27NB0F2	B14
IO27PB0F2	A14
IO28NB0F2	H14
IO28PB0F2	J14
IO29NB0F2	B15
IO29PB0F2	A15
IO30NB0F2/HCLKAN	C14
IO30PB0F2/HCLKAP	D14
IO31NB0F2/HCLKBN	E15
IO31PB0F2/HCLKBP	D15
Bank 1	
IO32NB1F3/HCLKCN	E17
IO32PB1F3/HCLKCP	E16
IO33NB1F3/HCLKDN	C17
IO33PB1F3/HCLKDP	D17

FG896	
AX1000 Function	Pin Number
IO34NB1F3	A17
IO34PB1F3	B17
IO35NB1F3	D18
IO35PB1F3	C18
IO36NB1F3	H17
IO36PB1F3	J17
IO37NB1F3	B19
IO37PB1F3	A19
IO38NB1F3	H18
IO38PB1F3	J18
IO39NB1F3	B20
IO39PB1F3	A20
IO40NB1F3	C20
IO40PB1F3	C19
IO41NB1F4	E20
IO41PB1F4	E19
IO42NB1F4	F18
IO42PB1F4	G18
IO43NB1F4	A22
IO43PB1F4	A21
IO44NB1F4	F20
IO44PB1F4	F19
IO45NB1F4	D21
IO45PB1F4	D20
IO46NB1F4	D22
IO46PB1F4	C22
IO47NB1F4	A25
IO47PB1F4	A24
IO48NB1F4	H19
IO48PB1F4	G19
IO49NB1F4	C24
IO49PB1F4	C23
IO50NB1F4	G20
IO50PB1F4	H20
IO51NB1F4	F21

FG896	
AX1000 Function	Pin Number
IO206PB6F19	AB4
IO207NB6F19	W6
IO207PB6F19	W7
IO208NB6F19	AB3
IO208PB6F19	AC3
IO209NB6F19	V8
IO209PB6F19	V9
IO210NB6F19	AA2
IO210PB6F19	AA1
IO211NB6F19	V5
IO211PB6F19	W5
IO212NB6F19	Y3
IO212PB6F19	Y4
IO213NB6F19	V7
IO213PB6F19	V6
IO214NB6F20	W3
IO214PB6F20	W4
IO215NB6F20	U8
IO215PB6F20	U9
IO216NB6F20	W1
IO216PB6F20	W2
IO217NB6F20	U7
IO217PB6F20	U6
IO218NB6F20	U4
IO218PB6F20	V4
IO219NB6F20	T5
IO219PB6F20	U5
IO220NB6F20	U3
IO220PB6F20	V3
IO221NB6F20	T8
IO221PB6F20	T9
IO222NB6F20	U2
IO222PB6F20	V2
IO223NB6F20	T7
IO223PB6F20	T6

FG896	
AX1000 Function	Pin Number
IO224NB6F20	R2
IO224PB6F20	T2
Bank 7	
IO225NB7F21	R7
IO225PB7F21	R6
IO226NB7F21	R4
IO226PB7F21	R5
IO227NB7F21	R8
IO227PB7F21	R9
IO228NB7F21	P1
IO228PB7F21	R1
IO229NB7F21	P9
IO229PB7F21	P8
IO230NB7F21	N2
IO230PB7F21	P2
IO231NB7F21	P7
IO231PB7F21	P6
IO232NB7F21	N3
IO232PB7F21	P3
IO233NB7F21	P4
IO233PB7F21	P5
IO234NB7F21	L1
IO234PB7F21	M1
IO235NB7F21	M4
IO235PB7F21	N4
IO236NB7F22	N7
IO236PB7F22	N6
IO237NB7F22	N8
IO237PB7F22	N9
IO238NB7F22	M5
IO238PB7F22	N5
IO239NB7F22	L2
IO239PB7F22	M2
IO240NB7F22	L3
IO240PB7F22	M3

FG896	
AX1000 Function	Pin Number
IO241NB7F22	M8
IO241PB7F22	M7
IO242NB7F22	K4
IO242PB7F22	L4
IO243NB7F22	L6
IO243PB7F22	M6
IO244NB7F22	K5
IO244PB7F22	L5
IO245NB7F22	J4
IO245PB7F22	J3
IO246NB7F22	G2
IO246PB7F22	H2
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	G3
IO248PB7F23	H3
IO249NB7F23	G4
IO249PB7F23	H4
IO250NB7F23	J6
IO250PB7F23	K6
IO251NB7F23	H5
IO251PB7F23	J5
IO252NB7F23	F2
IO252PB7F23	F1
IO253NB7F23	K8
IO253PB7F23	K7
IO254NB7F23	F4
IO254PB7F23	F3
IO255NB7F23	G6
IO255PB7F23	H6
IO256NB7F23	F5
IO256PB7F23	G5
IO257NB7F23	H7
IO257PB7F23	J7
Dedicated I/O	

FG1152	
AX2000 Function	Pin Number
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H31
NC	H33
NC	J1
NC	J3
NC	J34
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17

FG1152	
AX2000 Function	Pin Number
PRB	F18
PRC	AD18
PRD	AH18
TCK	J9
TDI	F7
TDO	L10
TMS	H8
TRST	E6
VCCA	AA13
VCCA	AA22
VCCA	AB14
VCCA	AB15
VCCA	AB16
VCCA	AB17
VCCA	AB18
VCCA	AB19
VCCA	AB20
VCCA	AB21
VCCA	AF8
VCCA	AK28
VCCA	G30
VCCA	G5
VCCA	N14
VCCA	N15
VCCA	N16
VCCA	N17
VCCA	N18
VCCA	N19
VCCA	N20
VCCA	N21
VCCA	P13
VCCA	P22
VCCA	R13
VCCA	R22
VCCA	T13

FG1152	
AX2000 Function	Pin Number
VCCA	T22
VCCA	U13
VCCA	U22
VCCA	V13
VCCA	V22
VCCA	W13
VCCA	W22
VCCA	Y13
VCCA	Y22
VCCDA	AF26
VCCDA	AF9
VCCDA	AG17
VCCDA	AG18
VCCDA	AH14
VCCDA	AH15
VCCDA	AH17
VCCDA	AH20
VCCDA	AH21
VCCDA	AK29
VCCDA	AK6
VCCDA	E15
VCCDA	E29
VCCDA	E7
VCCDA	F15
VCCDA	F21
VCCDA	F5
VCCDA	G20
VCCDA	H17
VCCDA	H18
VCCDA	H28
VCCDA	J18
VCCDA	V27
VCCDA	V6
VCCIB0	A5
VCCIB0	B5

CQ352	
AX1000 Function	Pin Number
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234

CQ352	
AX1000 Function	Pin Number
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
NC	91
NC	130
NC	131
NC	174
NC	268
NC	307
NC	308
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3

CQ352	
AX1000 Function	Pin Number
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	117
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	294
VCCDA	309
VCCDA	327
VCCDA	328

Revision	Changes	Page
Revision 12 (v2.4)	Revised ordering information and timing data to reflect phase out of –3 speed grade options.	
	Table 2-3 was updated.	2
Revision 11 (v2.3)	The "Packaging Data" section is new.	iv
	Table 2-2 was updated.	2-1
	"VCCDA Supply Voltage" was updated.	2-9
	"PRA/B/C/D Probe A, B, C and D" was updated.	2-10
	The "User I/Os" was updated.	2-11
Revision 10 (v2.2)	Figure 1-3 was updated.	1-2
	Table 2-2 was updated.	2-1
	The "Power-Up/Down Sequence" section was updated.	2-1
	Table 2-4 was updated.	2-3
	Table 2-5 was updated.	2-4
	The "Timing Characteristics" section was added.	2-7
	Table 2-7 was updated.	2-7
	Figure 2-1 was updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) equations in the "Hardwired Clock – Using LVTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) in the "Routed Clock – Using LVTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The "Global Pins" section was updated.	2-10
	The "User I/Os" section was updated.	2-11
	Table 2-17 was updated.	2-19
	Figure 2-8 was updated.	2-20
	Figure 2-13 and Figure 2-14 were updated.	2-24
	The following timing parameters were renamed in I/O timing characteristic tables from Table 2-22 to Table 2-60: $t_{IOCLKQ} > t_{ICLKQ}$ $t_{IOCLKY} > t_{OCLKQ}$	2-26 to 2-52
	Timing numbers were updated from Table 2-22 to Table 2-78.	2-26 to 2-69
	The "R-Cell" section was updated.	2-58
	Figure 2-59 was updated.	2-89
	Figure 2-60 was updated.	2-89
	Figure 2-67 was updated.	2-100
	Figure 2-68 was updated.	2-101
	Table 2-89 to Table 2-93 were updated.	2-90 to 2-94
	Table 2-98 to Table 2-102 were updated.	2-102 to 2-106

Revision	Changes	Page
Revision 10 (continued)	The "TRST" section was updated.	2-107
	The "Global Set Fuse" section was added.	2-109
	A footnote was added to "FG896" for the AX2000 regarding pins AB1, AE2, G1, and K2.	3-52
	Pinouts for the AX250, AX500, and AX1000 were added for "CQ352".	3-98
	Pinout for the AX1000 was added for "CG624".	3-115
Revision 9 (v2.1)	Table 2-79 was updated.	2-69
	The "Low Power Mode" section was updated.	2-106
Revision 8 (v2.0)	Table 1 has been updated.	i
	The "Ordering Information" section has been updated.	ii
	The "Device Resources" section has been updated.	ii
	The "Temperature Grade Offerings" section is new.	iii
	The "Speed Grade and Temperature Grade Matrix" section has been updated.	iii
	Table 2-9 has been updated.	2-12
	Table 2-10 has been updated.	2-12
	Table 2-1 has been updated.	2-1
	Table 2-2 has been updated.	2-1
	Table 2-3 has been updated.	2-2
	Table 2-4 has been updated.	2-3
	Table 2-5 has been updated.	2-4
	The "Power Estimation Example" section has been updated.	2-5
	The "Thermal Characteristics" section has been updated.	2-6
	The "Package Thermal Characteristics" section has been updated.	2-6
	The "Timing Characteristics" section has been updated.	2-7
	The "Pin Descriptions" section has been updated.	2-9
	Timing numbers have been updated from the "3.3 V LVTTL" section to the "Timing Characteristics" section. Many AC Loads were updated as well.	2-25 to 2-59
	Timing characteristics for the "Hardwired Clocks" and "Routed Clocks" sections were updated.	2-66, 2-68
	Table 2-89 to Table 2-92 and Table 2-98 to Table 2-99 were updated.	2-90 to 2-93, 2-102 to 2-103
	The following sections were updated: "Low Power Mode", "Interface", "Data Registers (DRs)", "Security", "Silicon Explorer II Probe Interface", and "Programming"	2-106 to 2-110
	In the "PQ208" (AX500) section, pins 2, 52, and 156 changed from V_{CCDA} to V_{CCA}. For pins 170 and 171, the I/O names refer to pair 23 instead of 24.	3-84