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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	115
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-1pqg208

Figure 1-2 • **Axcelerator Family Interconnect Elements**

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

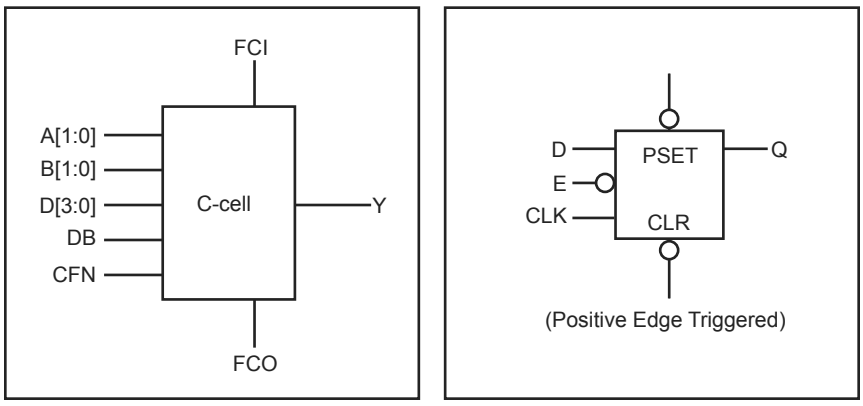


Figure 1-3 • **AX C-Cell and R-Cell**

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

I/O Standard Electrical Specifications

***Table 2-18* • Input Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	VIN = 0, f = 1.0 MHz		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	VIN = 0, f = 1.0 MHz		10	pF

Table 2-19* • I/O Input Rise Time and Fall Time

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTL	No Requirement	50 ns
LVCMOS 2.5V	No Requirement	50 ns
LVCMOS 1.8V	No Requirement	50 ns
LVCMOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

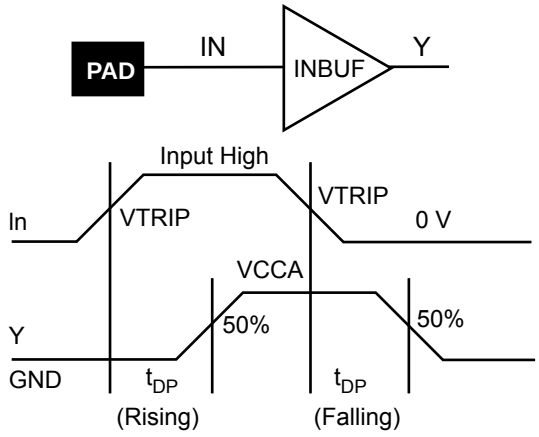


***Figure 2-9 •* Input Buffer Delays**

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength =3 (16 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		11.03		12.56		14.77	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		11.42		13.01		15.29	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		11.04		12.58		14.79	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.86		1.88		1.88	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.50		2.51		2.52	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Differential Standards

Physical Implementation

Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O Cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350 mV.

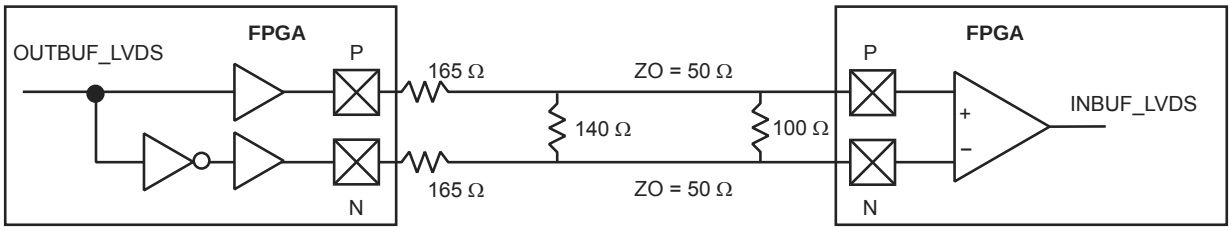


Figure 2-25 • **LVDS Board-Level Implementation**

The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2 V to 2.2 V for a differential input with 400 mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (note that the driver is not a current-mode driver). This driver provides a nominal constant current of 3.5 mA. When this current flows through a 100 Ω termination resistor on the receiver side, a voltage swing of 350 mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350 mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

Table 2-56 • **DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI[1]	Supply Voltage	2.375	2.5	2.625	V
VOH	Output High Voltage	1.25	1.425	1.6	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM2	Input Common Mode Voltage	0.2	1.25	2.2	V

Notes:

1. *±5%*
2. *Differential input voltage = ±350 mV.*

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t_{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t_{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t_{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t_{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t_{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t_{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t_{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t_{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t_{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-38).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-39).

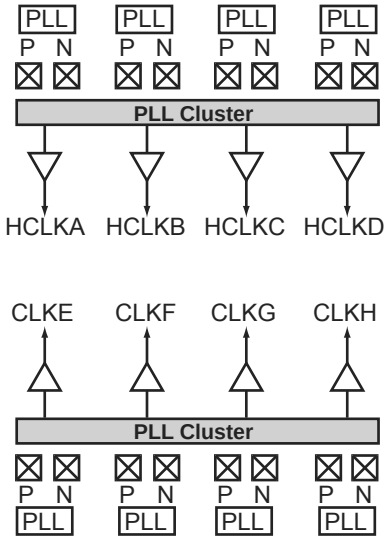


Figure 2-38 • **PLL Group**

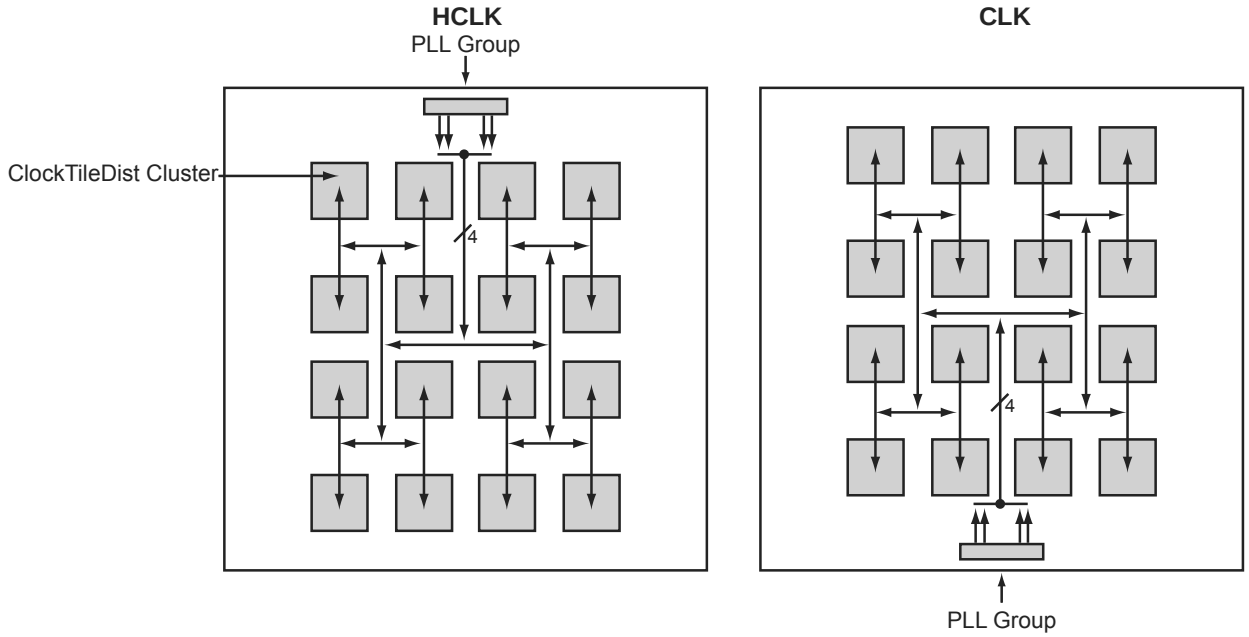


Figure 2-39 • **Example of HCLK and CLK Distributions on the AX2000**

PLL Configurations

The following rules apply to the different PLL inputs and outputs:

Reference Clock

The RefCLK can be driven by (Figure 2-50):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. CLK1 output of an adjacent PLL
3. [H]CLKxP (single-ended or voltage-referenced)
4. [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Feedback Clock

The feedback clock can be driven by (Figure 2-51 on page 2-78):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
3. An internal signal from the PLL block

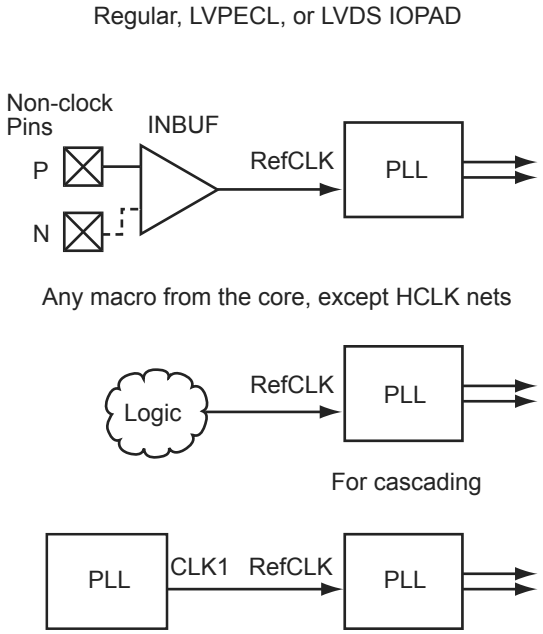


Figure 2-50 • **Reference Clock Connections**

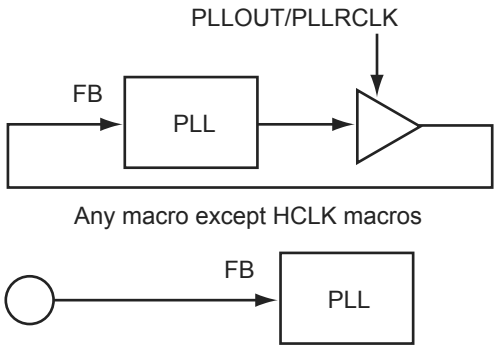


Figure 2-51 • **Feedback Clock Connections**

Embedded Memory

The AX architecture provides extensive, high-speed memory resources to the user. Each 4,608 bit block of RAM contains its own embedded FIFO controller, allowing the user to configure each block as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate in synchronous mode for both read and write operations. However, the read and write clocks are completely independent, and each may operate up to and above 500 MHz.

No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The AX memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in Figure 2-57.

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

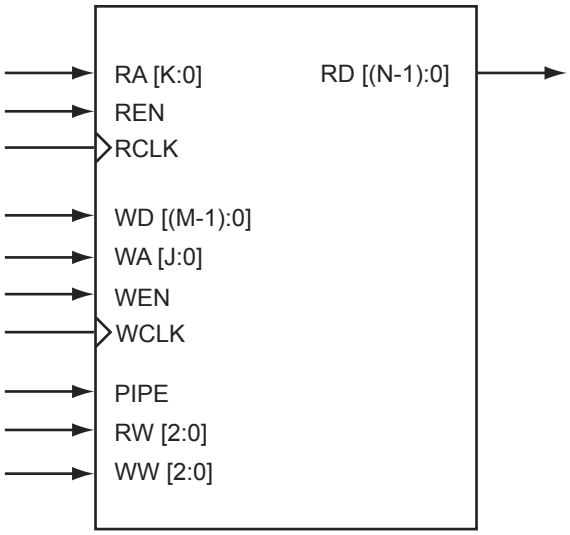


Figure 2-57 • **Axcelerator Memory Module**

***Table 2-92* • Eight RAM Blocks Cascaded**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		5.78		6.58		7.74	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		5.78		6.58		7.74	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		5.78		6.58		7.74	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	5.13		5.13		5.13		ns
t_{WCKP}	WCLK Minimum Period	5.88		5.88		5.88		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		6.75		7.69		9.04	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		6.75		7.69		9.04	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		3.39		3.86		4.54	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		4.93		5.62		6.61	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	5.77		5.77		5.77		ns
t_{RCKP}	RCLK Minimum Period	6.50		6.50		6.50		ns

Note: Timing data for these eight cascaded RAM blocks uses a depth of 32,768. For all other combinations, use Microsemi's timing software.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

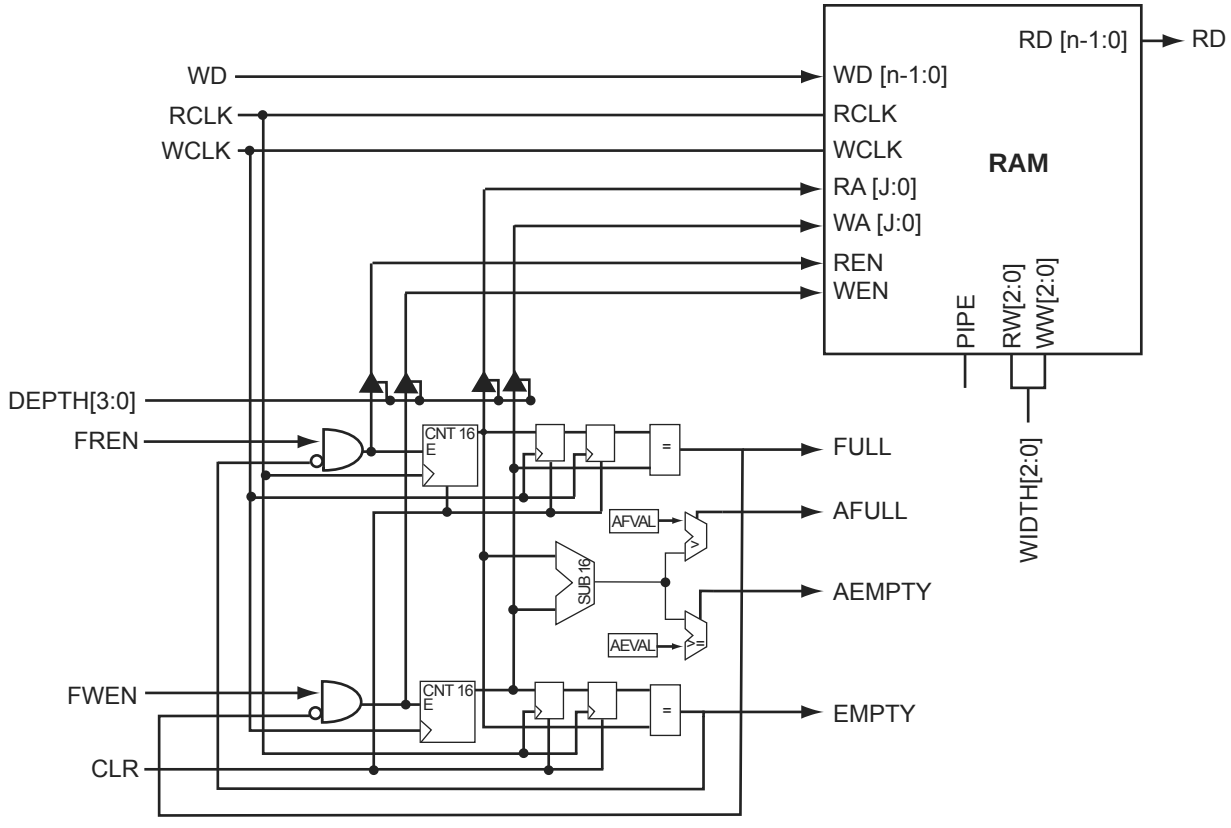


Figure 2-61 • **Axcelerator RAM with Embedded FIFO Controller**

BG729	
AX1000 Function	Pin Number
GND	B27
GND	B3
GND	C1
GND	C2
GND	C25
GND	C26
GND	C27
GND	C3
GND	E27
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17

BG729	
AX1000 Function	Pin Number
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND/LP	J8
NC	U3
PRA	J14
PRB	D14
PRC	V14
PRD	AB14
TCK	E4
TDI	D4
TDO	J9
TMS	H8
TRST	E3
VCCA	AA21
VCCA	AD5
VCCA	E1
VCCA	G22
VCCA	K10

BG729	
AX1000 Function	Pin Number
VCCA	K11
VCCA	K17
VCCA	K18
VCCA	L10
VCCA	L18
VCCA	U10
VCCA	U18
VCCA	V10
VCCA	V11
VCCA	V17
VCCA	V18
VCCPLA	A13
VCCPLB	J13
VCCPLC	B15
VCCPLD	C15
VCCPLE	AG14
VCCPLF	AF14
VCCPLG	AB13
VCCPLH	AG13
VCCDA	A11
VCCDA	AB12
VCCDA	AC12
VCCDA	AC25
VCCDA	AD16
VCCDA	AD17
VCCDA	E16
VCCDA	E2
VCCDA	E24
VCCDA	F12
VCCDA	F16
VCCDA	F7
VCCDA	K14
VCCDA	P10
VCCDA	P18
VCCDA	W14
VCCDA	W9
VCCIB0	A4

FG256-Pin FBGA	
AX125 Function	**Pin Number**
Bank 0	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO04NB0F0	B6
IO04PB0F0	B5
IO06NB0F0	A6
IO06PB0F0	A5
IO07NB0F0/HCLKAN	B8
IO07PB0F0/HCLKAP	B7
IO08NB0F0/HCLKBN	A9
IO08PB0F0/HCLKBP	A8
Bank 1	
IO09NB1F1/HCLKCN	C10
IO09PB1F1/HCLKCP	C9
IO10NB1F1/HCLKDN	B11
IO10PB1F1/HCLKDP	B10
IO12NB1F1	A13
IO12PB1F1	A12
IO13NB1F1	B13
IO13PB1F1	B12
IO14NB1F1	C12
IO14PB1F1	C11
IO15NB1F1	A15
IO15PB1F1	B14
IO16NB1F1	C15
IO16PB1F1	C14
IO17NB1F1	D13
IO17PB1F1	D12
Bank 2	
IO18NB2F2	F13
IO18PB2F2	E13
IO19NB2F2	F14
IO19PB2F2	E14

FG256-Pin FBGA	
AX125 Function	**Pin Number**
IO20NB2F2	F15
IO20PB2F2	E15
IO21NB2F2	C16
IO21PB2F2	B16
IO22NB2F2	H13
IO22PB2F2	G13
IO23NB2F2	E16
IO23PB2F2	D16
IO25NB2F2	H15
IO25PB2F2	G15
IO26NB2F2	H14
IO26PB2F2	G14
IO27NB2F2	G16
IO27PB2F2	F16
IO28NB2F2	K15
IO28PB2F2	K16
IO29NB2F2	J16
IO29PB2F2	H16
Bank 3	
IO30NB3F3	K13
IO30PB3F3	J13
IO31NB3F3	K14
IO31PB3F3	J14
IO33NB3F3	L15
IO33PB3F3	L16
IO35NB3F3	P16
IO35PB3F3	N16
IO36PB3F3	M16
IO37NB3F3	P15
IO37PB3F3	R16
IO39NB3F3	N15
IO39PB3F3	M15
IO40NB3F3	M13
IO40PB3F3	L13
IO41NB3F3	M14

FG256-Pin FBGA	
AX125 Function	**Pin Number**
IO41PB3F3	L14
Bank 4	
IO42NB4F4	N12
IO42PB4F4	N13
IO43NB4F4	T14
IO43PB4F4	R14
IO44PB4F4	T15
IO45NB4F4	R12
IO45PB4F4	R13
IO46NB4F4	P11
IO46PB4F4	P12
IO47PB4F4	T11
IO48NB4F4	T12
IO48PB4F4	T13
IO49NB4F4/CLKEN	R9
IO49PB4F4/CLKEP	R10
IO50NB4F4/CLKFN	T8
IO50PB4F4/CLKFP	T9
Bank 5	
IO51NB5F5/CLKGN	P7
IO51PB5F5/CLKGP	P8
IO52NB5F5/CLKHN	R6
IO52PB5F5/CLKHP	R7
IO54NB5F5	T5
IO54PB5F5	T6
IO55NB5F5	P5
IO55PB5F5	P6
IO56NB5F5	T3
IO56PB5F5	T4
IO57NB5F5	R3
IO57PB5F5	R4
IO58NB5F5	R1
IO58PB5F5	T2
IO59NB5F5	N4
IO59PB5F5	N5

FG256	
AX250 Function	Pin Number
Bank 0	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO05NB0F0	B6
IO05PB0F0	B5
IO07NB0F0	A6
IO07PB0F0	A5
IO12NB0F0/HCLKAN	B8
IO12PB0F0/HCLKAP	B7
IO13NB0F0/HCLKBN	A9
IO13PB0F0/HCLKBP	A8
Bank 1	
IO14NB1F1/HCLKCN	C10
IO14PB1F1/HCLKCP	C9
IO15NB1F1/HCLKDN	B11
IO15PB1F1/HCLKDP	B10
IO17NB1F1	A13
IO17PB1F1	A12
IO19NB1F1	B13
IO19PB1F1	B12
IO21NB1F1	C12
IO21PB1F1	C11
IO23NB1F1	A15
IO23PB1F1	B14
IO26NB1F1	C15
IO26PB1F1	C14
IO27NB1F1	D13
IO27PB1F1	D12
Bank 2	
IO29NB2F2	F13
IO29PB2F2	E13
IO30NB2F2	F14
IO30PB2F2	E14

FG256	
AX250 Function	Pin Number
IO32NB2F2	C16
IO32PB2F2	B16
IO33NB2F2	F15
IO33PB2F2	E15
IO35NB2F2	H13
IO35PB2F2	G13
IO36NB2F2	E16
IO36PB2F2	D16
IO38NB2F2	H15
IO38PB2F2	G15
IO39NB2F2	H14
IO39PB2F2	G14
IO40NB2F2	G16
IO40PB2F2	F16
IO43NB2F2	K15
IO43PB2F2	K16
IO44NB2F2	J16
IO44PB2F2	H16
Bank 3	
IO45NB3F3	K13
IO45PB3F3	J13
IO46NB3F3	K14
IO46PB3F3	J14
IO52NB3F3	L15
IO52PB3F3	L16
IO54NB3F3	P16
IO54PB3F3	N16
IO55PB3F3	M16
IO56NB3F3	P15
IO56PB3F3	R16
IO58NB3F3	N15
IO58PB3F3	M15
IO59NB3F3	M13
IO59PB3F3	L13
IO61NB3F3	M14

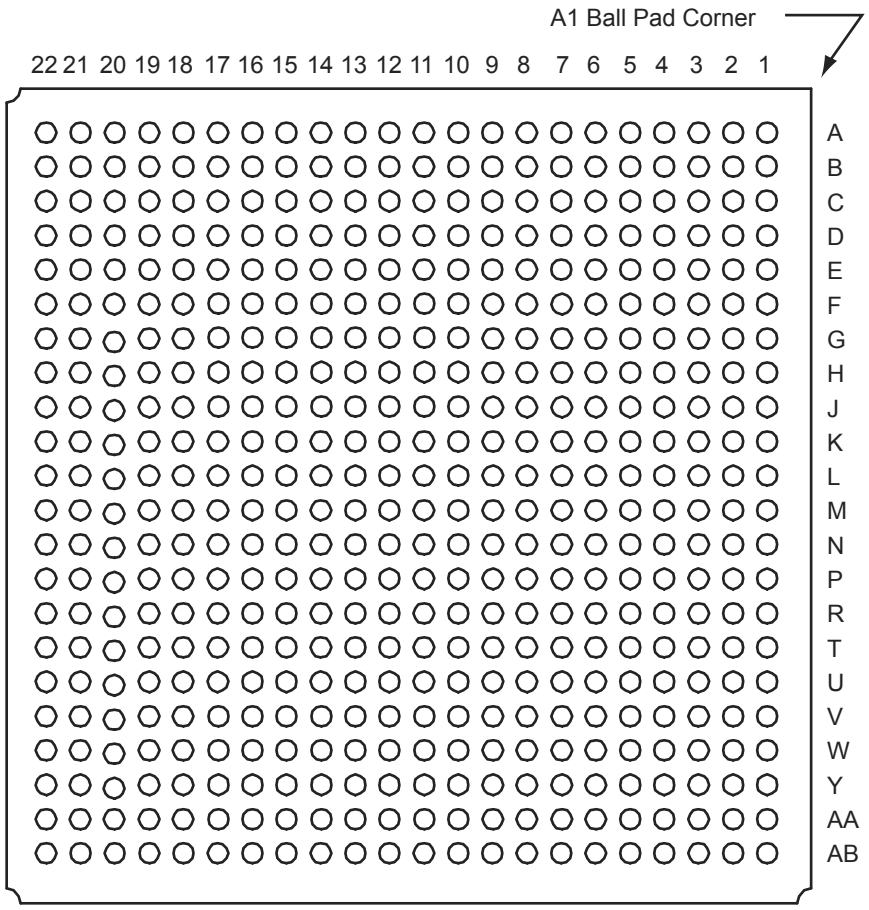
FG256	
AX250 Function	Pin Number
IO61PB3F3	L14
Bank 4	
IO62NB4F4	N12
IO62PB4F4	N13
IO63NB4F4	T14
IO63PB4F4	R14
IO66PB4F4	T15
IO67NB4F4	R12
IO67PB4F4	R13
IO69NB4F4	P11
IO69PB4F4	P12
IO70PB4F4	T11
IO73NB4F4	T12
IO73PB4F4	T13
IO74NB4F4/CLKEN	R9
IO74PB4F4/CLKEP	R10
IO75NB4F4/CLKFN	T8
IO75PB4F4/CLKFP	T9
Bank 5	
IO76NB5F5/CLKGN	P7
IO76PB5F5/CLKGP	P8
IO77NB5F5/CLKHN	R6
IO77PB5F5/CLKHP	R7
IO79NB5F5	T5
IO79PB5F5	T6
IO81NB5F5	P5
IO81PB5F5	P6
IO83NB5F5	T3
IO83PB5F5	T4
IO85NB5F5	R3
IO85PB5F5	R4
IO88NB5F5	R1
IO88PB5F5	T2
IO89NB5F5	N4
IO89PB5F5	N5

FG324	
AX125 Function	**Pin Number**
GND	R4
GND	T16
GND	T3
GND	U17
GND	U2
GND	V1
GND	V18
GND/LP	E5
NC	A10
NC	A11
NC	A12
NC	A13
NC	A8
NC	A9
NC	B12
NC	F15
NC	F4
NC	G15
NC	G4
NC	H14
NC	H15
NC	H5
NC	J1
NC	J14
NC	J15
NC	J5
NC	K14
NC	K15
NC	K5
NC	L14
NC	L15
NC	L5
NC	M4
NC	M5
NC	N17

FG324	
AX125 Function	**Pin Number**
NC	N4
NC	N5
NC	R12
NC	R13
NC	R6
NC	R7
NC	T12
NC	T6
NC	U16
NC	V17
PRA	E9
PRB	D9
PRC	P10
PRD	R10
TCK	E6
TDI	D7
TDO	D5
TMS	D4
TRST	D6
VCCA	E15
VCCA	G10
VCCA	G11
VCCA	G5
VCCA	G8
VCCA	G9
VCCA	H12
VCCA	H7
VCCA	J12
VCCA	J7
VCCA	K12
VCCA	K7
VCCA	L12
VCCA	L7
VCCA	M10
VCCA	M11

FG324	
AX125 Function	**Pin Number**
VCCA	M8
VCCA	M9
VCCA	P4
VCCA	R15
VCCPLA	D8
VCCPLB	E7
VCCPLC	B11
VCCPLD	E11
VCCPLE	R11
VCCPLF	P12
VCCPLG	U8
VCCPLH	P8
VCCDA	B3
VCCDA	D14
VCCDA	E10
VCCDA	J2
VCCDA	K16
VCCDA	P15
VCCDA	P9
VCCDA	R5
VCCIB0	F7
VCCIB0	F8
VCCIB0	F9
VCCIB1	F10
VCCIB1	F11
VCCIB1	F12
VCCIB2	G13
VCCIB2	H13
VCCIB2	J13
VCCIB3	K13
VCCIB3	L13
VCCIB3	M13
VCCIB4	N10
VCCIB4	N11
VCCIB4	N12

FG484



Note

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FG896	
AX1000 Function	Pin Number
NC	K1
NC	K2
NC	L30
NC	M30
NC	N29
NC	T1
NC	U1
NC	W30
NC	Y1
NC	Y2
NC	Y30
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11

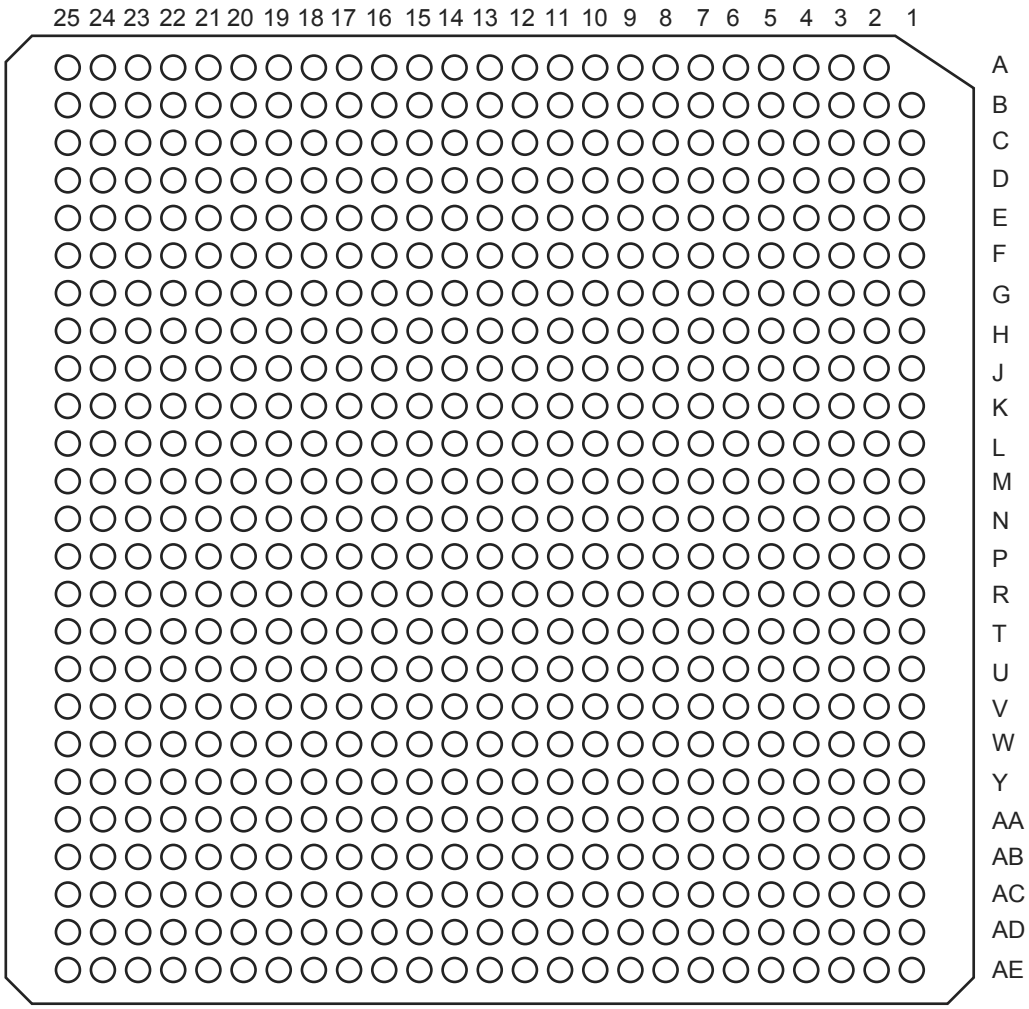
FG896	
AX1000 Function	Pin Number
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCCDA	AD24
VCCDA	AD7
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18

FG896	
AX1000 Function	Pin Number
VCCDA	AF19
VCCDA	C13
VCCDA	C5
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F26
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21

CQ352	
AX1000 Function	**Pin Number**
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX1000 Function	**Pin Number**
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CG624



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Revision	Changes	Page
Revision 17 (continued)	The C180 package was removed from product tables and the "Package Pin Assignments" section (PDN 0909).	3-1
	Package names used in the"Axcelerator Family Product Profile" and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	i, 3-1
	The "Introduction" section for "User I/Os" was updated as follows: "The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os" (SARs 24181, 24309).	2-11
	Power values in Table 2-4 • Default CLOAD/VCCI were updated to reflect those of SmartPower (SAR 33945).	2-3
	Two parameter names were corrected in Figure 2-10 • Output Buffer Delays. One occurrence of t_{ENLZ} was changed to t_{ENZL} and one occurrence of t_{ENHZ} was changed to t_{ENZH} (SAR 33890).	2-22
	The "Timing Model" section was updated with new timing values. Timing tables in the "I/O Specifications" section were updated to include enable paths. Values in the timing tables in the "Voltage-Referenced I/O Standards" section and "Differential Standards" section were updated. Table 2-63 • R-Cell was updated (SAR 33945).	2-8, 2-26 to 2-53
	Figure 2-11 • Timing Model was replaced (SAR 33043).	2-23
	The timing tables for "RAM" and "FIFO" were updated (SAR 33945).	2-90 to 2-106
	"Data Registers (DRs)" values were modified for IDCODE and USERCODE (SARs 18257, 26406).	2-108
	The package diagram for the "CQ208" package was incorrect and has been replaced with the correct diagram (SARs 23865, 26345).	3-89
Revision 16 (v2.8, Oct. 2009)	The datasheet was updated to include AX2000-CQ2526 information.	N/A
	MIL-STD-883 Class B is no longer supported by Axcelerator FPGAs and as a result was removed.	N/A
	A footnote was added to the "Introduction" in the "Axcelerator Clock Management System" section.	2-75
Revision 15 (v2.7, Nov. 2008)	RoHS-compliant information was added to the "Ordering Information".	ii
	ACTgen was changed to SmartGen because ACTgen is obsolete.	N/A
Revision 14 (v2.6)	In Table 2-4, the units for the P_{LOAD}, P_{10}, and $P_{I/O}$ were updated from mW/MHz to mW/MHz.	2-3
	In the "Pin Descriptions"section, the HCLK and CLK descriptions were updated to include tie-off information.	2-9
	The "Global Resource Distribution" section was updated.	2-70
	The " CG624" table was updated.	3-116
Revision 13 (v2.5)	A note was added to Table 2-2.	2-1
	In the "Package Thermal Characteristics", the temperature was changed from 150°C to 125°C.	2-6