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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	115
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-1pqg208m

1 – General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microsemi AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

Device Architecture

AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

The very nature of Microsemi's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-108).

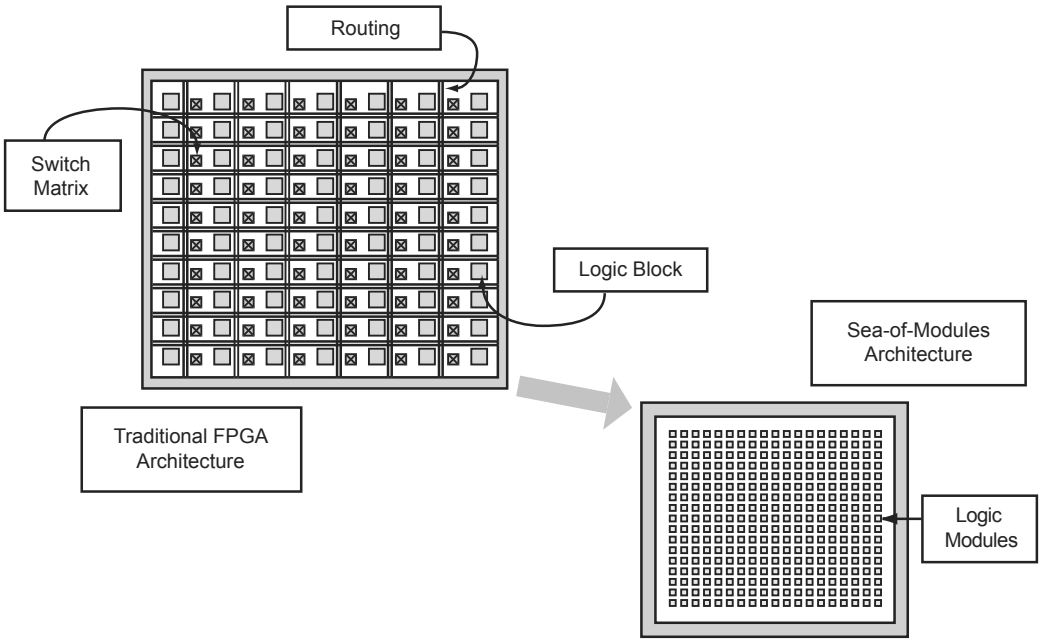


Figure 1-1 • **Sea-of-Modules Comparison**

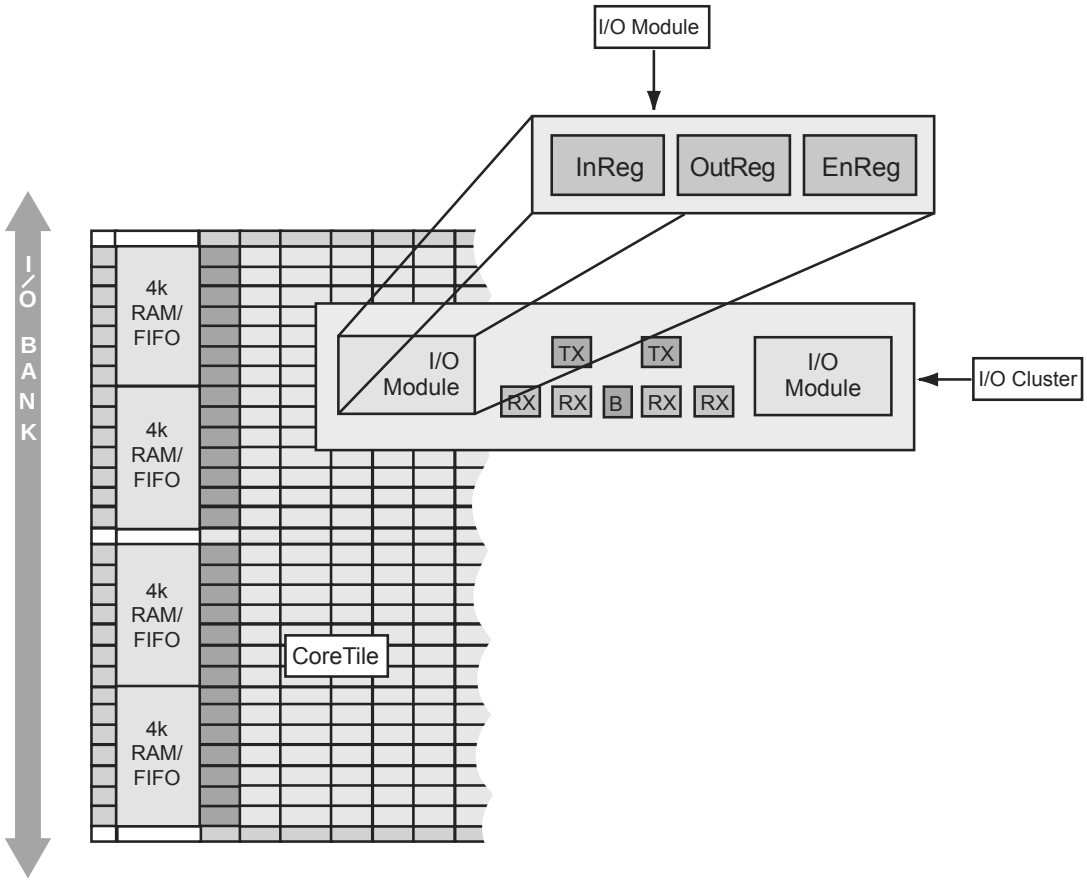


Figure 1-7 • **I/O Cluster Arrangement**

Routing

The AX hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together (Figure 1-8 on page 1-6). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

FastConnects provide high-performance, horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the FCO output of one two-bit, C-cell carry logic to the FCI input of the two-bit, C-cell carry logic of the SuperCluster below it. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. Over the SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns, respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north-to-south and east-to-west. These tracks are composed of highway routing that extend the entire length of the device (segmented at core tile boundaries) as well as segmented routing of varying lengths.

Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 kΩ). These are weak transistors with the gates tied on, so the on resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors; they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8 mA, 12 mA, 16 mA, or 24 mA – that can be specified in Designer.[5]

Table 2-14 • **Bank-Wide Delay Values**

Bits Setting	Delay (ns)	Bits Setting	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

5. *These values are minimum drive strengths.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, –3.5 V in undershoot, and 7.1 V in overshoot.

***Table 2-33* • DC Input and Output Levels**

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
PCI	–0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	–0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

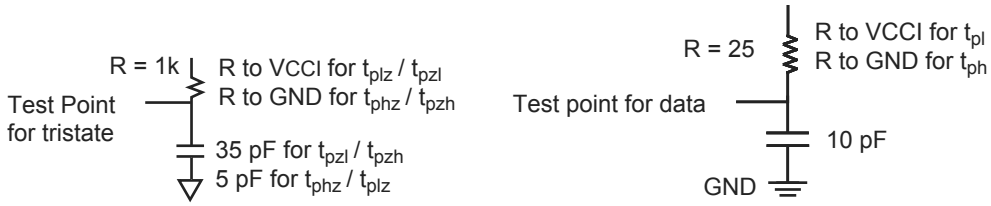


***Figure 2-18 •* AC Test Loads**

***Table 2-34* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

*Note: * Measuring Point = VTRIP*

***Table 2-57* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.2 – 0.125	1.2 + 0.125	1.2

*Note: * Measuring Point = VTRIP*

Timing Characteristics

***Table 2-58* • LVDS I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVDS Output Module Timing								
t_{DP}	Input Buffer		1.80		2.05		2.41	ns
t_{PY}	Output Buffer		2.32		2.64		3.11	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

***Table 2-83* • South PLL Connections**

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g., CLK1 driving both CLK1 and CLK2 is not supported).

Sample Implementations

Frequency Synthesis

Figure 2-53 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 2-54 illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

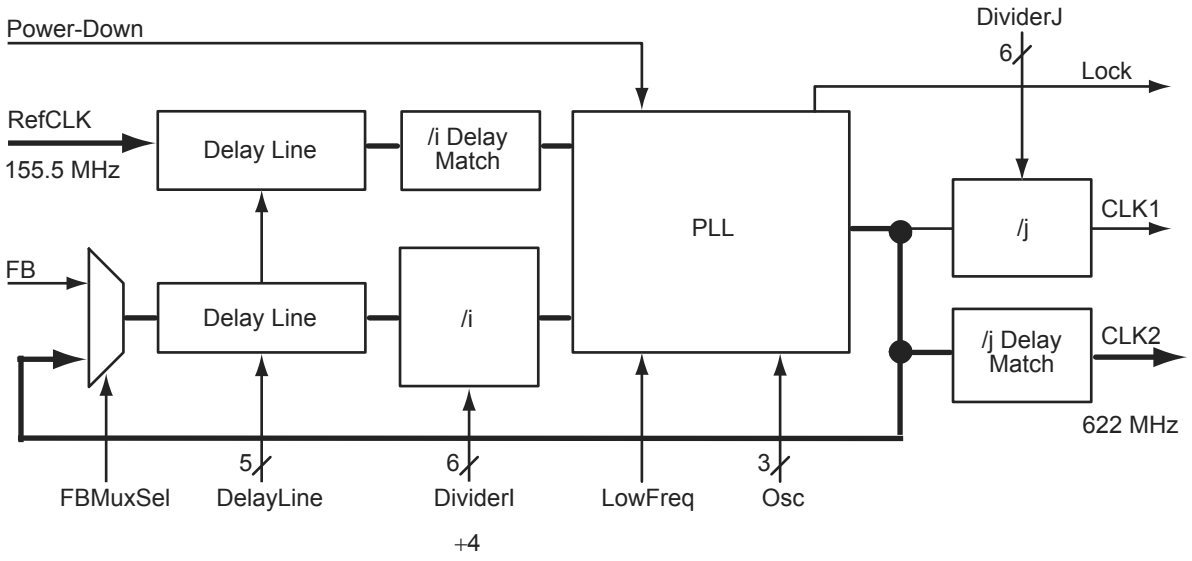


Figure 2-53 • **Using the PLL 155.5 MHz In, 622 MHz Out**

Adjustable Clock Delay

Figure 2-55 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

Clock Skew Minimization

Figure 2-56 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to the *Axcelerator Family PLL and Clock Management* application note for more information.

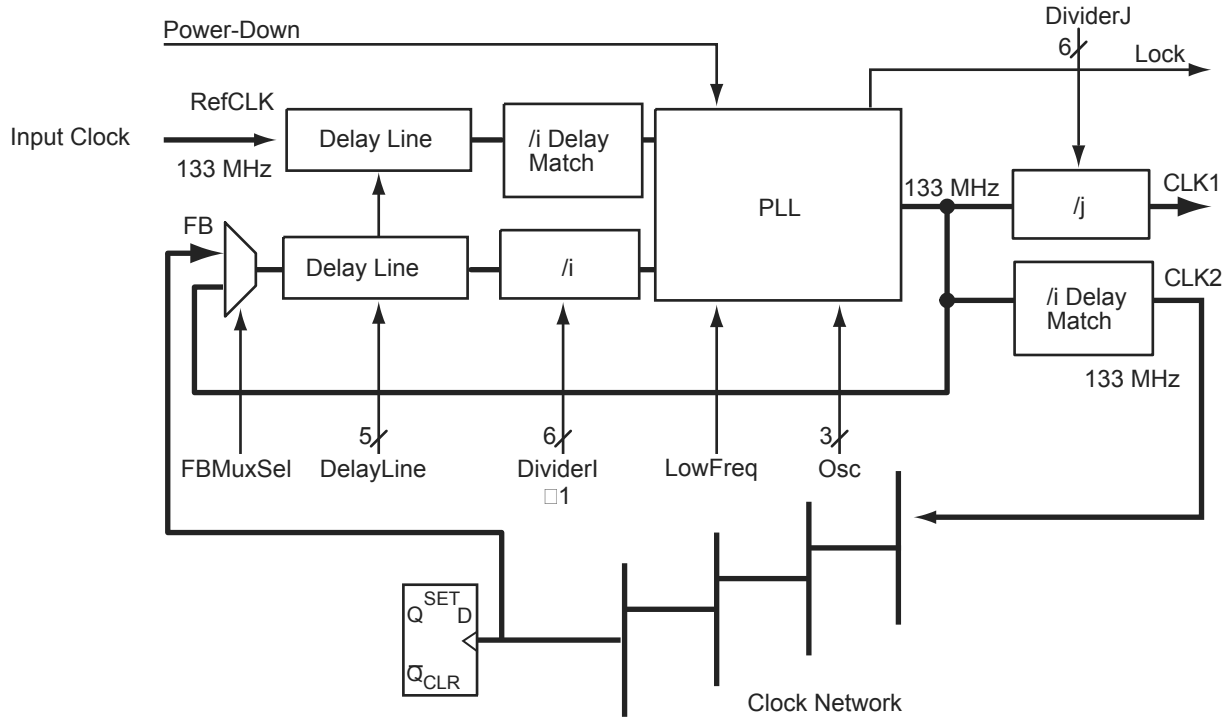


Figure 2-56 • **Using the PLL for Clock Deskewing**

Figure 2-63 illustrates flag generation.

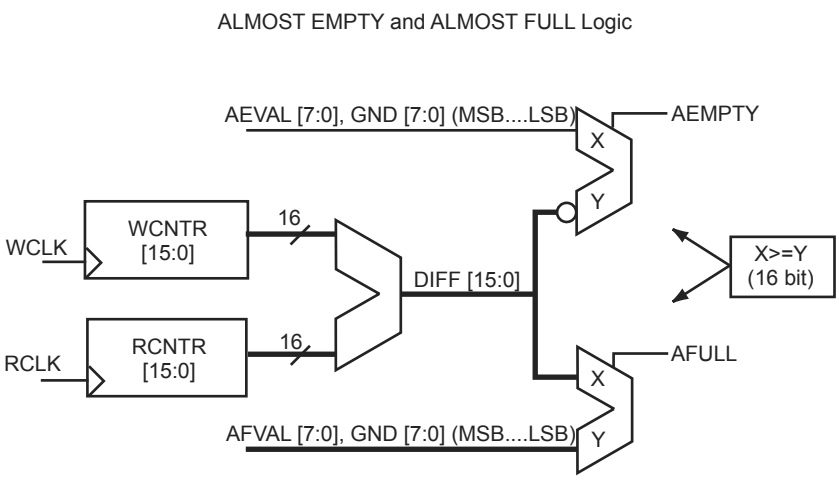


Figure 2-63 • **ALMOST-EMPTY and ALMOST-FULL Logic**

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-95).

Table 2-95 • **Number of Available Configuration Bits**

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

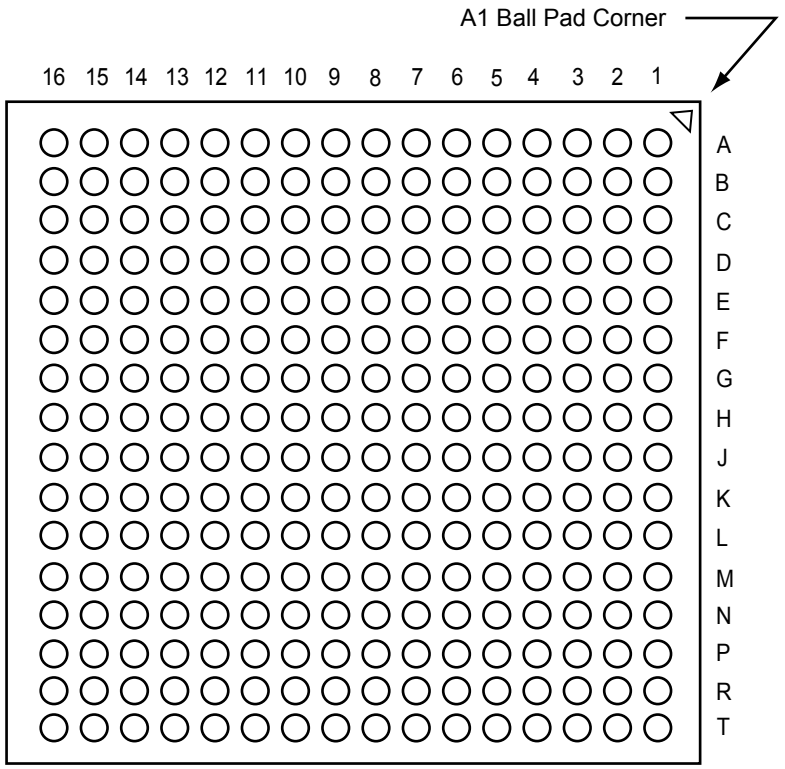
Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-100.

BG729	
AX1000 Function	Pin Number
IO109NB3F10	V24
IO109PB3F10	V25
IO110NB3F10	T20
IO110PB3F10	T21
IO111NB3F10	W26
IO111PB3F10	W27
IO112NB3F10	U22
IO112PB3F10	U23
IO113NB3F10	Y26
IO113PB3F10	Y27
IO114NB3F10	U20
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	W25
IO116NB3F10	V22
IO116PB3F10	V23
IO117NB3F10	Y24
IO117PB3F10	Y25
IO118NB3F11	V20
IO118PB3F11	V21
IO119NB3F11	AA26
IO119PB3F11	AA27
IO120NB3F11	W22
IO120PB3F11	W23
IO121NB3F11	AA24
IO121PB3F11	AA25
IO122NB3F11	W20
IO122PB3F11	W21
IO123NB3F11	AB26
IO123PB3F11	AB27
IO124NB3F11	Y22
IO124PB3F11	Y23
IO125NB3F11	AB24
IO125PB3F11	AB25
IO126NB3F11	AA22
IO126PB3F11	AA23
IO127NB3F11	AC26

BG729	
AX1000 Function	Pin Number
IO127PB3F11	AC27
IO128NB3F11	Y20
IO128PB3F11	W19
Bank 4	
IO129NB4F12	AA20
IO129PB4F12	Y21
IO130NB4F12	AB22
IO130PB4F12	AB23
IO131NB4F12	AC22
IO131PB4F12	AC23
IO132NB4F12	AD23
IO132PB4F12	AD24
IO133NB4F12	AF23
IO133PB4F12	AE23
IO134NB4F12	AC21
IO134PB4F12	AB21
IO135NB4F12	AC20
IO135PB4F12	AB20
IO136NB4F12	AD21
IO136PB4F12	AD22
IO137NB4F12	Y19
IO137PB4F12	AA19
IO138NB4F12	AE21
IO138PB4F12	AE22
IO139NB4F13	AF21
IO139PB4F13	AF22
IO140NB4F13	AG22
IO140PB4F13	AG23
IO141NB4F13	Y18
IO141PB4F13	AA18
IO142NB4F13	AE20
IO142PB4F13	AD20
IO143NB4F13	AG20
IO143PB4F13	AG21
IO144NB4F13	AC19
IO144PB4F13	AB19
IO145NB4F13	AD18

BG729	
AX1000 Function	Pin Number
IO145PB4F13	AD19
IO146NB4F13	AC18
IO146PB4F13	AB18
IO147NB4F13	Y17
IO147PB4F13	AA17
IO148NB4F13	AF19
IO148PB4F13	AF20
IO149NB4F13	AC17
IO149PB4F13	AB17
IO150NB4F13	AE18
IO150PB4F13	AE19
IO151NB4F13	AA16
IO151PB4F13	Y16
IO152NB4F14	AG18
IO152PB4F14	AG19
IO153NB4F14	AC16
IO153PB4F14	AB16
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AB15
IO155PB4F14	AC15
IO156NB4F14	AE16
IO156PB4F14	AE17
IO157NB4F14	Y15
IO157PB4F14	AA15
IO158NB4F14	AG16
IO158PB4F14	AG17
IO159NB4F14/CLKEN	AF15
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AD14
IO160PB4F14/CLKFP	AD15
Bank 5	
IO161NB5F15/CLKGN	AE14
IO161PB5F15/CLKGP	AE15
IO162NB5F15/CLKHN	AC13
IO162PB5F15/CLKHP	AD13
IO163NB5F15	Y14

FG256



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG484	
AX250 Function	**Pin Number**
IO52NB3F3	P18
IO52PB3F3	P19
IO53NB3F3	R20
IO53PB3F3	P20
IO54NB3F3	T21
IO54PB3F3	R21
IO55NB3F3	R17
IO55PB3F3	P17
IO56NB3F3	U20
IO56PB3F3	T20
IO57NB3F3	T18
IO57PB3F3	R18
IO58NB3F3	U19
IO58PB3F3	T19
IO59NB3F3	R16
IO59PB3F3	P16
IO60NB3F3	W20
IO60PB3F3	V20
IO61NB3F3	U18
IO61PB3F3	V19
Bank 4	
IO62NB4F4	T15
IO62PB4F4	T16
IO63NB4F4	W17
IO63PB4F4	V17
IO64NB4F4	V15
IO64PB4F4	V16
IO65NB4F4	Y19
IO65PB4F4	W18
IO66NB4F4	AB18
IO66PB4F4	AB19
IO67NB4F4	W15
IO67PB4F4	W16
IO68NB4F4	U14
IO68PB4F4	U15
IO69NB4F4	AA16

FG484	
AX250 Function	**Pin Number**
IO69PB4F4	AA17
IO70NB4F4	AB14
IO70PB4F4	AB15
IO71NB4F4	Y14
IO71PB4F4	W14
IO72NB4F4	AA14
IO72PB4F4	AA15
IO73NB4F4	AA13
IO73PB4F4	AB13
IO74NB4F4/CLKEN	V12
IO74PB4F4/CLKEP	V13
IO75NB4F4/CLKFN	W11
IO75PB4F4/CLKFP	W12
Bank 5	
IO76NB5F5/CLKGN	U10
IO76PB5F5/CLKGP	U11
IO77NB5F5/CLKHN	V9
IO77PB5F5/CLKHP	V10
IO78NB5F5	AA9
IO78PB5F5	AA10
IO79NB5F5	AB9
IO79PB5F5	AB10
IO80NB5F5	AA7
IO80PB5F5	AA8
IO81NB5F5	W8
IO81PB5F5	W9
IO82NB5F5	AB5
IO82PB5F5	AB6
IO83NB5F5	AA5
IO83PB5F5	AA6
IO84NB5F5	U8
IO84PB5F5	U9
IO85NB5F5	Y6
IO85PB5F5	Y7
IO86NB5F5	W6
IO86PB5F5	W7

FG484	
AX250 Function	**Pin Number**
IO87NB5F5	Y4
IO87PB5F5	Y5
IO88NB5F5	V6
IO88PB5F5	V7
IO89NB5F5	T7
IO89PB5F5	T8
Bank 6	
IO90NB6F6	V4
IO90PB6F6	W5
IO91NB6F6	P7
IO91PB6F6	R7
IO92NB6F6	U5
IO92PB6F6	T5
IO93NB6F6	P6
IO93PB6F6	R6
IO94NB6F6	T4
IO94PB6F6	U4
IO95NB6F6	P5
IO95PB6F6	R5
IO96NB6F6	T3
IO96PB6F6	U3
IO97NB6F6	P3
IO97PB6F6	R3
IO98NB6F6	R2
IO98PB6F6	T2
IO99NB6F6	P4
IO99PB6F6	R4
IO100NB6F6	P1
IO100PB6F6	R1
IO101NB6F6	M7
IO101PB6F6	N7
IO102NB6F6	N2
IO102PB6F6	P2
IO103NB6F6	M6
IO103PB6F6	N6
IO104NB6F6	M4

FG484	
AX1000 Function	**Pin Number**
IO246NB7F22	F3
IO246PB7F22	G3
IO250NB7F23	F4
IO250PB7F23	G4
IO253NB7F23	G5
IO253PB7F23	G6
IO254NB7F23	D1
IO254PB7F23	E1
IO257NB7F23	F5
IO257PB7F23	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19

FG484	
AX1000 Function	**Pin Number**
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18

FG484	
AX1000 Function	**Pin Number**
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17

FG896	
AX1000 Function	Pin Number
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12

FG896	
AX1000 Function	Pin Number
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8

FG896	
AX1000 Function	Pin Number
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4

FG896	
AX2000 Function	Pin Number
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
Bank 3	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26

FG896	
AX2000 Function	Pin Number
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27

FG896	
AX2000 Function	Pin Number
IO163NB3F15	AC26
IO163PB3F15	AB26
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23
IO170PB3F15	AA23
Bank 4	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23

PQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

PQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

PQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

PQ208	
AX250 Function	**Pin Number**
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90

PQ208	
AX250 Function	**Pin Number**
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189

PQ208	
AX250 Function	**Pin Number**
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX250 Function	**Pin Number**
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	**Pin Number**
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

Revision	Changes	Page
Revision 10 (continued)	The "TRST" section was updated.	2-107
	The "Global Set Fuse" section was added.	2-109
	A footnote was added to "FG896" for the AX2000 regarding pins AB1, AE2, G1, and K2.	3-52
	Pinouts for the AX250, AX500, and AX1000 were added for "CQ352".	3-98
	Pinout for the AX1000 was added for "CG624".	3-115
Revision 9 (v2.1)	Table 2-79 was updated.	2-69
	The "Low Power Mode" section was updated.	2-106
Revision 8 (v2.0)	Table 1 has been updated.	i
	The "Ordering Information" section has been updated.	ii
	The "Device Resources" section has been updated.	ii
	The "Temperature Grade Offerings" section is new.	iii
	The "Speed Grade and Temperature Grade Matrix" section has been updated.	iii
	Table 2-9 has been updated.	2-12
	Table 2-10 has been updated.	2-12
	Table 2-1 has been updated.	2-1
	Table 2-2 has been updated.	2-1
	Table 2-3 has been updated.	2-2
	Table 2-4 has been updated.	2-3
	Table 2-5 has been updated.	2-4
	The "Power Estimation Example" section has been updated.	2-5
	The "Thermal Characteristics" section has been updated.	2-6
	The "Package Thermal Characteristics" section has been updated.	2-6
	The "Timing Characteristics" section has been updated.	2-7
	The "Pin Descriptions" section has been updated.	2-9
	Timing numbers have been updated from the "3.3 V LVTTL" section to the "Timing Characteristics" section. Many AC Loads were updated as well.	2-25 to 2-59
	Timing characteristics for the "Hardwired Clocks" and "Routed Clocks" sections were updated.	2-66, 2-68
	Table 2-89 to Table 2-92 and Table 2-98 to Table 2-99 were updated.	2-90 to 2-93, 2-102 to 2-103
	The following sections were updated: "Low Power Mode", "Interface", "Data Registers (DRs)", "Security", "Silicon Explorer II Probe Interface", and "Programming"	2-106 to 2-110
	In the "PQ208" (AX500) section, pins 2, 52, and 156 changed from V_{CCDA} to V_{CCA}. For pins 170 and 171, the I/O names refer to pair 23 instead of 24.	3-84