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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	336
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-2fg676

Figure 1-2 • Axcelerator Family Interconnect Elements

Logic Modules

Microsemi's Axcelerator family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3).

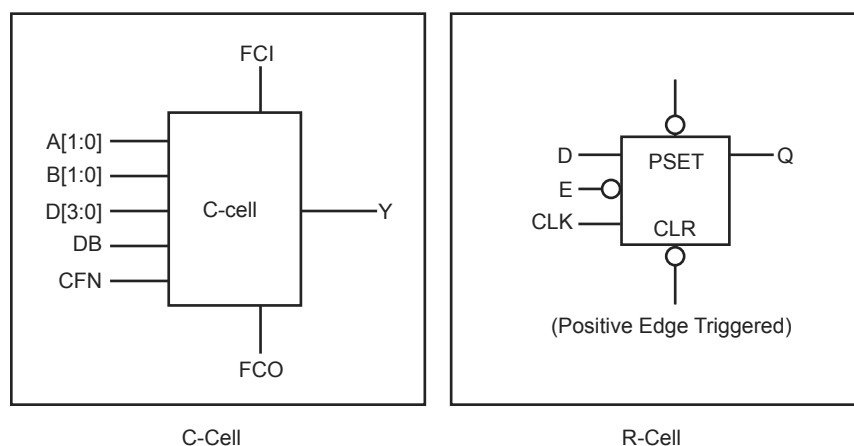


Figure 1-3 • AX C-Cell and R-Cell

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

$$P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po}$$

C_{load} = the output load (technology dependent)
 V_{CCI} = the output voltage (technology dependent)
 po = the number of outputs
 F_{po} = the average output frequency

$$P_{\text{memory}} = P_{11} * N_{\text{block}} * FR_{\text{CLK}} + P_{12} * N_{\text{block}} * FW_{\text{CLK}}$$

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
 F_{RCLK} = the read-clock frequency of the memory
 F_{WCLK} = the write-clock frequency of the memory

$$P_{\text{PLL}} = P_{13} * F_{\text{CLK}}$$

F_{RefCLK} = the clock frequency of the clock input of the PLL
 F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
 F_s = 100 MHz
 s = 1080

$$\Rightarrow P_{\text{HCLK}} = (P_1 + P_2 * s + P_3 * \text{sqrt}[s]) * F_s = 79 \text{ mW}$$

and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{R-cells}} = P_7 * ms * F_s = 173 \text{ mW}$$

mc = 1 (1 C-cell in this shift-register)
and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{C-cells}} = P_8 * mc * F_s = 0.14 \text{ mW}$$

$F_{pi} \sim 0 \text{ MHz}$

and $pi = 1$ (1 reset input => this is why $F_{pi} = 0$)

$$\Rightarrow P_{\text{inputs}} = P_9 * pi * F_{pi} = 0 \text{ mW}$$

$F_{po} = 50 \text{ MHz}$

and $po = 1$

$$\Rightarrow P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po} = 27.10 \text{ mW}$$

No RAM/FIFO in this shift-register

$$\Rightarrow P_{\text{memory}} = 0 \text{ mW}$$

No PLL in this shift-register

$$\Rightarrow P_{\text{PLL}} = 0 \text{ mW}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}} = 276 \text{ mW}$$

$$P_{\text{dc}} = 7.5\text{mA} * 1.5\text{V} = 11.25 \text{ mW}$$

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}} = 11.25 \text{ mW} + 276\text{mW} = 290.30 \text{ mW}$$

I/O Standard Electrical Specifications

Table 2-18 • Input Capacitance

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF

Table 2-19 • I/O Input Rise Time and Fall Time*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTTL	No Requirement	50 ns
LVC MOS 2.5V	No Requirement	50 ns
LVC MOS 1.8V	No Requirement	50 ns
LVC MOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

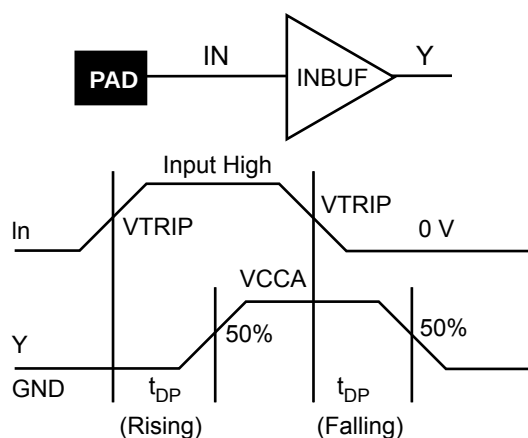


Figure 2-9 • Input Buffer Delays

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		3.30		3.76		4.42	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.74		4.26		5.00	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.06		3.49		4.10	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.29		2.30		2.31	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-25 • 2.5V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS25 I/O Module Timing								
t _{DP}	Input Buffer		1.95		2.22		2.61	ns
t _{PY}	Output Buffer		3.29		3.74		4.40	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		2.48		2.50		2.51	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		2.48		2.50		2.51	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		5.74		6.54		7.69	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.60		7.51		8.83	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111". If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:
The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microsemi identity, part number, and version number in a specific JTAG format.
2. USERCODE:
The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.
3. Boundary-Scan Register (BSR):
Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.
4. Bypass Register (BYR):
This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

Special Fuses

Security

Microsemi antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO163PB5F15	AA14	IO182NB5F17	AF7	IO200NB6F18	AA4
IO164NB5F15	AE13	IO182PB5F17	AG7	IO200PB6F18	AA5
IO164PB5F15	AF13	IO183NB5F17	AD7	IO201NB6F18	W5
IO165NB5F15	AF12	IO183PB5F17	AE7	IO201PB6F18	W6
IO165PB5F15	AG12	IO184NB5F17	AC7	IO202NB6F18	AB1
IO166NB5F15	AD12	IO184PB5F17	AC8	IO202PB6F18	AC1
IO166PB5F15	AE12	IO185NB5F17	AF6	IO203NB6F19	Y3
IO167NB5F15	Y13	IO185PB5F17	AG6	IO203PB6F19	AA3
IO167PB5F15	AA13	IO186NB5F17	AB7	IO204NB6F19	AA2
IO168NB5F15	AD11	IO186PB5F17	AB8	IO204PB6F19	AB2
IO168PB5F15	AE11	IO187NB5F17	Y9	IO205NB6F19	U8
IO169NB5F15	AG11	IO187PB5F17	AA9	IO205PB6F19	V8
IO169PB5F15	AF11	IO188NB5F17	AD6	IO206NB6F19	V5
IO170NB5F15	AB11	IO188PB5F17	AE6	IO206PB6F19	V6
IO170PB5F15	AC11	IO189NB5F17	AB6	IO207NB6F19	Y1
IO171NB5F16	AF10	IO189PB5F17	AC6	IO207PB6F19	AA1
IO171PB5F16	AG10	IO190NB5F17	AF5	IO208NB6F19	W4
IO172NB5F16	AD10	IO190PB5F17	AG5	IO208PB6F19	Y4
IO172PB5F16	AE10	IO191NB5F17	AA6	IO209NB6F19	T7
IO173NB5F16	Y12	IO191PB5F17	AA7	IO209PB6F19	U7
IO173PB5F16	AA12	IO192NB5F17	Y8	IO210NB6F19	W2
IO174NB5F16	AB10	IO192PB5F17	AA8	IO210PB6F19	Y2
IO174PB5F16	AC10	Bank 6		IO211NB6F19	U5
IO175NB5F16	AF9	IO193NB6F18	W8	IO211PB6F19	U6
IO175PB5F16	AG9	IO193PB6F18	Y7	IO212NB6F19	V3
IO176NB5F16	AD9	IO194NB6F18	AB5	IO212PB6F19	W3
IO176PB5F16	AE9	IO194PB6F18	AC5	IO213NB6F19	R9
IO177NB5F16	Y11	IO195NB6F18	AC2	IO213PB6F19	T8
IO177PB5F16	AA11	IO195PB6F18	AC3	IO214NB6F20	U4
IO178NB5F16	AF8	IO196NB6F18	AC4	IO214PB6F20	V4
IO178PB5F16	AG8	IO196PB6F18	AD4	IO215NB6F20	T5
IO179NB5F16	AD8	IO197NB6F18	Y5	IO215PB6F20	T6
IO179PB5F16	AE8	IO197PB6F18	Y6	IO216NB6F20	V1
IO180NB5F16	AB9	IO198NB6F18	AB3	IO216PB6F20	W1
IO180PB5F16	AC9	IO198PB6F18	AB4	IO217NB6F20	R7
IO181NB5F17	Y10	IO199NB6F18	V7	IO217PB6F20	R8
IO181PB5F17	AA10	IO199PB6F18	W7	IO218NB6F20	U2

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO218PB6F20	V2	IO236PB7F22	L1	IO255NB7F23	F5
IO219NB6F20	T1	IO237NB7F22	L4	IO255PB7F23	G5
IO219PB6F20	U1	IO237PB7F22	L3	IO256NB7F23	F3
IO220NB6F20	R5	IO238NB7F22	L6	IO256PB7F23	F4
IO220PB6F20	R6	IO238PB7F22	M6	IO257NB7F23	H7
IO221NB6F20	T3	IO239NB7F22	M8	IO257PB7F23	J7
IO221PB6F20	T4	IO239PB7F22	M7	Dedicated I/O	
IO222NB6F20	R2	IO240NB7F22	K2	GND	A1
IO222PB6F20	T2	IO240PB7F22	K1	GND	A2
IO223NB6F20	P8	IO241NB7F22	K4	GND	A25
IO223PB6F20	P9	IO241PB7F22	K3	GND	A26
IO224NB6F20	R3	IO242NB7F22	K5	GND	A27
IO224PB6F20	R4	IO242PB7F22	L5	GND	A3
Bank 7		IO243NB7F22	J2	GND	AC24
IO225NB7F21	P1	IO243PB7F22	J1	GND	AE1
IO225PB7F21	R1	IO244NB7F22	J4	GND	AE2
IO226NB7F21	P3	IO244PB7F22	J3	GND	AE25
IO226PB7F21	P2	IO245NB7F22	H2	GND	AE26
IO227NB7F21	N7	IO245PB7F22	H1	GND	AE27
IO227PB7F21	P7	IO246NB7F22	H4	GND	AE3
IO228NB7F21	P5	IO246PB7F22	H3	GND	AE5
IO228PB7F21	P4	IO247NB7F23	L8	GND	AF1
IO229NB7F21	N2	IO247PB7F23	L7	GND	AF2
IO229PB7F21	N1	IO248NB7F23	J6	GND	AF25
IO230NB7F21	N6	IO248PB7F23	K6	GND	AF26
IO230PB7F21	P6	IO249NB7F23	H5	GND	AF27
IO231NB7F21	N9	IO249PB7F23	J5	GND	AF3
IO231PB7F21	N8	IO250NB7F23	G2	GND	AG1
IO232NB7F21	N4	IO250PB7F23	G1	GND	AG2
IO232PB7F21	N3	IO251NB7F23	K8	GND	AG25
IO233NB7F21	M2	IO251PB7F23	K7	GND	AG26
IO233PB7F21	M1	IO252NB7F23	G4	GND	AG27
IO234NB7F21	M4	IO252PB7F23	G3	GND	AG3
IO234PB7F21	M3	IO253NB7F23	F2	GND	B1
IO235NB7F21	M5	IO253PB7F23	F1	GND	B2
IO235PB7F21	N5	IO254NB7F23	G6	GND	B25
IO236NB7F22	L2	IO254PB7F23	H6	GND	B26

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	B27	GND	R11	VCCA	K11
GND	B3	GND	R12	VCCA	K17
GND	C1	GND	R13	VCCA	K18
GND	C2	GND	R14	VCCA	L10
GND	C25	GND	R15	VCCA	L18
GND	C26	GND	R16	VCCA	U10
GND	C27	GND	R17	VCCA	U18
GND	C3	GND	T11	VCCA	V10
GND	E27	GND	T12	VCCA	V11
GND	L11	GND	T13	VCCA	V17
GND	L12	GND	T14	VCCA	V18
GND	L13	GND	T15	VCCPLA	A13
GND	L14	GND	T16	VCCPLB	J13
GND	L15	GND	T17	VCCPLC	B15
GND	L16	GND	U11	VCCPLD	C15
GND	L17	GND	U12	VCCPLE	AG14
GND	M11	GND	U13	VCCPLF	AF14
GND	M12	GND	U14	VCCPLG	AB13
GND	M13	GND	U15	VCCPLH	AG13
GND	M14	GND	U16	VCCDA	A11
GND	M15	GND	U17	VCCDA	AB12
GND	M16	GND/LP	J8	VCCDA	AC12
GND	M17	NC	U3	VCCDA	AC25
GND	N11	PRA	J14	VCCDA	AD16
GND	N12	PRB	D14	VCCDA	AD17
GND	N13	PRC	V14	VCCDA	E16
GND	N14	PRD	AB14	VCCDA	E2
GND	N15	TCK	E4	VCCDA	E24
GND	N16	TDI	D4	VCCDA	F12
GND	N17	TDO	J9	VCCDA	F16
GND	P11	TMS	H8	VCCDA	F7
GND	P12	TRST	E3	VCCDA	K14
GND	P13	VCCA	AA21	VCCDA	P10
GND	P14	VCCA	AD5	VCCDA	P18
GND	P15	VCCA	E1	VCCDA	W14
GND	P16	VCCA	G22	VCCDA	W9
GND	P17	VCCA	K10	VCCIB0	A4

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 6		IO81NB7F7	C2	GND	M12
IO60NB6F6	L4	IO81PB7F7	B1	GND	M5
IO60PB6F6	M4	IO82NB7F7	D2	GND	P13
IO61NB6F6	L3	IO82PB7F7	D3	GND	P3
IO61PB6F6	M3	IO83NB7F7	E3	GND	R15
IO63NB6F6	P2	IO83PB7F7	F3	GND	R2
IO63PB6F6	N2	Dedicated I/O		GND	T1
IO64NB6F6	J4	VCCDA	E4	GND	T16
IO64PB6F6	K4	GND	A1	GND/LP	D4
IO65NB6F6	N1	GND	A16	NC	A11
IO65PB6F6	P1	GND	B15	NC	R11
IO67NB6F6	L2	GND	B2	NC	R5
IO67PB6F6	M2	GND	D15	PRA	D8
IO69NB6F6	L1	GND	E12	PRB	C8
IO69PB6F6	M1	GND	E5	PRC	N9
IO70NB6F6	J3	GND	F11	PRD	P9
IO70PB6F6	K3	GND	F6	TCK	D5
IO71NB6F6	J2	GND	G10	TDI	C6
IO71PB6F6	K2	GND	G7	TDO	C4
Bank 7		GND	G8	TMS	C3
IO72NB7F7	J1	GND	G9	TRST	C5
IO72PB7F7	K1	GND	H10	VCCA	D14
IO73NB7F7	G2	GND	H7	VCCA	F10
IO73PB7F7	H2	GND	H8	VCCA	F4
IO74NB7F7	G3	GND	H9	VCCA	F7
IO74PB7F7	H3	GND	J10	VCCA	F8
IO75NB7F7	E1	GND	J7	VCCA	F9
IO75PB7F7	F1	GND	J8	VCCA	G11
IO76NB7F7	G1	GND	J9	VCCA	G6
IO77NB7F7	E2	GND	K10	VCCA	H11
IO77PB7F7	F2	GND	K7	VCCA	H6
IO78NB7F7	G4	GND	K8	VCCA	J11
IO78PB7F7	H4	GND	K9	VCCA	J6
IO79NB7F7	C1	GND	L11	VCCA	K11
IO79PB7F7	D1	GND	L6	VCCA	K6

FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9

FG676	
AX500 Function	Pin Number
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21

FG676	
AX500 Function	Pin Number
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

FG896	
AX2000 Function	Pin Number
IO65PB1F6	H20
IO66NB1F6	B23
IO66PB1F6	B21
IO67NB1F6	H21
IO67PB1F6	G21
IO68NB1F6	D22
IO68PB1F6	C22
IO69NB1F6	A25
IO69PB1F6	A24
IO70NB1F6	F22
IO70PB1F6	E22
IO71NB1F6	F21
IO71PB1F6	E21
IO73NB1F6	C24
IO73PB1F6	C23
IO74NB1F6	D24
IO74PB1F6	D23
IO75NB1F6	H23
IO75PB1F6	H22
IO76NB1F7	B25
IO76PB1F7	B24
IO78NB1F7	B26
IO78PB1F7	A26
IO79NB1F7	F23
IO79PB1F7	E23
IO80NB1F7	D25
IO80PB1F7	C25
IO81NB1F7	G23
IO81PB1F7	G22
IO82NB1F7	B27
IO82PB1F7	A27
IO83NB1F7	F24
IO83PB1F7	E24
IO84NB1F7	D26
IO84PB1F7	C26

FG896	
AX2000 Function	Pin Number
IO85NB1F7	F25
IO85PB1F7	E25
Bank 2	
IO86NB2F8	G26
IO86PB2F8	G25
IO87NB2F8	K23
IO87PB2F8	J23
IO88NB2F8	J24
IO88PB2F8	H24
IO89NB2F8	E29
IO89PB2F8	D29
IO90NB2F8	F27
IO90PB2F8	E27
IO91NB2F8	H26
IO91PB2F8	H25
IO92NB2F8	G28
IO92PB2F8	F28
IO93NB2F8	J26
IO93PB2F8	J25
IO94NB2F8	H27
IO94PB2F8	G27
IO95NB2F8	H29
IO95PB2F8	G29
IO96NB2F9	G30
IO96PB2F9	F30
IO97NB2F9	K25
IO97PB2F9	K24
IO98NB2F9	J28
IO98PB2F9	H28
IO99NB2F9	L23
IO99PB2F9	L24
IO100NB2F9	K27
IO100PB2F9	J27
IO101PB2F9	J30
IO102NB2F9	E30

FG896	
AX2000 Function	Pin Number
IO102PB2F9	D30
IO103NB2F9	L26
IO103PB2F9	K26
IO104NB2F9	F29
IO105NB2F9	M25
IO105PB2F9	L25
IO106NB2F9	K30
IO106PB2F9	K29
IO107NB2F10	M23
IO107PB2F10	M24
IO109NB2F10	M27
IO109PB2F10	L27
IO110NB2F10	M28
IO110PB2F10	L28
IO111NB2F10	N22
IO111PB2F10	N23
IO112NB2F10	M29
IO112PB2F10	L29
IO113NB2F10	N26
IO113PB2F10	M26
IO114NB2F10	M30
IO114PB2F10	L30
IO115NB2F10	N28
IO115PB2F10	N27
IO117NB2F10	N25
IO117PB2F10	N24
IO118NB2F11	N29
IO119NB2F11	P22
IO119PB2F11	P23
IO121NB2F11	P25
IO121PB2F11	P24
IO122NB2F11	P28
IO122PB2F11	P27
IO123NB2F11	R26
IO123PB2F11	P26

FG896	
AX2000 Function	Pin Number
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
Bank 3	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26

FG896	
AX2000 Function	Pin Number
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27

FG896	
AX2000 Function	Pin Number
IO163NB3F15	AC26
IO163PB3F15	AB26
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23
IO170PB3F15	AA23
Bank 4	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	N1	GND	U19	NC	A26
GND	N13	GND	U20	NC	AB2
GND	N22	GND	U21	NC	AB33
GND	N34	GND	U30	NC	AC34
GND	P14	GND	U5	NC	AD3
GND	P15	GND	V14	NC	AD34
GND	P16	GND	V15	NC	AE31
GND	P17	GND	V16	NC	AE33
GND	P18	GND	V17	NC	AE34
GND	P19	GND	V18	NC	AF1
GND	P20	GND	V19	NC	AF34
GND	P21	GND	V20	NC	AG2
GND	R14	GND	V21	NC	AG4
GND	R15	GND	V30	NC	AH1
GND	R16	GND	V5	NC	AH2
GND	R17	GND	W14	NC	AH31
GND	R18	GND	W15	NC	AH32
GND	R19	GND	W16	NC	AH34
GND	R20	GND	W17	NC	AJ1
GND	R21	GND	W18	NC	AJ2
GND	R3	GND	W19	NC	AJ3
GND	R32	GND	W20	NC	AJ31
GND	T14	GND	W21	NC	AJ32
GND	T15	GND	Y14	NC	AJ33
GND	T16	GND	Y15	NC	AJ34
GND	T17	GND	Y16	NC	AJ4
GND	T18	GND	Y17	NC	AL29
GND	T19	GND	Y18	NC	AM19
GND	T20	GND	Y19	NC	AM7
GND	T21	GND	Y20	NC	AN13
GND	U14	GND	Y21	NC	AN17
GND	U15	GND	Y3	NC	AN25
GND	U16	GND	Y32	NC	AN27
GND	U17	GND/LP	G6	NC	AN8
GND	U18	NC	A17	NC	AP17

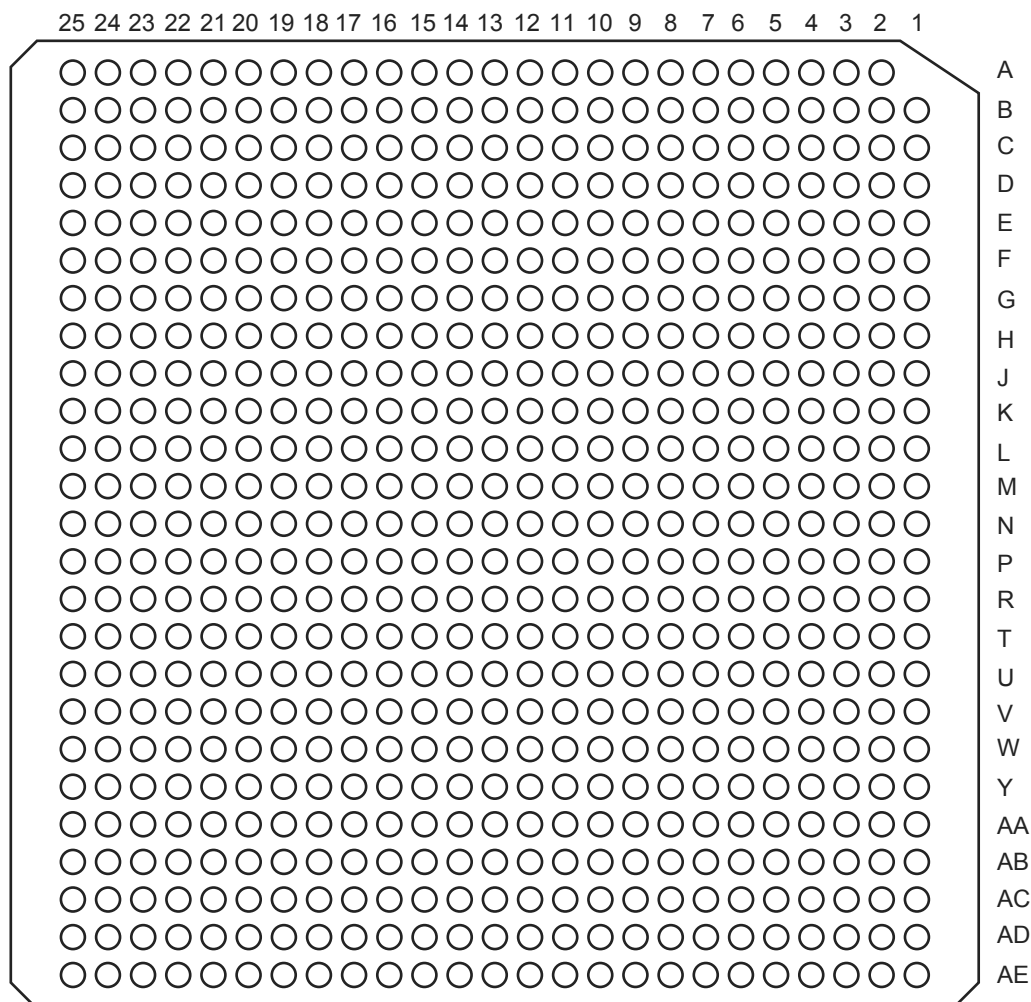
CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	21	GND	240	VCCA	14
GND	27	GND	246	VCCA	32
GND	33	GND	252	VCCA	56
GND	39	GND	258	VCCA	74
GND	45	GND	264	VCCA	87
GND	51	GND	265	VCCA	102
GND	57	GND	274	VCCA	114
GND	63	GND	280	VCCA	150
GND	69	GND	286	VCCA	162
GND	75	GND	292	VCCA	175
GND	81	GND	298	VCCA	191
GND	88	GND	310	VCCA	209
GND	89	GND	322	VCCA	233
GND	97	GND	330	VCCA	251
GND	103	GND	334	VCCA	263
GND	109	GND	340	VCCA	279
GND	115	GND	345	VCCA	291
GND	121	GND	352	VCCA	329
GND	133	NC	91	VCCA	339
GND	145	NC	130	VCCDA	2
GND	151	NC	131	VCCDA	44
GND	157	NC	174	VCCDA	90
GND	163	NC	268	VCCDA	116
GND	169	NC	307	VCCDA	117
GND	176	NC	308	VCCDA	132
GND	177	PRA	312	VCCDA	148
GND	186	PRB	311	VCCDA	149
GND	192	PRC	135	VCCDA	178
GND	198	PRD	134	VCCDA	221
GND	204	TCK	349	VCCDA	266
GND	210	TDI	348	VCCDA	293
GND	216	TDO	347	VCCDA	294
GND	222	TMS	350	VCCDA	309
GND	228	TRST	351	VCCDA	327
GND	234	VCCA	3	VCCDA	328

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15

CG624



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

CG624	
AX2000 Function	Pin Number
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22*
IO169PB3F15	W23*
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20*
IO171PB4F16	AC21*
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5
GND	V1
GND	V25
GND	V5
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
TDI	C5
TDO	F6
TMS	D6
TRST	E6
VCCA	AB20
VCCA	F22
VCCA	F4
VCCA	J17
VCCA	J9
VCCA	K10
VCCA	K11
VCCA	K15
VCCA	K16
VCCA	L10
VCCA	L16
VCCA	R10
VCCA	R16
VCCA	T10
VCCA	T11
VCCA	T15
VCCA	T16
VCCA	U17
VCCA	U9
VCCA	Y4
VCCDA	A12
VCCDA	A14
VCCDA	AA13
VCCDA	AA15
VCCDA	AA20
VCCDA	AA7
VCCDA	AB13
VCCDA	AC11

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
VCCDA	AD11
VCCDA	AD4
VCCDA	AE12
VCCDA	AE17
VCCDA	B15
VCCDA	C15
VCCDA	C6
VCCDA	D13
VCCDA	E13
VCCDA	E19
VCCDA	F21
VCCDA	G10
VCCDA	G5
VCCDA	N21
VCCDA	N5
VCCDA	W21
VCCIB0	A3
VCCIB0	B3
VCCIB0	C4
VCCIB0	D5
VCCIB0	J10
VCCIB0	J11
VCCIB0	K12
VCCIB1	A23
VCCIB1	B23
VCCIB1	C22
VCCIB1	D21
VCCIB1	J15
VCCIB1	J16
VCCIB1	K14
VCCIB2	C24
VCCIB2	C25

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.