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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

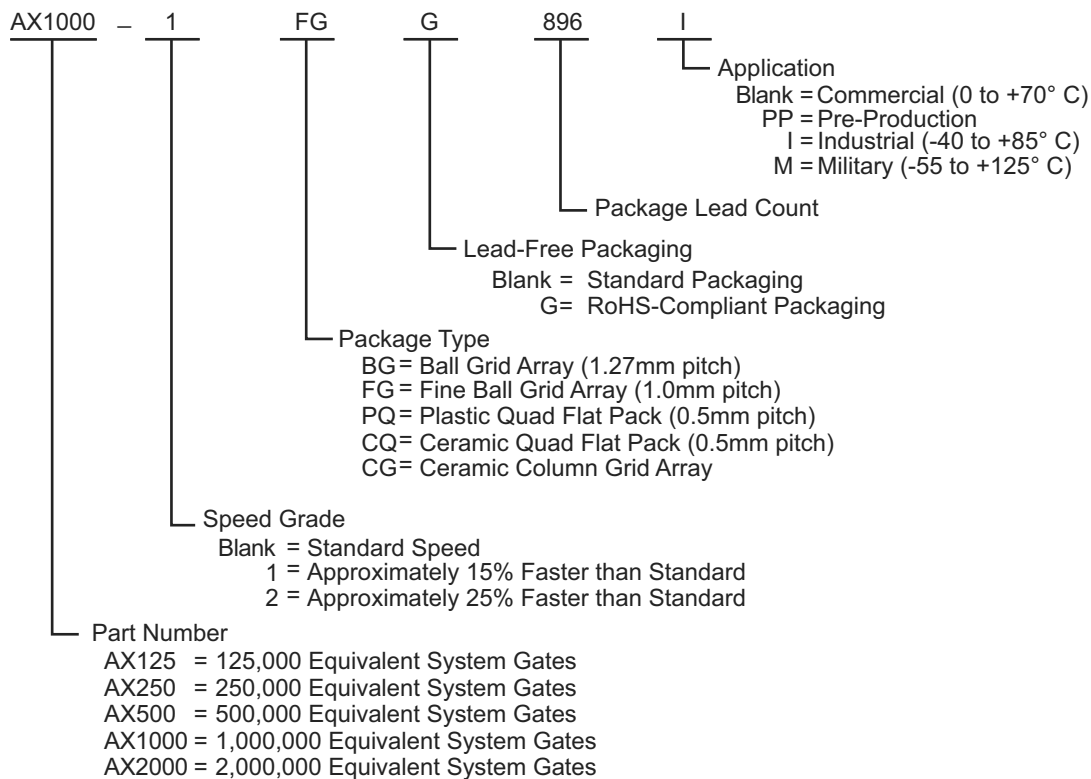
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	317
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-2fgg484

Ordering Information



Device Resources

User I/Os (Including Clock Buffers)					
Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	115	115	–	–
CQ208	–	115	115	–	–
CQ256	–	–	–	–	136
FG256	138	138	–	–	–
FG324	168	–	–	–	–
CQ352	–	198	198	198	198
FG484	–	248	317	317	–
CG624	–	–	–	418	418
FG676	–	–	336	418	–
BG729	–	–	–	516	–
FG896	–	–	–	516	586
FG1152	–	–	–	–	684

Note: The FG256, FG324, and FG484 are footprint compatible with one another. The FG676, FG896, and FG1152 are also footprint compatible with one another.

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 1 (8 mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		4.23		4.81		5.66	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		4.64		5.28		6.21	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.23		4.81		5.66	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.01		2.02		2.03	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-35 • 3.3 V PCI I/O Module

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3 V PCI Output Module Timing								
t _{DP}	Input Buffer		1.57		1.79		2.10	ns
t _{PY}	Output Buffer		1.91		2.18		2.56	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		1.61		1.62		1.63	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		1.45		1.47		1.47	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		2.55		2.90		3.41	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		3.52		4.01		4.72	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-40 • 3.3 V GTL+ I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V GTL+I/O Module Timing								
t _{DP}	Input Buffer		1.71		1.95		2.29	ns
t _{PY}	Output Buffer		1.13		1.29		1.52	ns
t _{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Class II

Table 2-47 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	15.2	-15.2

AC Loadings

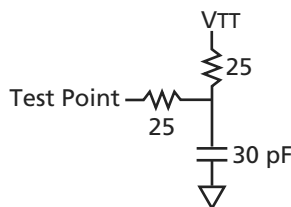


Figure 2-22 • AC Test Loads

Table 2-48 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 0.75	VREF + 0.75	VREF	1.25	30

Note: * Measuring Point = V_{trip}

Timing Characteristics

Table 2-49 • 2.5 V SSTL2 Class II I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
2.5 V SSTL2 Class II I/O Module Timing								
t _{DP}	Input Buffer		1.89		2.16		2.53	ns
t _{PY}	Output Buffer		2.39		2.72		3.20	ns
t _{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-70 • AX125 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-71 • AX250 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t _{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-72 • AX500 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		2.35		2.68		3.15	ns
t _{HCKH}	Input High to Low		2.44		2.79		3.27	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-73 • AX1000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-74 • AX2000 Dedicated (Hardwired) Array Clock Networks
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks								
t _{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t _{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t _{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t _{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t _{HP}	Minimum Period	1.15		1.31		1.54		ns
t _{HMAX}	Maximum Frequency		870		763		649	MHz

FG484		FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number	AX250 Function	Pin Number
NC	A19	NC	G22	PRA	G11
NC	A4	NC	G3	PRB	F11
NC	A5	NC	H3	PRC	T12
NC	AA11	NC	J3	PRD	U12
NC	AA12	NC	K21	TCK	G8
NC	AA18	NC	K22	TDI	F9
NC	AA19	NC	N22	TDO	F7
NC	AA4	NC	P22	TMS	F6
NC	AB16	NC	R19	TRST	F8
NC	AB17	NC	R22	VCCA	G17
NC	AB4	NC	T1	VCCA	J10
NC	AB7	NC	T22	VCCA	J11
NC	AB8	NC	U1	VCCA	J12
NC	B11	NC	U2	VCCA	J13
NC	B12	NC	U21	VCCA	J7
NC	B17	NC	U22	VCCA	K14
NC	B18	NC	V1	VCCA	K9
NC	B19	NC	V2	VCCA	L14
NC	B4	NC	V21	VCCA	L9
NC	B5	NC	V22	VCCA	M14
NC	C10	NC	V3	VCCA	M9
NC	C11	NC	W1	VCCA	N14
NC	C14	NC	W2	VCCA	N9
NC	C15	NC	W21	VCCA	P10
NC	C18	NC	W22	VCCA	P11
NC	C19	NC	W3	VCCA	P12
NC	D1	NC	Y10	VCCA	P13
NC	D2	NC	Y11	VCCA	T6
NC	D21	NC	Y12	VCCA	U17
NC	D3	NC	Y13	VCCPLA	F10
NC	E1	NC	Y15	VCCPLB	G9
NC	E2	NC	Y16	VCCPLC	D13
NC	E21	NC	Y17	VCCPLD	G13
NC	E3	NC	Y18	VCCPLE	U13
NC	F22	NC	Y8	VCCPLF	T14
NC	F3	NC	Y9	VCCPLG	W10

FG484	
AX1000 Function	Pin Number
Bank 0	
IO01NB0F0	E3
IO01PB0F0	D3
IO02NB0F0	E7
IO02PB0F0	E6
IO05NB0F0	D2
IO05PB0F0	E2
IO06NB0F0	C5
IO06PB0F0	C4
IO12NB0F1	D7
IO12PB0F1	D6
IO13NB0F1	B5
IO13PB0F1	B4
IO14NB0F1	E9
IO14PB0F1	E8
IO15NB0F1	C7
IO15PB0F1	C6
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	B7
IO17PB0F1	B6
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	C9
IO19PB0F1	C8
IO20NB0F1	D9
IO20PB0F1	D8
IO21NB0F1	B9
IO21PB0F1	B8
IO22NB0F2	A9
IO22PB0F2	A8
IO23NB0F2	B10
IO23PB0F2	A10
IO26NB0F2	A14
IO26PB0F2	A13

FG484	
AX1000 Function	Pin Number
IO29NB0F2	B12
IO29PB0F2	B11
IO30NB0F2/HCLKAN	E11
IO30PB0F2/HCLKAP	E10
IO31NB0F2/HCLKBN	D12
IO31PB0F2/HCLKBP	D11
Bank 1	
IO32NB1F3/HCLKCN	F13
IO32PB1F3/HCLKCP	F12
IO33NB1F3/HCLKDN	E14
IO33PB1F3/HCLKDP	E13
IO34NB1F3	C13
IO34PB1F3	C12
IO37NB1F3	B14
IO37PB1F3	B13
IO38NB1F3	A16
IO38PB1F3	A15
IO40NB1F3	C15
IO42NB1F4	A18
IO42PB1F4	A17
IO43NB1F4	B16
IO43PB1F4	B15
IO44NB1F4	B18
IO44PB1F4	B17
IO45NB1F4	B19
IO45PB1F4	A19
IO46NB1F4	C19
IO46PB1F4	C18
IO48NB1F4	F15
IO48PB1F4	F14
IO49NB1F4	D16
IO49PB1F4	D15
IO50NB1F4	C17
IO50PB1F4	C16
IO51NB1F4	E22

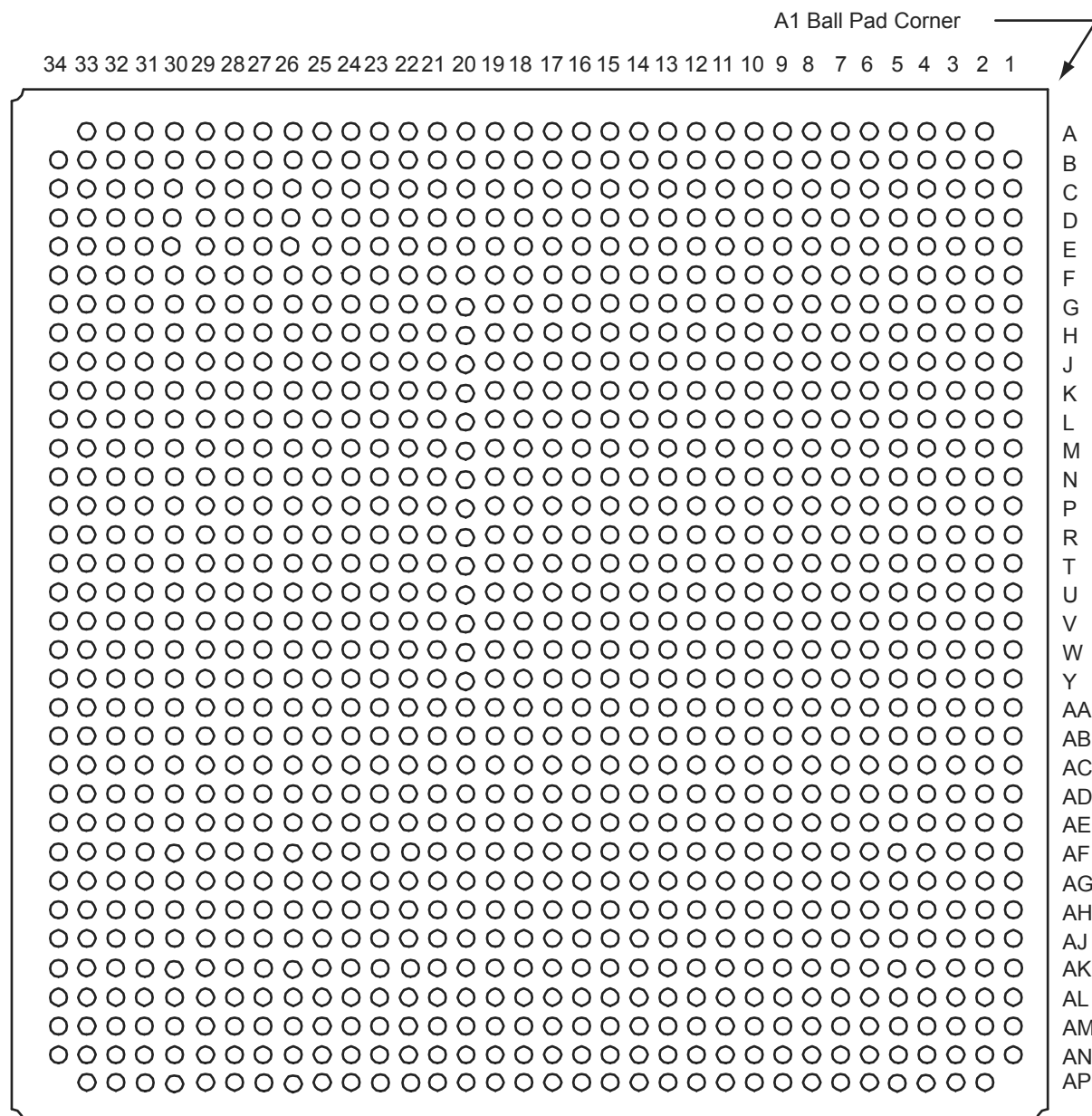
FG484	
AX1000 Function	Pin Number
IO51PB1F4	D22
IO52NB1F4	E16
IO52PB1F4	E15
IO57NB1F5	E21
IO57PB1F5	D21
IO60NB1F5	G16
IO60PB1F5	G15
IO61NB1F5	D18
IO61PB1F5	E17
IO63NB1F5	E20
IO63PB1F5	D20
Bank 2	
IO64NB2F6	F18
IO64PB2F6	F17
IO67NB2F6	F19
IO67PB2F6	E19
IO68NB2F6	J16
IO68PB2F6	H16
IO70NB2F6	J17
IO70PB2F6	H17
IO74NB2F7	J18
IO74PB2F7	H18
IO75NB2F7	G20
IO75PB2F7	F20
IO79NB2F7	H19
IO79PB2F7	G19
IO80NB2F7	L16
IO80PB2F7	K16
IO84NB2F7	L17
IO84PB2F7	K17
IO85NB2F8	G21
IO85PB2F8	F21
IO86NB2F8	G22
IO86PB2F8	F22
IO87NB2F8	J20

FG896	
AX2000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX2000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	Pin Number
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

FG1152



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO51PB1F4	J20	IO69NB1F6	C27	IO86NB2F8	J28
IO52NB1F4	B20	IO69PB1F6	C26	IO86PB2F8	J27
IO52PB1F4	A20	IO70NB1F6	H24	IO87NB2F8	M25
IO53NB1F4	F20	IO70PB1F6	G24	IO87PB2F8	L25
IO53PB1F4	E20	IO71NB1F6	H23	IO88NB2F8	L26
IO54NB1F5	B21	IO71PB1F6	G23	IO88PB2F8	K26
IO54PB1F5	A21	IO72NB1F6	B28	IO89NB2F8	G31
IO55NB1F5	K21	IO72PB1F6	A28	IO89PB2F8	F31
IO55PB1F5	J21	IO73NB1F6	E26	IO90NB2F8	H29
IO56NB1F5	D21	IO73PB1F6	E25	IO90PB2F8	G29
IO56PB1F5	C21	IO74NB1F6	F26	IO91NB2F8	K28
IO57NB1F5	G22	IO74PB1F6	F25	IO91PB2F8	K27
IO57PB1F5	G21	IO75NB1F6	K25	IO92NB2F8	J30
IO58NB1F5	E22	IO75PB1F6	K24	IO92PB2F8	H30
IO58PB1F5	E21	IO76NB1F7	D27	IO93NB2F8	L28
IO59NB1F5	D22	IO76PB1F7	D26	IO93PB2F8	L27
IO59PB1F5	C22	IO77NB1F7	B29	IO94NB2F8	K29
IO60NB1F5	B23	IO77PB1F7	A29	IO94PB2F8	J29
IO60PB1F5	A23	IO78NB1F7	D28	IO95NB2F8	K31
IO61NB1F5	H22	IO78PB1F7	C28	IO95PB2F8	J31
IO61PB1F5	H21	IO79NB1F7	H25	IO96NB2F9	J32
IO62NB1F5	C24	IO79PB1F7	G25	IO96PB2F9	H32
IO62PB1F5	C23	IO80NB1F7	F27	IO97NB2F9	M27
IO63NB1F5	F23	IO80PB1F7	E27	IO97PB2F9	M26
IO63PB1F5	F22	IO81NB1F7	J25	IO98NB2F9	L30
IO64NB1F6	B24	IO81PB1F7	J24	IO98PB2F9	K30
IO64PB1F6	A24	IO82NB1F7	D29	IO99NB2F9	N25
IO65NB1F6	J22	IO82PB1F7	C29	IO99PB2F9	N26
IO65PB1F6	K22	IO83NB1F7	H26	IO100NB2F9	M29
IO66NB1F6	B25	IO83PB1F7	G26	IO100PB2F9	L29
IO66PB1F6	A25	IO84NB1F7	F28	IO101NB2F9	L33
IO67NB1F6	K23	IO84PB1F7	E28	IO101PB2F9	L32
IO67PB1F6	J23	IO85NB1F7	H27	IO102NB2F9	K34
IO68NB1F6	F24	IO85PB1F7	G27	IO102PB2F9	K33
IO68PB1F6	E24	Bank 2		IO103NB2F9	N28

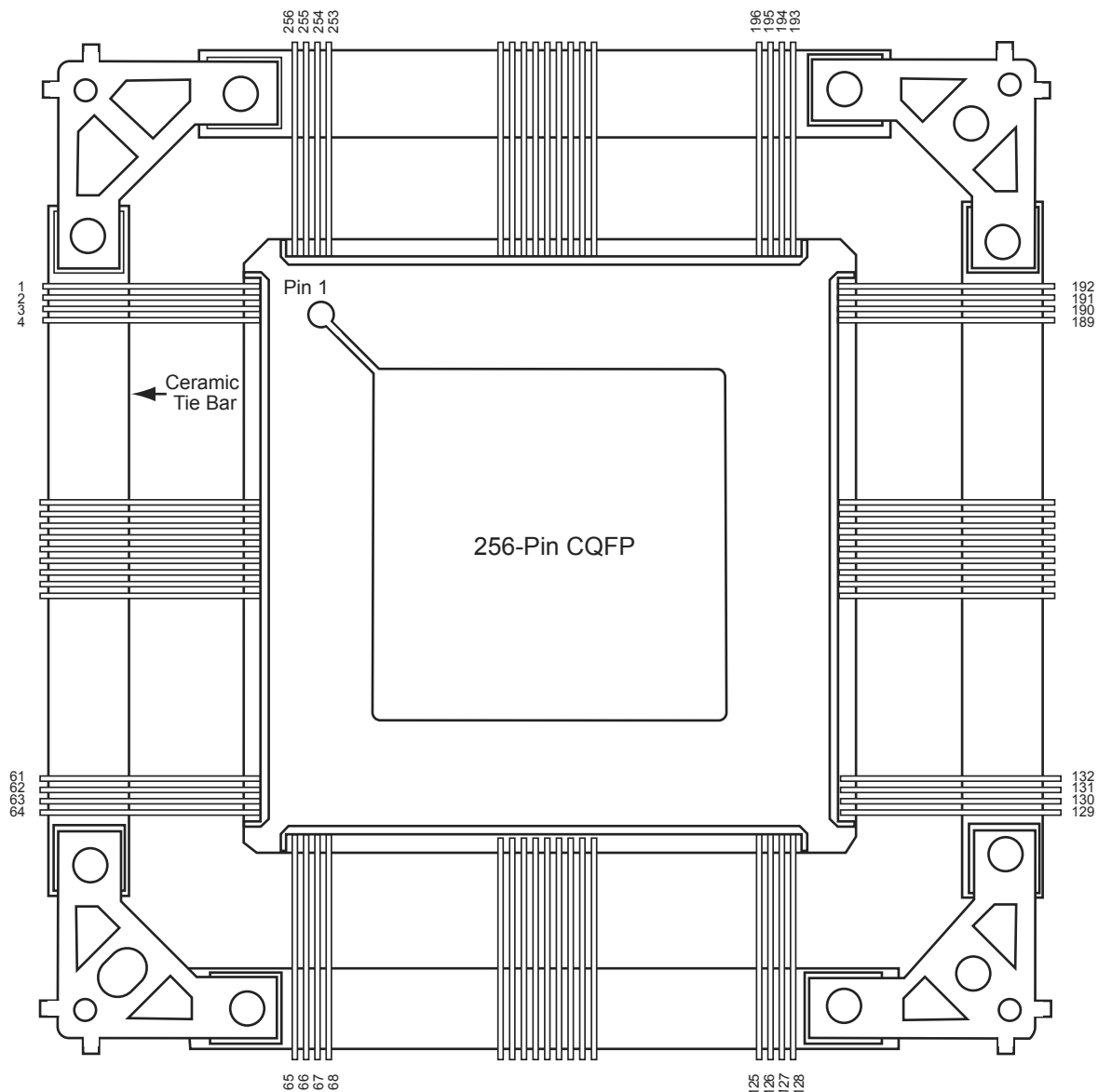
FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
GND	N1	GND	U19	NC	A26
GND	N13	GND	U20	NC	AB2
GND	N22	GND	U21	NC	AB33
GND	N34	GND	U30	NC	AC34
GND	P14	GND	U5	NC	AD3
GND	P15	GND	V14	NC	AD34
GND	P16	GND	V15	NC	AE31
GND	P17	GND	V16	NC	AE33
GND	P18	GND	V17	NC	AE34
GND	P19	GND	V18	NC	AF1
GND	P20	GND	V19	NC	AF34
GND	P21	GND	V20	NC	AG2
GND	R14	GND	V21	NC	AG4
GND	R15	GND	V30	NC	AH1
GND	R16	GND	V5	NC	AH2
GND	R17	GND	W14	NC	AH31
GND	R18	GND	W15	NC	AH32
GND	R19	GND	W16	NC	AH34
GND	R20	GND	W17	NC	AJ1
GND	R21	GND	W18	NC	AJ2
GND	R3	GND	W19	NC	AJ3
GND	R32	GND	W20	NC	AJ31
GND	T14	GND	W21	NC	AJ32
GND	T15	GND	Y14	NC	AJ33
GND	T16	GND	Y15	NC	AJ34
GND	T17	GND	Y16	NC	AJ4
GND	T18	GND	Y17	NC	AL29
GND	T19	GND	Y18	NC	AM19
GND	T20	GND	Y19	NC	AM7
GND	T21	GND	Y20	NC	AN13
GND	U14	GND	Y21	NC	AN17
GND	U15	GND	Y3	NC	AN25
GND	U16	GND	Y32	NC	AN27
GND	U17	GND/LP	G6	NC	AN8
GND	U18	NC	A17	NC	AP17

PQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132

PQ208	
AX500 Function	Pin Number
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
Bank 4	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76

PQ208	
AX500 Function	Pin Number
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18

CQ256



Note

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CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO87PB4F8	171	IO119PB5F11	101	IO146NB6F13	46
IO89NB4F8	166	IO121NB5F11	98	IO146PB6F13	47
IO89PB4F8	167	IO121PB5F11	99	Bank 7	
IO94NB4F9	164	IO123NB5F11	94	IO147NB7F14	40
IO94PB4F9	165	IO123PB5F11	95	IO147PB7F14	41
IO95NB4F9	160	IO125NB5F11	92	IO148NB7F14	42
IO95PB4F9	161	IO125PB5F11	93	IO148PB7F14	43
IO97NB4F9	158	Bank 6		IO149NB7F14	36
IO97PB4F9	159	IO126PB6F12	86	IO149PB7F14	37
IO99NB4F9	154	IO127NB6F12	84	IO151NB7F14	30
IO99PB4F9	155	IO127PB6F12	85	IO151PB7F14	31
IO100NB4F9	146	IO129NB6F12	82	IO152NB7F14	34
IO100PB4F9	147	IO129PB6F12	83	IO152PB7F14	35
IO101NB4F9	152	IO131NB6F12	78	IO153NB7F14	28
IO101PB4F9	153	IO131PB6F12	79	IO153PB7F14	29
IO103NB4F9/CLKEN	142	IO133NB6F12	76	IO155NB7F14	24
IO103PB4F9/CLKEP	143	IO133PB6F12	77	IO155PB7F14	25
IO104NB4F9/CLKFN	136	IO134NB6F12	72	IO157NB7F14	22
IO104PB4F9/CLKFP	137	IO134PB6F12	73	IO157PB7F14	23
Bank 5		IO135NB6F12	70	IO159NB7F15	16
IO105NB5F10/CLKGN	128	IO135PB6F12	71	IO159PB7F15	17
IO105PB5F10/CLKGP	129	IO137NB6F13	66	IO160NB7F15	18
IO106NB5F10/CLKHN	122	IO137PB6F13	67	IO160PB7F15	19
IO106PB5F10/CLKHP	123	IO138NB6F13	64	IO161NB7F15	12
IO107NB5F10	118	IO138PB6F13	65	IO161PB7F15	13
IO107PB5F10	119	IO139NB6F13	60	IO163NB7F15	10
IO114NB5F11	112	IO139PB6F13	61	IO163PB7F15	11
IO114PB5F11	113	IO141NB6F13	54	IO165NB7F15	6
IO115NB5F11	110	IO141PB6F13	55	IO165PB7F15	7
IO115PB5F11	111	IO142NB6F13	58	IO167NB7F15	4
IO116NB5F11	106	IO142PB6F13	59	IO167PB7F15	5
IO116PB5F11	107	IO143NB6F13	52	Dedicated I/O	
IO117NB5F11	104	IO143PB6F13	53	GND	1
IO117PB5F11	105	IO145NB6F13	48	GND	9
IO119NB5F11	100	IO145PB6F13	49	GND	15

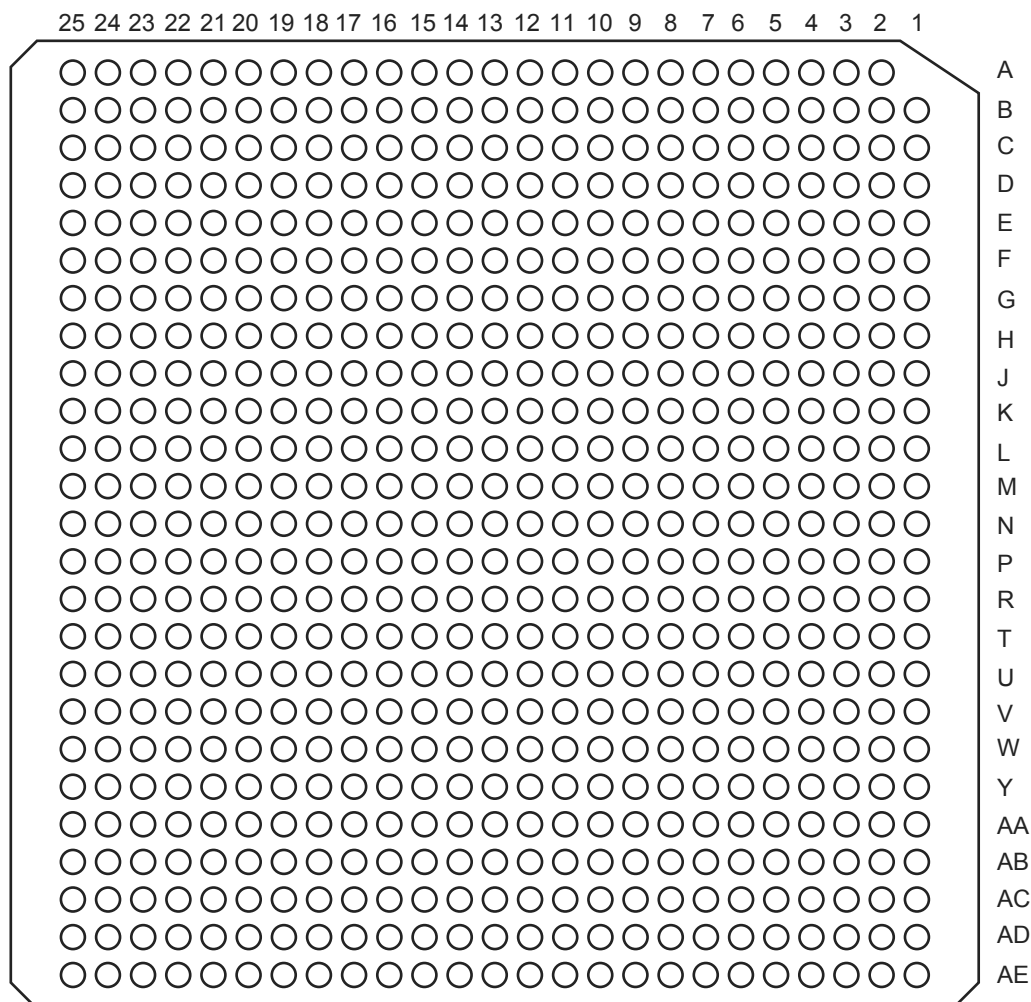
CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO131PB4F12	171	IO187PB5F17	99	IO224NB6F20	46
IO132NB4F12	166	IO188NB5F17	100	IO224PB6F20	47
IO132PB4F12	167	IO188PB5F17	101	Bank 7	
IO133NB4F12	164	IO190NB5F17	94	IO225NB7F21	40
IO133PB4F12	165	IO190PB5F17	95	IO225PB7F21	41
IO134NB4F12	160	IO192NB5F17	92	IO226NB7F21	42
IO134PB4F12	161	IO192PB5F17	93	IO226PB7F21	43
IO136NB4F12	158	Bank 6		IO237NB7F22	34
IO136PB4F12	159	IO193PB6F18	86	IO237PB7F22	35
IO137NB4F12	154	IO194NB6F18	84	IO238NB7F22	36
IO137PB4F12	155	IO194PB6F18	85	IO238PB7F22	37
IO138NB4F12	152	IO196NB6F18	78	IO240NB7F22	30
IO138PB4F12	153	IO196PB6F18	79	IO240PB7F22	31
IO153NB4F14	146	IO197NB6F18	82	IO241NB7F22	28
IO153PB4F14	147	IO197PB6F18	83	IO241PB7F22	29
IO159NB4F14/CLKEN	142	IO198NB6F18	76	IO242NB7F22	24
IO159PB4F14/CLKEP	143	IO198PB6F18	77	IO242PB7F22	25
IO160NB4F14/CLKFN	136	IO203NB6F19	72	IO244NB7F22	22
IO160PB4F14/CLKFP	137	IO203PB6F19	73	IO244PB7F22	23
Bank 5		IO204NB6F19	70	IO245NB7F22	18
IO161NB5F15/CLKGN	128	IO204PB6F19	71	IO245PB7F22	19
IO161PB5F15/CLKGP	129	IO205NB6F19	66	IO246NB7F22	16
IO162NB5F15/CLKHN	122	IO205PB6F19	67	IO246PB7F22	17
IO162PB5F15/CLKHP	123	IO206NB6F19	64	IO249NB7F23	12
IO167NB5F15	118	IO206PB6F19	65	IO249PB7F23	13
IO167PB5F15	119	IO207NB6F19	60	IO250NB7F23	10
IO183NB5F17	110	IO207PB6F19	61	IO250PB7F23	11
IO183PB5F17	111	IO208NB6F19	58	IO256NB7F23	4
IO184NB5F17	112	IO208PB6F19	59	IO256PB7F23	5
IO184PB5F17	113	IO211NB6F19	54	IO257NB7F23	6
IO185NB5F17	104	IO211PB6F19	55	IO257PB7F23	7
IO185PB5F17	105	IO212NB6F19	52	Dedicated I/O	
IO186NB5F17	106	IO212PB6F19	53	GND	1
IO186PB5F17	107	IO223NB6F20	48	GND	9
IO187NB5F17	98	IO223PB6F20	49	GND	15

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15

CG624



Note

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Revision	Changes	Page
Revision 12 (v2.4)	Revised ordering information and timing data to reflect phase out of –3 speed grade options.	
	Table 2-3 was updated.	2
Revision 11 (v2.3)	The "Packaging Data" section is new.	iv
	Table 2-2 was updated.	2-1
	"VCCDA Supply Voltage" was updated.	2-9
	"PRA/B/C/D Probe A, B, C and D" was updated.	2-10
	The "User I/Os" was updated.	2-11
Revision 10 (v2.2)	Figure 1-3 was updated.	1-2
	Table 2-2 was updated.	2-1
	The "Power-Up/Down Sequence" section was updated.	2-1
	Table 2-4 was updated.	2-3
	Table 2-5 was updated.	2-4
	The "Timing Characteristics" section was added.	2-7
	Table 2-7 was updated.	2-7
	Figure 2-1 was updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) equations in the "Hardwired Clock – Using LVTTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The External Setup and Clock-to-Out (Pad-to-Pad) in the "Routed Clock – Using LVTTTL 24 mA High Slew Clock I/O" section were updated.	2-8
	The "Global Pins" section was updated.	2-10
	The "User I/Os" section was updated.	2-11
	Table 2-17 was updated.	2-19
	Figure 2-8 was updated.	2-20
	Figure 2-13 and Figure 2-14 were updated.	2-24
	The following timing parameters were renamed in I/O timing characteristic tables from Table 2-22 to Table 2-60: $t_{IOCLKQ} > t_{CLKQ}$ $t_{IOCLKY} > t_{OCLKQ}$	2-26 to 2-52
	Timing numbers were updated from Table 2-22 to Table 2-78.	2-26 to 2-69
	The "R-Cell" section was updated.	2-58
	Figure 2-59 was updated.	2-89
	Figure 2-60 was updated.	2-89
	Figure 2-67 was updated.	2-100
	Figure 2-68 was updated.	2-101
	Table 2-89 to Table 2-93 were updated.	2-90 to 2-94
	Table 2-98 to Table 2-102 were updated.	2-102 to 2-106