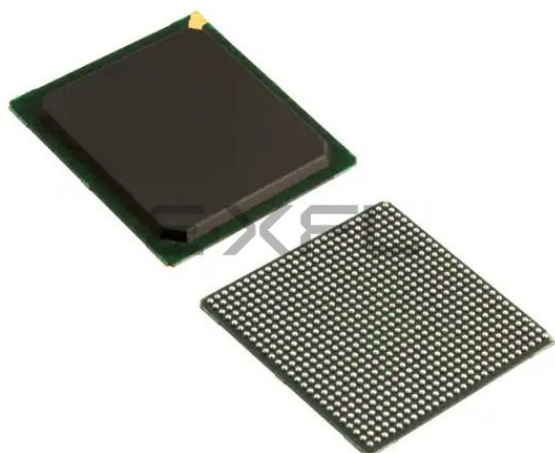




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

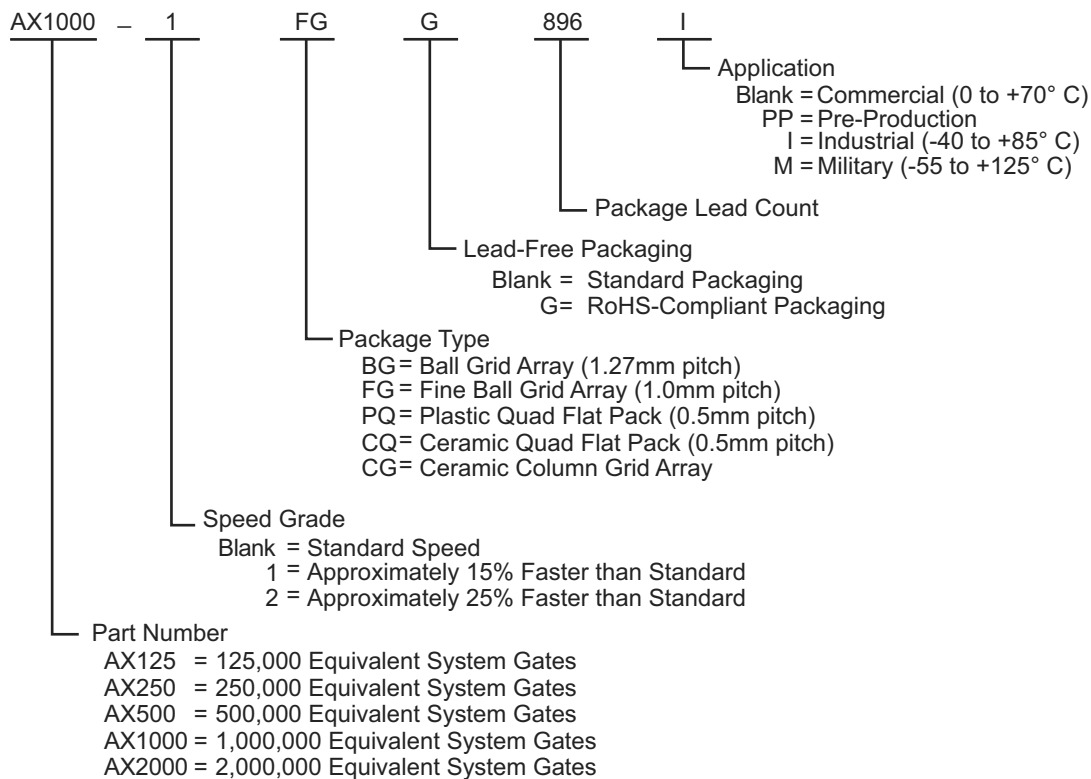
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	336
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-2fgg676i

Ordering Information



Device Resources

User I/Os (Including Clock Buffers)					
Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	115	115	–	–
CQ208	–	115	115	–	–
CQ256	–	–	–	–	136
FG256	138	138	–	–	–
FG324	168	–	–	–	–
CQ352	–	198	198	198	198
FG484	–	248	317	317	–
CG624	–	–	–	418	418
FG676	–	–	336	418	–
BG729	–	–	–	516	–
FG896	–	–	–	516	586
FG1152	–	–	–	–	684

Note: The FG256, FG324, and FG484 are footprint compatible with one another. The FG676, FG896, and FG1152 are also footprint compatible with one another.

The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6 on page 1-4).

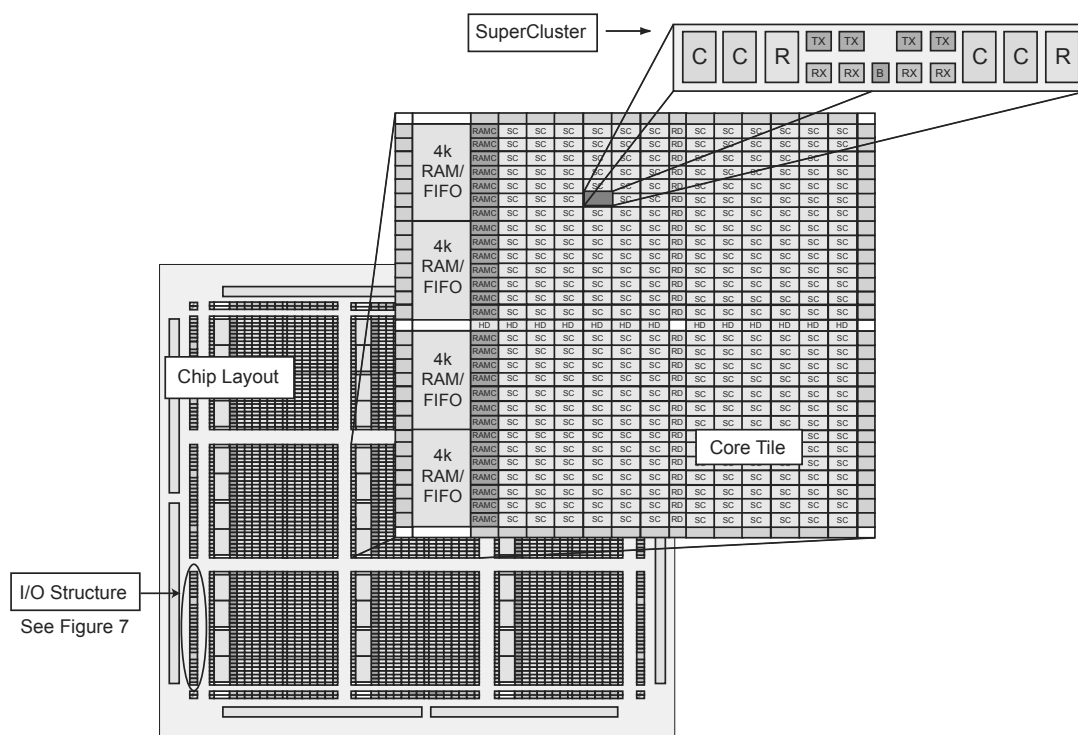


Figure 1-6 • AX Device Architecture (AX1000 shown)

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-5). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

I/O Standard Electrical Specifications

Table 2-18 • Input Capacitance

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		10	pF

Table 2-19 • I/O Input Rise Time and Fall Time*

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTTL	No Requirement	50 ns
LVC MOS 2.5V	No Requirement	50 ns
LVC MOS 1.8V	No Requirement	50 ns
LVC MOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

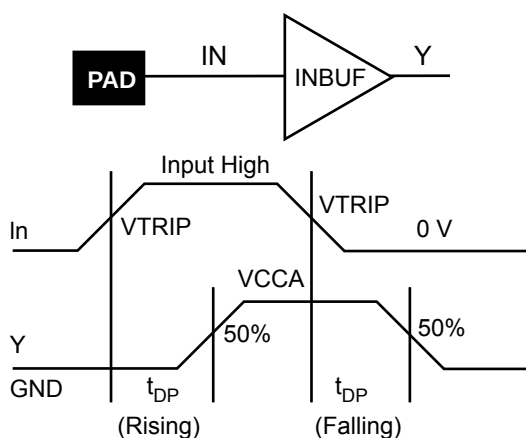


Figure 2-9 • Input Buffer Delays

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5 V tolerant with the aid of external components. Axcelerator 3.3 V PCI and 3.3 V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, -3.5 V in undershoot, and 7.1 V in overshoot.

Table 2-33 • DC Input and Output Levels

	VIL		VIH		VOL	VOH	IOL	IOH
	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
PCI	-0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	-0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

AC Loadings

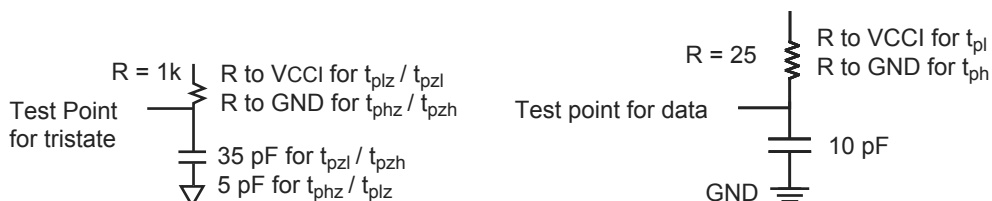


Figure 2-18 • AC Test Loads

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note: * Measuring Point = VTRIP

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

Table 2-41 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCC – 0.4	8	-8

AC Loadings

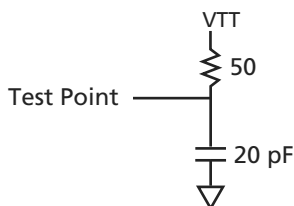


Figure 2-20 • AC Test Loads

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 0.5	VREF + 0.5	VREF	0.75	20

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-43 • 1.5 V HSTL Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.425 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
1.5 V HSTL Class I I/O Module Timing								
t _{DP}	Input Buffer		1.80		2.05		2.41	ns
t _{PY}	Output Buffer		4.90		5.58		6.56	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

PLL Configurations

The following rules apply to the different PLL inputs and outputs:

Reference Clock

The RefCLK can be driven by (Figure 2-50):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. CLK1 output of an adjacent PLL
3. [H]CLKxP (single-ended or voltage-referenced)
4. [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Feedback Clock

The feedback clock can be driven by (Figure 2-51 on page 2-78):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
3. An internal signal from the PLL block

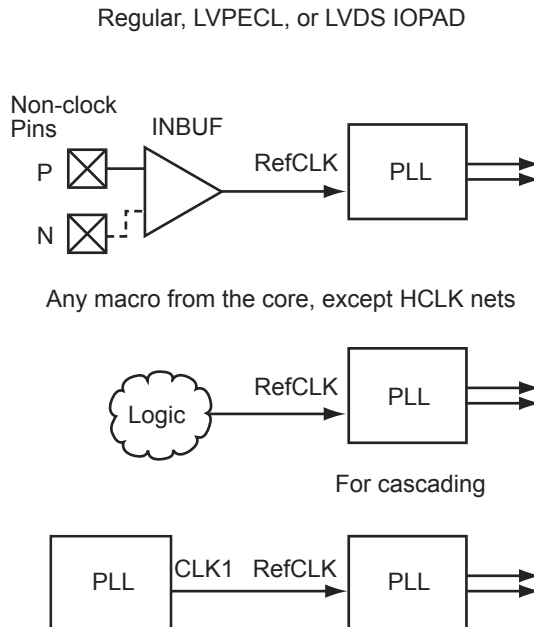


Figure 2-50 • Reference Clock Connections

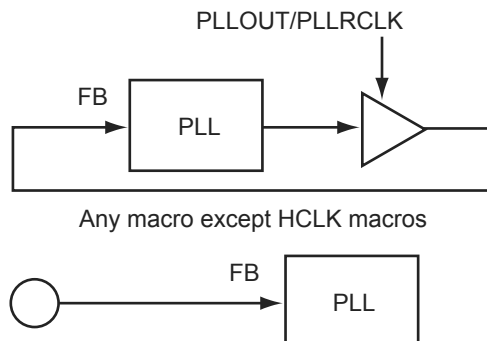


Figure 2-51 • Feedback Clock Connections

Table 2-102 • Sixteen FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		16.32		18.60		21.86	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		13.40		13.40		13.40	ns
t _{WCKP}	Minimum WCLK Period	14.15		14.15		14.15		ns
t _{RSU}	Read Setup		17.16		19.54		22.97	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		14.41		14.41		14.41	ns
t _{RCKP}	Minimum RCLK period	15.14		15.14		15.14		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		12.08		13.76		16.17	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		12.83		14.62		17.18	ns

Note: Timing data for these sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, use Microsemi's timing software.

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen Core Generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (refer to the *SmartGen*, *FlashROM*, *Analog System Builder*, and *Flash Memory System Builder* User's Guide for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Low Power Mode

Although designed for high performance, the AX architecture also allows the user to place the device into a low power mode. Each I/O bank in an Axcelerator device can be configured individually, when in low power mode, to tristate all outputs, disable inputs, or both. The low power mode is activated by asserting the LP pin, which is grounded in normal operation.

While in the low power mode, the device is still fully functional and all internal logic states are preserved. This allows a user to disable all but a few signals and operate the part in a low-frequency, watchdog

BG729		BG729		BG729	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
IO218PB6F20	V2	IO236PB7F22	L1	IO255NB7F23	F5
IO219NB6F20	T1	IO237NB7F22	L4	IO255PB7F23	G5
IO219PB6F20	U1	IO237PB7F22	L3	IO256NB7F23	F3
IO220NB6F20	R5	IO238NB7F22	L6	IO256PB7F23	F4
IO220PB6F20	R6	IO238PB7F22	M6	IO257NB7F23	H7
IO221NB6F20	T3	IO239NB7F22	M8	IO257PB7F23	J7
IO221PB6F20	T4	IO239PB7F22	M7	Dedicated I/O	
IO222NB6F20	R2	IO240NB7F22	K2	GND	A1
IO222PB6F20	T2	IO240PB7F22	K1	GND	A2
IO223NB6F20	P8	IO241NB7F22	K4	GND	A25
IO223PB6F20	P9	IO241PB7F22	K3	GND	A26
IO224NB6F20	R3	IO242NB7F22	K5	GND	A27
IO224PB6F20	R4	IO242PB7F22	L5	GND	A3
Bank 7		IO243NB7F22	J2	GND	AC24
IO225NB7F21	P1	IO243PB7F22	J1	GND	AE1
IO225PB7F21	R1	IO244NB7F22	J4	GND	AE2
IO226NB7F21	P3	IO244PB7F22	J3	GND	AE25
IO226PB7F21	P2	IO245NB7F22	H2	GND	AE26
IO227NB7F21	N7	IO245PB7F22	H1	GND	AE27
IO227PB7F21	P7	IO246NB7F22	H4	GND	AE3
IO228NB7F21	P5	IO246PB7F22	H3	GND	AE5
IO228PB7F21	P4	IO247NB7F23	L8	GND	AF1
IO229NB7F21	N2	IO247PB7F23	L7	GND	AF2
IO229PB7F21	N1	IO248NB7F23	J6	GND	AF25
IO230NB7F21	N6	IO248PB7F23	K6	GND	AF26
IO230PB7F21	P6	IO249NB7F23	H5	GND	AF27
IO231NB7F21	N9	IO249PB7F23	J5	GND	AF3
IO231PB7F21	N8	IO250NB7F23	G2	GND	AG1
IO232NB7F21	N4	IO250PB7F23	G1	GND	AG2
IO232PB7F21	N3	IO251NB7F23	K8	GND	AG25
IO233NB7F21	M2	IO251PB7F23	K7	GND	AG26
IO233PB7F21	M1	IO252NB7F23	G4	GND	AG27
IO234NB7F21	M4	IO252PB7F23	G3	GND	AG3
IO234PB7F21	M3	IO253NB7F23	F2	GND	B1
IO235NB7F21	M5	IO253PB7F23	F1	GND	B2
IO235PB7F21	N5	IO254NB7F23	G6	GND	B25
IO236NB7F22	L2	IO254PB7F23	H6	GND	B26

FG484		FG484	
AX250 Function	Pin Number	AX250 Function	Pin Number
VCCPLH	T10	VCCIB4	R14
VCCDA	D14	VCCIB5	AA3
VCCDA	D5	VCCIB5	AB3
VCCDA	F16	VCCIB5	R10
VCCDA	G12	VCCIB5	R11
VCCDA	L4	VCCIB5	R9
VCCDA	M18	VCCIB6	M8
VCCDA	T11	VCCIB6	N8
VCCDA	T17	VCCIB6	P8
VCCDA	U7	VCCIB6	Y1
VCCDA	V14	VCCIB6	Y2
VCCDA	V8	VCCIB7	C1
VCCIB0	A3	VCCIB7	C2
VCCIB0	B3	VCCIB7	J8
VCCIB0	H10	VCCIB7	K8
VCCIB0	H11	VCCIB7	L8
VCCIB0	H9	VCOMPLA	D10
VCCIB1	A20	VCOMPLB	G10
VCCIB1	B20	VCOMPLC	E12
VCCIB1	H12	VCOMPLD	G14
VCCIB1	H13	VCOMPLE	W13
VCCIB1	H14	VCOMPLF	T13
VCCIB2	C21	VCOMPLG	V11
VCCIB2	C22	VCOMPLH	T9
VCCIB2	J15	VPUMP	D17
VCCIB2	K15		
VCCIB2	L15		
VCCIB3	M15		
VCCIB3	N15		
VCCIB3	P15		
VCCIB3	Y21		
VCCIB3	Y22		
VCCIB4	AA20		
VCCIB4	AB20		
VCCIB4	R12		
VCCIB4	R13		

FG676	
AX1000 Function	Pin Number
IO129PB4F12	AA21
IO131NB4F12	AD22
IO131PB4F12	AD23
IO132NB4F12	AE23
IO132PB4F12	AE24
IO133NB4F12	AB20
IO133PB4F12	AA20
IO134NB4F12	AC21
IO134PB4F12	AC22
IO135NB4F12	AF22
IO135PB4F12	AF23
IO137NB4F12	AB19
IO137PB4F12	AA19
IO139NB4F13	AC19
IO139PB4F13	AC20
IO140NB4F13	AE21
IO140PB4F13	AE22
IO141NB4F13	AD20
IO141PB4F13	AD21
IO143NB4F13	AB17
IO143PB4F13	AB18
IO144NB4F13	AE19
IO144PB4F13	AE20
IO145NB4F13	AC17
IO145PB4F13	AC18
IO146NB4F13	AD18
IO146PB4F13	AD19
IO147NB4F13	AA17
IO147PB4F13	AA18
IO148NB4F13	AF20
IO148PB4F13	AF21
IO149NB4F13	AA16
IO149PB4F13	Y16
IO151NB4F13	AC16
IO151PB4F13	AB16
IO153NB4F14	AE17

FG676	
AX1000 Function	Pin Number
IO153PB4F14	AE18
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AA15
IO155PB4F14	Y15
IO157NB4F14	AC15
IO157PB4F14	AB15
IO159NB4F14/CLKEN	AE16
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AE14
IO160PB4F14/CLKFP	AE15
Bank 5	
IO161NB5F15/CLKGN	AE12
IO161PB5F15/CLKGP	AE13
IO162NB5F15/CLKHN	AE11
IO162PB5F15/CLKHP	AF11
IO163NB5F15	AC12
IO163PB5F15	AB12
IO165NB5F15	Y12
IO165PB5F15	AA13
IO167NB5F15	Y11
IO167PB5F15	AA12
IO168NB5F15	AF9
IO168PB5F15	AF10
IO169NB5F15	AB11
IO169PB5F15	AA11
IO171NB5F16	AE9
IO171PB5F16	AE10
IO173NB5F16	AC10
IO173PB5F16	AC11
IO174NB5F16	AE7
IO174PB5F16	AE8
IO175NB5F16	AC9
IO175PB5F16	AD9
IO176NB5F16	AF6
IO176PB5F16	AF7

FG676	
AX1000 Function	Pin Number
IO177NB5F16	AA10
IO177PB5F16	AB10
IO179NB5F16	AD7
IO179PB5F16	AD8
IO180NB5F16	AC7
IO180PB5F16	AC8
IO181NB5F17	AA9
IO181PB5F17	AB9
IO183NB5F17	AD6
IO183PB5F17	AE6
IO184NB5F17	AE5
IO184PB5F17	AF5
IO185NB5F17	AA8
IO185PB5F17	AB8
IO187NB5F17	AC5
IO187PB5F17	AC6
IO188NB5F17	AD4
IO188PB5F17	AD5
IO189NB5F17	AB6
IO189PB5F17	AB7
IO190NB5F17	AF4
IO190PB5F17	AE4
IO191NB5F17	AE3
IO191PB5F17	AF3
IO192NB5F17	AA6
IO192PB5F17	AA7
Bank 6	
IO193NB6F18	Y5
IO193PB6F18	AA5
IO194NB6F18	AB3
IO194PB6F18	AC3
IO195NB6F18	Y4
IO195PB6F18	AA4
IO196NB6F18	AC2
IO196PB6F18	AD2
IO197NB6F18	W6

FG896	
AX1000 Function	Pin Number
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13

FG896	
AX1000 Function	Pin Number
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12

FG896	
AX1000 Function	Pin Number
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3

FG896	
AX2000 Function	Pin Number
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	Pin Number
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO51PB1F4	J20	IO69NB1F6	C27	IO86NB2F8	J28
IO52NB1F4	B20	IO69PB1F6	C26	IO86PB2F8	J27
IO52PB1F4	A20	IO70NB1F6	H24	IO87NB2F8	M25
IO53NB1F4	F20	IO70PB1F6	G24	IO87PB2F8	L25
IO53PB1F4	E20	IO71NB1F6	H23	IO88NB2F8	L26
IO54NB1F5	B21	IO71PB1F6	G23	IO88PB2F8	K26
IO54PB1F5	A21	IO72NB1F6	B28	IO89NB2F8	G31
IO55NB1F5	K21	IO72PB1F6	A28	IO89PB2F8	F31
IO55PB1F5	J21	IO73NB1F6	E26	IO90NB2F8	H29
IO56NB1F5	D21	IO73PB1F6	E25	IO90PB2F8	G29
IO56PB1F5	C21	IO74NB1F6	F26	IO91NB2F8	K28
IO57NB1F5	G22	IO74PB1F6	F25	IO91PB2F8	K27
IO57PB1F5	G21	IO75NB1F6	K25	IO92NB2F8	J30
IO58NB1F5	E22	IO75PB1F6	K24	IO92PB2F8	H30
IO58PB1F5	E21	IO76NB1F7	D27	IO93NB2F8	L28
IO59NB1F5	D22	IO76PB1F7	D26	IO93PB2F8	L27
IO59PB1F5	C22	IO77NB1F7	B29	IO94NB2F8	K29
IO60NB1F5	B23	IO77PB1F7	A29	IO94PB2F8	J29
IO60PB1F5	A23	IO78NB1F7	D28	IO95NB2F8	K31
IO61NB1F5	H22	IO78PB1F7	C28	IO95PB2F8	J31
IO61PB1F5	H21	IO79NB1F7	H25	IO96NB2F9	J32
IO62NB1F5	C24	IO79PB1F7	G25	IO96PB2F9	H32
IO62PB1F5	C23	IO80NB1F7	F27	IO97NB2F9	M27
IO63NB1F5	F23	IO80PB1F7	E27	IO97PB2F9	M26
IO63PB1F5	F22	IO81NB1F7	J25	IO98NB2F9	L30
IO64NB1F6	B24	IO81PB1F7	J24	IO98PB2F9	K30
IO64PB1F6	A24	IO82NB1F7	D29	IO99NB2F9	N25
IO65NB1F6	J22	IO82PB1F7	C29	IO99PB2F9	N26
IO65PB1F6	K22	IO83NB1F7	H26	IO100NB2F9	M29
IO66NB1F6	B25	IO83PB1F7	G26	IO100PB2F9	L29
IO66PB1F6	A25	IO84NB1F7	F28	IO101NB2F9	L33
IO67NB1F6	K23	IO84PB1F7	E28	IO101PB2F9	L32
IO67PB1F6	J23	IO85NB1F7	H27	IO102NB2F9	K34
IO68NB1F6	F24	IO85PB1F7	G27	IO102PB2F9	K33
IO68PB1F6	E24	Bank 2		IO103NB2F9	N28

CQ208	
AX500 Function	Pin Number
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX500 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352		CQ352		CQ352	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
Bank 0		IO35NB1F3	275	Bank 3	
IO00PB0F0	343	IO35PB1F3	276	IO63NB3F6	217
IO03NB0F0	341	IO37NB1F3	271	IO63PB3F6	218
IO03PB0F0	342	IO37PB1F3	272	IO64NB3F6	219
IO05NB0F0	337	IO41NB1F3	269	IO64PB3F6	220
IO05PB0F0	338	IO41PB1F3	270	IO65NB3F6	213
IO07NB0F0	335	Bank 2		IO65PB3F6	214
IO07PB0F0	336	IO43NB2F4	261	IO67NB3F6	207
IO09NB0F0	331	IO43PB2F4	262	IO67PB3F6	208
IO09PB0F0	332	IO45NB2F4	259	IO68NB3F6	211
IO15NB0F1	325	IO45PB2F4	260	IO68PB3F6	212
IO15PB0F1	326	IO47NB2F4	255	IO69NB3F6	205
IO17NB0F1	323	IO47PB2F4	256	IO69PB3F6	206
IO17PB0F1	324	IO49NB2F4	253	IO71NB3F6	201
IO19NB0F1/HCLKAN	319	IO49PB2F4	254	IO71PB3F6	202
IO19PB0F1/HCLKAP	320	IO50NB2F4	247	IO73NB3F6	199
IO20NB0F1/HCLKBN	313	IO50PB2F4	248	IO73PB3F6	200
IO20PB0F1/HCLKBP	314	IO51NB2F4	249	IO75NB3F7	193
Bank 1		IO51PB2F4	250	IO75PB3F7	194
IO21NB1F2/HCLKCN	305	IO53NB2F5	243	IO76NB3F7	195
IO21PB1F2/HCLKCP	306	IO53PB2F5	244	IO76PB3F7	196
IO22NB1F2/HCLKDN	299	IO54NB2F5	241	IO77NB3F7	189
IO22PB1F2/HCLKDP	300	IO54PB2F5	242	IO77PB3F7	190
IO23NB1F2	289	IO55NB2F5	237	IO79NB3F7	187
IO23PB1F2	290	IO55PB2F5	238	IO79PB3F7	188
IO24NB1F2	295	IO57NB2F5	235	IO80NB3F7	183
IO24PB1F2	296	IO57PB2F5	236	IO80PB3F7	184
IO25NB1F2	287	IO58NB2F5	231	IO81NB3F7	181
IO25PB1F2	288	IO58PB2F5	232	IO81PB3F7	182
IO27NB1F2	283	IO59NB2F5	229	IO83NB3F7	179
IO27PB1F2	284	IO59PB2F5	230	IO83PB3F7	180
IO29NB1F2	281	IO61NB2F5	225	Bank 4	
IO29PB1F2	282	IO61PB2F5	226	IO85NB4F8	172
IO31NB1F2	277	IO62NB2F5	223	IO85PB4F8	173
IO31PB1F2	278	IO62PB2F5	224	IO87NB4F8	170

CQ352	
AX2000 Function	Pin Number
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100

CQ352	
AX2000 Function	Pin Number
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49

CQ352	
AX2000 Function	Pin Number
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0					
IO00NB0F0	F8	IO23NB0F2	E11	IO42NB1F4	G21
IO00PB0F0	F7	IO23PB0F2	F11	IO42PB1F4	G20
IO02NB0F0	G7	IO24NB0F2	D7	IO43NB1F4	A16
IO02PB0F0	G6	IO24PB0F2	E7	IO43PB1F4	A15
IO04NB0F0	E9	IO25PB0F2	B12	IO44NB1F4	A20
IO04PB0F0	D8	IO26NB0F2	H11	IO44PB1F4	A19
IO06NB0F0	G9	IO26PB0F2	G11	IO45NB1F4	B17
IO06PB0F0	G8	IO27NB0F2	C11	IO45PB1F4	B16
IO07PB0F0	B6	IO27PB0F2	B8	IO46NB1F4	G17
IO08NB0F0	F10	IO28NB0F2	J13	IO46PB1F4	H17
IO08PB0F0	F9	IO28PB0F2	K13	IO47NB1F4	A17
IO09PB0F0	C7	IO29NB0F2	J8	IO48NB1F4	C19
IO10NB0F0	H8	IO29PB0F2	J7	IO48PB1F4	C18
IO10PB0F0	H7	IO30NB0F2/HCLKAN	G13	IO49NB1F4	B20
IO11NB0F0	D10	IO30PB0F2/HCLKAP	G12	IO49PB1F4	B19
IO11PB0F0	D9	IO31NB0F2/HCLKBN	C13	IO50NB1F4	H20
IO12NB0F1	B5	IO31PB0F2/HCLKBP	C12	IO50PB1F4	H19
IO12PB0F1	B4	Bank 1		IO51NB1F4	A22
IO13NB0F1	A7	IO32NB1F3/HCLKCN	G15	IO51PB1F4	A21
IO13PB0F1	A6	IO32PB1F3/HCLKCP	G14	IO52NB1F4	C21
IO14NB0F1	C9	IO33NB1F3/HCLKDN	B14	IO52PB1F4	C20
IO14PB0F1	C8	IO33PB1F3/HCLKDP	B13	IO53NB1F4	B22
IO15PB0F1	B7	IO34NB1F3	G16	IO53PB1F4	B21
IO16NB0F1	A5	IO34PB1F3	H16	IO54NB1F5	J18
IO16PB0F1	A4	IO35NB1F3	C17	IO54PB1F5	J19
IO17NB0F1	A9	IO35PB1F3	B18	IO55NB1F5	D18
IO17PB0F1	B9	IO36NB1F3	H18	IO55PB1F5	D17
IO18NB0F1	D12	IO36PB1F3	H15	IO56NB1F5	F20
IO18PB0F1	D11	IO37NB1F3	H13	IO56PB1F5	F19
IO20NB0F1	B11	IO38NB1F3	E15	IO58NB1F5	E17
IO20PB0F1	B10	IO38PB1F3	F15	IO58PB1F5	F17
IO21NB0F1	A11	IO39NB1F3	D14	IO60NB1F5	D20
IO21PB0F1	A10	IO39PB1F3	C14	IO60PB1F5	D19
IO22NB0F2	H10	IO40NB1F3	D16	IO62NB1F5	E18
IO22PB0F2	H9	IO40PB1F3	D15	IO62PB1F5	F18
		IO41NB1F4	F16	IO63NB1F5	G19

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
VCCA	U17	VCCIB2	D23	VCCIB7	E4
VCCA	U9	VCCIB2	E22	VCCIB7	K9
VCCA	Y4	VCCIB2	K17	VCCIB7	L9
VCCDA	A12	VCCIB2	L17	VCCIB7	M10
VCCDA	AA13	VCCIB2	M16	VCCPLA	E12
VCCDA	AA15	VCCIB3	AA22	VCCPLB	J12
VCCDA	AA7	VCCIB3	AB23	VCCPLC	E14
VCCDA	AC11	VCCIB3	AC24	VCCPLD	H14
VCCDA	AD11	VCCIB3	AC25	VCCPLE	Y14
VCCDA	AE17	VCCIB3	P16	VCCPLF	U14
VCCDA	B15	VCCIB3	R17	VCCPLG	Y12
VCCDA	C15	VCCIB3	T17	VCCPLH	U12
VCCDA	C6	VCCIB4	AB21	VCOMPLA	F12
VCCDA	D13	VCCIB4	AC22	VCOMPLB	H12
VCCDA	E13	VCCIB4	AD23	VCOMPLC	F14
VCCDA	E19	VCCIB4	AE23	VCOMPLD	J14
VCCDA	G5	VCCIB4	T14	VCOMPLE	AA14
VCCDA	N21	VCCIB4	U15	VCOMPLF	V14
VCCDA	N5	VCCIB4	U16	VCOMPLG	AA12
VCCDA	W21	VCCIB5	AB5	VCOMPLH	V12
VCCIB0	A3	VCCIB5	AC4	VPUMP	E20
VCCIB0	B3	VCCIB5	AD3		
VCCIB0	C4	VCCIB5	AE3		
VCCIB0	D5	VCCIB5	T12		
VCCIB0	J10	VCCIB5	U10		
VCCIB0	J11	VCCIB5	U11		
VCCIB0	K12	VCCIB6	AA4		
VCCIB1	A23	VCCIB6	AB3		
VCCIB1	B23	VCCIB6	AC1		
VCCIB1	C22	VCCIB6	AC2		
VCCIB1	D21	VCCIB6	P10		
VCCIB1	J15	VCCIB6	R9		
VCCIB1	J16	VCCIB6	T9		
VCCIB1	K14	VCCIB7	C1		
VCCIB2	C24	VCCIB7	C2		
VCCIB2	C25	VCCIB7	D3		

Revision	Changes	Page
Revision 17 (continued)	The C180 package was removed from product tables and the "Package Pin Assignments" section (PDN 0909).	3-1
	Package names used in the "Axcelerator Family Product Profile" and "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	i, 3-1
	The "Introduction" section for "User I/Os" was updated as follows: "The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os" (SARs 24181, 24309).	2-11
	Power values in Table 2-4 • Default CLOAD/VCCI were updated to reflect those of SmartPower (SAR 33945).	2-3
	Two parameter names were corrected in Figure 2-10 • Output Buffer Delays. One occurrence of t_{ENLZ} was changed to t_{ENZL} and one occurrence of t_{ENHZ} was changed to t_{ENZH} (SAR 33890).	2-22
	The "Timing Model" section was updated with new timing values. Timing tables in the "I/O Specifications" section were updated to include enable paths. Values in the timing tables in the "Voltage-Referenced I/O Standards" section and "Differential Standards" section were updated. Table 2-63 • R-Cell was updated (SAR 33945).	2-8, 2-26 to 2-53
	Figure 2-11 • Timing Model was replaced (SAR 33043).	2-23
	The timing tables for "RAM" and "FIFO" were updated (SAR 33945).	2-90 to 2-106
	"Data Registers (DRs)" values were modified for IDCODE and USERCODE (SARs 18257, 26406).	2-108
Revision 16 (v2.8, Oct. 2009)	The package diagram for the "CQ208" package was incorrect and has been replaced with the correct diagram (SARs 23865, 26345).	3-89
	The datasheet was updated to include AX2000-CQ2526 information.	N/A
	MIL-STD-883 Class B is no longer supported by Axcelerator FPGAs and as a result was removed.	N/A
Revision 15 (v2.7, Nov. 2008)	A footnote was added to the "Introduction" in the "Axcelerator Clock Management System" section.	2-75
	RoHS-compliant information was added to the "Ordering Information".	ii
Revision 14 (v2.6)	ACTgen was changed to SmartGen because ACTgen is obsolete.	N/A
	In Table 2-4, the units for the P_{LOAD} , P_{10} , and $P_{I/O}$ were updated from mW/MHz to mW/MHz.	2-3
	In the "Pin Descriptions" section, the HCLK and CLK descriptions were updated to include tie-off information.	2-9
	The "Global Resource Distribution" section was updated.	2-70
Revision 13 (v2.5)	The "CG624" table was updated.	3-116
	A note was added to Table 2-2.	2-1
Revision 13 (v2.5)	In the "Package Thermal Characteristics", the temperature was changed from 150°C to 125°C.	2-6

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Axcelerator Family Device Status" table on page iii, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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