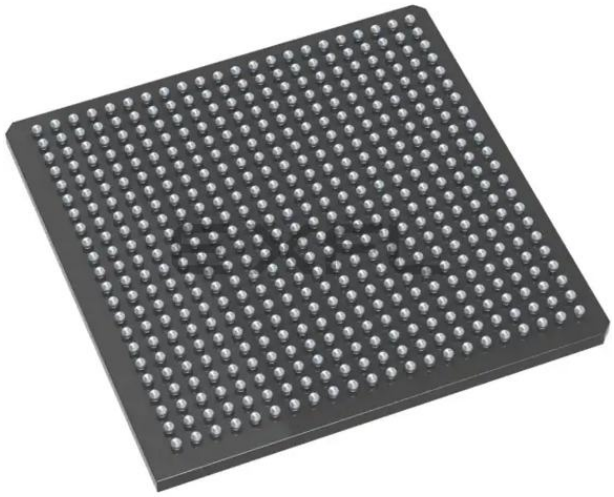

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 8064 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 73728 |
| Number of I/O | 317 |
| Number of Gates | 500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ax500-fg484 |

# Table of Contents

## I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

***Table 2-11 •*** **Compatible I/O Standards for Different VREF Values**

| VREF | Compatible Standards |
|---|---|
| 1.5 V | SSTL 3 (Class I and II) |
| 1.25 V | SSTL 2 (Class I and II) |
| 1.0 V | GTL+ (2.5V and 3.3V Outputs) |
| 0.75 V | HSTL (Class I) |

***Table 2-12 •*** **Compatible I/O Standards for Different VCCI Values**

| VCCI[1] | Compatible Standards | VREF |
|---|---|---|
| 3.3 V | LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V | 1.0 |
| 3.3 V | SSTL 3 (Class I and II), LVTTL, PCI, LVPECL | 1.5 |
| 2.5 V | LVCMOS 2.5 V, GTL+ 2.5 V, LVDS[2] | 1.0 |
| 2.5 V | LVCMOS 2.5 V, SSTL 2 (Classes I and II), LVDS[2] | 1.25 |
| 1.8 V | LVCMOS 1.8 V | N/A |
| 1.5 V | LVCMOS 1.5 V, HSTL Class I | 0.75 |

*Notes:*

1. *VCCI is used for both inputs and outputs*
2. *VCCI tolerance is* ±5%

# Axcelerator Clock Management System

## Introduction

Each member of the Axcelerator family[6] contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20µs

## Physical Implementation

The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. Figure 2-48 illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250 Ω resistor. Furthermore, 0.1 µF and 10 µF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

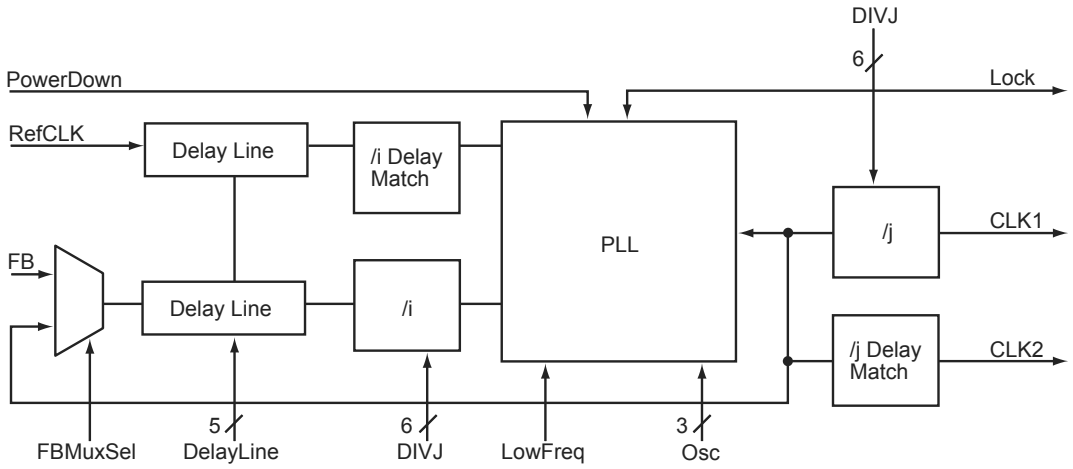


***Figure 2-48 •*** **PLL Block Diagram**

Note: The VCOMPPLL pin should never be grounded (Figure 2-2 on page 2-9)!

The I/O pads associated with the PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair,

6. *AX2000-CQ256 does not support operation of the phase-locked loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.*

# Programming

Device programming is supported through the Silicon Sculptor II, a single-site, robust and compact device programmer for the PC. Up to four Silicon Sculptor IIs can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor II to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor II also provides a self-test to test its own hardware extensively.

Programming an Axcelerator device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

1. Load the *.AFM file.
2. Select the device to be programmed.
3. Begin programming.

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via our In-House Programming Center.

In addition, BP Microsystems offers multi-site programmers that provide qualified support for Axcelerator devices.

For more details on programming the Axcelerator devices, please refer to the *Silicon Sculptor II User's Guide*.

| FG256-Pin FBGA | |
|---|---|
| **AX125 Function** | **Pin Number** |
| **Bank 6** | |
| IO60NB6F6 | L4 |
| IO60PB6F6 | M4 |
| IO61NB6F6 | L3 |
| IO61PB6F6 | M3 |
| IO63NB6F6 | P2 |
| IO63PB6F6 | N2 |
| IO64NB6F6 | J4 |
| IO64PB6F6 | K4 |
| IO65NB6F6 | N1 |
| IO65PB6F6 | P1 |
| IO67NB6F6 | L2 |
| IO67PB6F6 | M2 |
| IO69NB6F6 | L1 |
| IO69PB6F6 | M1 |
| IO70NB6F6 | J3 |
| IO70PB6F6 | K3 |
| IO71NB6F6 | J2 |
| IO71PB6F6 | K2 |
| **Bank 7** | |
| IO72NB7F7 | J1 |
| IO72PB7F7 | K1 |
| IO73NB7F7 | G2 |
| IO73PB7F7 | H2 |
| IO74NB7F7 | G3 |
| IO74PB7F7 | H3 |
| IO75NB7F7 | E1 |
| IO75PB7F7 | F1 |
| IO76NB7F7 | G1 |
| IO77NB7F7 | E2 |
| IO77PB7F7 | F2 |
| IO78NB7F7 | G4 |
| IO78PB7F7 | H4 |
| IO79NB7F7 | C1 |
| IO79PB7F7 | D1 |

| FG256-Pin FBGA | |
|---|---|
| **AX125 Function** | **Pin Number** |
| IO81NB7F7 | C2 |
| IO81PB7F7 | B1 |
| IO82NB7F7 | D2 |
| IO82PB7F7 | D3 |
| IO83NB7F7 | E3 |
| IO83PB7F7 | F3 |
| **Dedicated I/O** | |
| VCCDA | E4 |
| GND | A1 |
| GND | A16 |
| GND | B15 |
| GND | B2 |
| GND | D15 |
| GND | E12 |
| GND | E5 |
| GND | F11 |
| GND | F6 |
| GND | G10 |
| GND | G7 |
| GND | G8 |
| GND | G9 |
| GND | H10 |
| GND | H7 |
| GND | H8 |
| GND | H9 |
| GND | J10 |
| GND | J7 |
| GND | J8 |
| GND | J9 |
| GND | K10 |
| GND | K7 |
| GND | K8 |
| GND | K9 |
| GND | L11 |
| GND | L6 |

| FG256-Pin FBGA | |
|---|---|
| **AX125 Function** | **Pin Number** |
| GND | M12 |
| GND | M5 |
| GND | P13 |
| GND | P3 |
| GND | R15 |
| GND | R2 |
| GND | T1 |
| GND | T16 |
| GND/LP | D4 |
| NC | A11 |
| NC | R11 |
| NC | R5 |
| PRA | D8 |
| PRB | C8 |
| PRC | N9 |
| PRD | P9 |
| TCK | D5 |
| TDI | C6 |
| TDO | C4 |
| TMS | C3 |
| TRST | C5 |
| VCCA | D14 |
| VCCA | F10 |
| VCCA | F4 |
| VCCA | F7 |
| VCCA | F8 |
| VCCA | F9 |
| VCCA | G11 |
| VCCA | G6 |
| VCCA | H11 |
| VCCA | H6 |
| VCCA | J11 |
| VCCA | J6 |
| VCCA | K11 |
| VCCA | K6 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| IO104PB6F6 | N4 |
| IO105NB6F6 | M5 |
| IO105PB6F6 | N5 |
| IO106NB6F6 | M3 |
| IO106PB6F6 | N3 |
| **Bank 7** | |
| IO107NB7F7 | M2 |
| IO107PB7F7 | N1 |
| IO108NB7F7 | L3 |
| IO108PB7F7 | L2 |
| IO109NB7F7 | K2 |
| IO109PB7F7 | K1 |
| IO110NB7F7 | K5 |
| IO110PB7F7 | L5 |
| IO111NB7F7 | K6 |
| IO111PB7F7 | L6 |
| IO112NB7F7 | K4 |
| IO112PB7F7 | K3 |
| IO113NB7F7 | K7 |
| IO113PB7F7 | L7 |
| IO114NB7F7 | H1 |
| IO114PB7F7 | J1 |
| IO115NB7F7 | H2 |
| IO115PB7F7 | J2 |
| IO116NB7F7 | H4 |
| IO116PB7F7 | J4 |
| IO117NB7F7 | H5 |
| IO117PB7F7 | J5 |
| IO118NB7F7 | F2 |
| IO118PB7F7 | G2 |
| IO119NB7F7 | H6 |
| IO119PB7F7 | J6 |
| IO120NB7F7 | F1 |
| IO120PB7F7 | G1 |
| IO121NB7F7 | F4 |
| IO121PB7F7 | G4 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| IO122NB7F7 | G5 |
| IO122PB7F7 | G6 |
| IO123NB7F7 | F5 |
| IO123PB7F7 | E4 |
| **Dedicated I/O** | |
| VCCDA | H7 |
| GND | A1 |
| GND | A11 |
| GND | A12 |
| GND | A2 |
| GND | A21 |
| GND | A22 |
| GND | AA1 |
| GND | AA2 |
| GND | AA21 |
| GND | AA22 |
| GND | AB1 |
| GND | AB11 |
| GND | AB12 |
| GND | AB2 |
| GND | AB21 |
| GND | AB22 |
| GND | B1 |
| GND | B2 |
| GND | B21 |
| GND | B22 |
| GND | C20 |
| GND | C3 |
| GND | D19 |
| GND | D4 |
| GND | E18 |
| GND | E5 |
| GND | G18 |
| GND | H15 |
| GND | H8 |
| GND | J14 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| GND | J9 |
| GND | K10 |
| GND | K11 |
| GND | K12 |
| GND | K13 |
| GND | L1 |
| GND | L10 |
| GND | L11 |
| GND | L12 |
| GND | L13 |
| GND | L22 |
| GND | M1 |
| GND | M10 |
| GND | M11 |
| GND | M12 |
| GND | M13 |
| GND | M22 |
| GND | N10 |
| GND | N11 |
| GND | N12 |
| GND | N13 |
| GND | P14 |
| GND | P9 |
| GND | R15 |
| GND | R8 |
| GND | U16 |
| GND | U6 |
| GND | V18 |
| GND | V5 |
| GND | W19 |
| GND | W4 |
| GND | Y20 |
| GND | Y3 |
| GND/LP | G7 |
| NC | A17 |
| NC | A18 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| NC | A19 |
| NC | A4 |
| NC | A5 |
| NC | AA11 |
| NC | AA12 |
| NC | AA18 |
| NC | AA19 |
| NC | AA4 |
| NC | AB16 |
| NC | AB17 |
| NC | AB4 |
| NC | AB7 |
| NC | AB8 |
| NC | B11 |
| NC | B12 |
| NC | B17 |
| NC | B18 |
| NC | B19 |
| NC | B4 |
| NC | B5 |
| NC | C10 |
| NC | C11 |
| NC | C14 |
| NC | C15 |
| NC | C18 |
| NC | C19 |
| NC | D1 |
| NC | D2 |
| NC | D21 |
| NC | D3 |
| NC | E1 |
| NC | E2 |
| NC | E21 |
| NC | E3 |
| NC | F22 |
| NC | F3 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| NC | G22 |
| NC | G3 |
| NC | H3 |
| NC | J3 |
| NC | K21 |
| NC | K22 |
| NC | N22 |
| NC | P22 |
| NC | R19 |
| NC | R22 |
| NC | T1 |
| NC | T22 |
| NC | U1 |
| NC | U2 |
| NC | U21 |
| NC | U22 |
| NC | V1 |
| NC | V2 |
| NC | V21 |
| NC | V22 |
| NC | V3 |
| NC | W1 |
| NC | W2 |
| NC | W21 |
| NC | W22 |
| NC | W3 |
| NC | Y10 |
| NC | Y11 |
| NC | Y12 |
| NC | Y13 |
| NC | Y15 |
| NC | Y16 |
| NC | Y17 |
| NC | Y18 |
| NC | Y8 |
| NC | Y9 |

| FG484 | |
|---|---|
| **AX250 Function** | **Pin Number** |
| PRA | G11 |
| PRB | F11 |
| PRC | T12 |
| PRD | U12 |
| TCK | G8 |
| TDI | F9 |
| TDO | F7 |
| TMS | F6 |
| TRST | F8 |
| VCCA | G17 |
| VCCA | J10 |
| VCCA | J11 |
| VCCA | J12 |
| VCCA | J13 |
| VCCA | J7 |
| VCCA | K14 |
| VCCA | K9 |
| VCCA | L14 |
| VCCA | L9 |
| VCCA | M14 |
| VCCA | M9 |
| VCCA | N14 |
| VCCA | N9 |
| VCCA | P10 |
| VCCA | P11 |
| VCCA | P12 |
| VCCA | P13 |
| VCCA | T6 |
| VCCA | U17 |
| VCCPLA | F10 |
| VCCPLB | G9 |
| VCCPLC | D13 |
| VCCPLD | G13 |
| VCCPLE | U13 |
| VCCPLF | T14 |
| VCCPLG | W10 |

| FG676 | |
|---|---|
| AX500 Function | Pin Number |
| IO102PB4F9 | AB15 |
| IO103NB4F9/CLKEN | AE16 |
| IO103PB4F9/CLKEP | AF16 |
| IO104NB4F9/CLKFN | AE14 |
| IO104PB4F9/CLKFP | AE15 |
| **Bank 5** | |
| IO105NB5F10/CLKGN | AE12 |
| IO105PB5F10/CLKGP | AE13 |
| IO106NB5F10/CLKHN | AE11 |
| IO106PB5F10/CLKHP | AF11 |
| IO107NB5F10 | Y12 |
| IO107PB5F10 | AA13 |
| IO108NB5F10 | AC12 |
| IO108PB5F10 | AB12 |
| IO109NB5F10 | AC10 |
| IO109PB5F10 | AC11 |
| IO110NB5F10 | AF9 |
| IO110PB5F10 | AF10 |
| IO111NB5F10 | Y11 |
| IO111PB5F10 | AA12 |
| IO112NB5F10 | AE9 |
| IO112PB5F10 | AE10 |
| IO113NB5F10 | AC9 |
| IO113PB5F10 | AD9 |
| IO114NB5F11 | AF6 |
| IO114PB5F11 | AF7 |
| IO115NB5F11 | AA10 |
| IO115PB5F11 | AB10 |
| IO116NB5F11 | AE7 |
| IO116PB5F11 | AE8 |
| IO117NB5F11 | AD7 |
| IO117PB5F11 | AD8 |
| IO118NB5F11 | AC7 |
| IO118PB5F11 | AC8 |
| IO119NB5F11 | AD6 |

| FG676 | |
|---|---|
| AX500 Function | Pin Number |
| IO119PB5F11 | AE6 |
| IO120NB5F11 | AE5 |
| IO120PB5F11 | AF5 |
| IO121NB5F11 | AF4 |
| IO121PB5F11 | AE4 |
| IO122NB5F11 | AC5 |
| IO122PB5F11 | AC6 |
| IO123NB5F11 | AD4 |
| IO123PB5F11 | AD5 |
| IO124NB5F11 | AB6 |
| IO124PB5F11 | AB7 |
| IO125NB5F11 | AE3 |
| IO125PB5F11 | AF3 |
| **Bank 6** | |
| IO126NB6F12 | AB3 |
| IO126PB6F12 | AC3 |
| IO127NB6F12 | AA2 |
| IO127PB6F12 | AB2 |
| IO128NB6F12 | AC2 |
| IO128PB6F12 | AD2 |
| IO129NB6F12 | Y1 |
| IO129PB6F12 | AA1 |
| IO130NB6F12 | Y3 |
| IO130PB6F12 | AA3 |
| IO131NB6F12 | U6 |
| IO131PB6F12 | V6 |
| IO132NB6F12 | W2 |
| IO132PB6F12 | Y2 |
| IO133NB6F12 | V4 |
| IO133PB6F12 | W4 |
| IO134NB6F12 | V3 |
| IO134PB6F12 | W3 |
| IO135NB6F12 | V1 |
| IO135PB6F12 | V2 |
| IO136NB6F13 | U4 |

| FG676 | |
|---|---|
| AX500 Function | Pin Number |
| IO136PB6F13 | U5 |
| IO137NB6F13 | T6 |
| IO137PB6F13 | T7 |
| IO138NB6F13 | T5 |
| IO138PB6F13 | T4 |
| IO139NB6F13 | R6 |
| IO139PB6F13 | R7 |
| IO140NB6F13 | T3 |
| IO140PB6F13 | U3 |
| IO141NB6F13 | U1 |
| IO141PB6F13 | U2 |
| IO142NB6F13 | R2 |
| IO142PB6F13 | T2 |
| IO143NB6F13 | P3 |
| IO143PB6F13 | R3 |
| IO144NB6F13 | P5 |
| IO144PB6F13 | P4 |
| IO145NB6F13 | P6 |
| IO145PB6F13 | P7 |
| IO146NB6F13 | R1 |
| IO146PB6F13 | T1 |
| **Bank 7** | |
| IO147NB7F14 | N6 |
| IO147PB7F14 | N7 |
| IO148NB7F14 | N5 |
| IO148PB7F14 | N4 |
| IO149NB7F14 | N2 |
| IO149PB7F14 | N3 |
| IO150NB7F14 | L1 |
| IO150PB7F14 | M1 |
| IO151NB7F14 | M2 |
| IO151PB7F14 | M3 |
| IO152NB7F14 | M5 |
| IO152PB7F14 | M4 |
| IO153NB7F14 | M7 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| GND | T12 |
| GND | T13 |
| GND | T14 |
| GND | T15 |
| GND | T16 |
| GND | T17 |
| GND | T18 |
| GND | T19 |
| GND | T28 |
| GND | T3 |
| GND | U12 |
| GND | U13 |
| GND | U14 |
| GND | U15 |
| GND | U16 |
| GND | U17 |
| GND | U18 |
| GND | U19 |
| GND | V1 |
| GND | V12 |
| GND | V13 |
| GND | V14 |
| GND | V15 |
| GND | V16 |
| GND | V17 |
| GND | V18 |
| GND | V19 |
| GND | V30 |
| GND | W12 |
| GND | W13 |
| GND | W14 |
| GND | W15 |
| GND | W16 |
| GND | W17 |
| GND | W18 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| GND | W19 |
| GND | Y11 |
| GND | Y20 |
| GND/LP | E4 |
| NC | A16 |
| NC | A26 |
| NC | A4 |
| NC | A6 |
| NC | AA30 |
| NC | AB1 |
| NC | AB30 |
| NC | AC2 |
| NC | AC29 |
| NC | AD1 |
| NC | AD2 |
| NC | AD30 |
| NC | AE1 |
| NC | AE15 |
| NC | AE16 |
| NC | AE2 |
| NC | AE30 |
| NC | AF1 |
| NC | AF2 |
| NC | AF29 |
| NC | AF30 |
| NC | AG1 |
| NC | AG2 |
| NC | AG29 |
| NC | AG30 |
| NC | AH27 |
| NC | AH4 |
| NC | AJ14 |
| NC | AJ15 |
| NC | AJ16 |
| NC | AJ27 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| NC | AJ4 |
| NC | AK14 |
| NC | AK15 |
| NC | AK16 |
| NC | AK17 |
| NC | AK22 |
| NC | AK4 |
| NC | AK5 |
| NC | B16 |
| NC | B18 |
| NC | B21 |
| NC | B23 |
| NC | B26 |
| NC | B4 |
| NC | B6 |
| NC | B8 |
| NC | C27 |
| NC | D1 |
| NC | D2 |
| NC | D29 |
| NC | D30 |
| NC | E1 |
| NC | E2 |
| NC | E29 |
| NC | E30 |
| NC | F15 |
| NC | F16 |
| NC | F29 |
| NC | F30 |
| NC | G1 |
| NC | G29 |
| NC | G30 |
| NC | H29 |
| NC | J1 |
| NC | J30 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| NC | K1 |
| NC | K2 |
| NC | L30 |
| NC | M30 |
| NC | N29 |
| NC | T1 |
| NC | U1 |
| NC | W30 |
| NC | Y1 |
| NC | Y2 |
| NC | Y30 |
| PRA | G15 |
| PRB | D16 |
| PRC | AB16 |
| PRD | AF16 |
| TCK | G7 |
| TDI | D5 |
| TDO | J8 |
| TMS | F6 |
| TRST | C4 |
| VCCA | AD6 |
| VCCA | AH26 |
| VCCA | E28 |
| VCCA | E3 |
| VCCA | L12 |
| VCCA | L13 |
| VCCA | L14 |
| VCCA | L15 |
| VCCA | L16 |
| VCCA | L17 |
| VCCA | L18 |
| VCCA | L19 |
| VCCA | M11 |
| VCCA | M20 |
| VCCA | N11 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| VCCA | N20 |
| VCCA | P11 |
| VCCA | P20 |
| VCCA | R11 |
| VCCA | R20 |
| VCCA | T11 |
| VCCA | T20 |
| VCCA | U11 |
| VCCA | U20 |
| VCCA | V11 |
| VCCA | V20 |
| VCCA | W11 |
| VCCA | W20 |
| VCCA | Y12 |
| VCCA | Y13 |
| VCCA | Y14 |
| VCCA | Y15 |
| VCCA | Y16 |
| VCCA | Y17 |
| VCCA | Y18 |
| VCCA | Y19 |
| VCCPLA | G14 |
| VCCPLB | H15 |
| VCCPLC | G17 |
| VCCPLD | J16 |
| VCCPLE | AH17 |
| VCCPLF | AC16 |
| VCCPLG | AH14 |
| VCCPLH | AD15 |
| VCCDA | AD24 |
| VCCDA | AD7 |
| VCCDA | AF12 |
| VCCDA | AF13 |
| VCCDA | AF15 |
| VCCDA | AF18 |

| FG896 | |
|---|---|
| AX1000 Function | Pin Number |
| VCCDA | AF19 |
| VCCDA | C13 |
| VCCDA | C5 |
| VCCDA | D13 |
| VCCDA | D19 |
| VCCDA | D3 |
| VCCDA | E18 |
| VCCDA | F26 |
| VCCDA | G16 |
| VCCDA | T25 |
| VCCDA | T4 |
| VCCIB0 | A3 |
| VCCIB0 | B3 |
| VCCIB0 | J10 |
| VCCIB0 | J11 |
| VCCIB0 | J12 |
| VCCIB0 | K11 |
| VCCIB0 | K12 |
| VCCIB0 | K13 |
| VCCIB0 | K14 |
| VCCIB0 | K15 |
| VCCIB1 | A28 |
| VCCIB1 | B28 |
| VCCIB1 | J19 |
| VCCIB1 | J20 |
| VCCIB1 | J21 |
| VCCIB1 | K16 |
| VCCIB1 | K17 |
| VCCIB1 | K18 |
| VCCIB1 | K19 |
| VCCIB1 | K20 |
| VCCIB2 | C29 |
| VCCIB2 | C30 |
| VCCIB2 | K22 |
| VCCIB2 | L21 |

| CG624 | |
|---|---|
| AX1000 Function | Pin Number |
| IO194NB6F18 | Y3 |
| IO194PB6F18 | AA3 |
| IO195NB6F18 | V6 |
| IO195PB6F18 | W4 |
| IO197NB6F18 | R5 |
| IO197PB6F18 | U3 |
| IO198NB6F18 | P6 |
| IO199NB6F18 | Y5 |
| IO199PB6F18 | W5 |
| IO200NB6F18 | V3 |
| IO200PB6F18 | W3 |
| IO201NB6F18 | T7 |
| IO201PB6F18 | U7 |
| IO202NB6F18 | V2 |
| IO203NB6F19 | W2 |
| IO203PB6F19 | Y2 |
| IO204NB6F19 | AA1 |
| IO204PB6F19 | AB1 |
| IO205NB6F19 | R6 |
| IO205PB6F19 | T6 |
| IO206NB6F19 | W1 |
| IO206PB6F19 | Y1 |
| IO207NB6F19 | T2 |
| IO207PB6F19 | U2 |
| IO208NB6F19 | T1 |
| IO208PB6F19 | U1 |
| IO209NB6F19 | AA2 |
| IO209PB6F19 | AB2 |
| IO210NB6F19 | P5 |
| IO211NB6F19 | M1 |
| IO211PB6F19 | N1 |
| IO212NB6F19 | P1 |
| IO212PB6F19 | R1 |
| IO213NB6F19 | R8 |
| IO213PB6F19 | T8 |
| IO215NB6F20 | U4 |

| CG624 | |
|---|---|
| AX1000 Function | Pin Number |
| IO215PB6F20 | V4 |
| IO216NB6F20 | P8 |
| IO216PB6F20 | R3 |
| IO217NB6F20 | P7 |
| IO217PB6F20 | R7 |
| IO219NB6F20 | R4 |
| IO219PB6F20 | T4 |
| IO220NB6F20 | P2 |
| IO220PB6F20 | R2 |
| IO221NB6F20 | N4 |
| IO221PB6F20 | P4 |
| IO223NB6F20 | M2 |
| IO223PB6F20 | N2 |
| IO224NB6F20 | N3 |
| IO224PB6F20 | P3 |
| **Bank 7** | |
| IO225NB7F21 | J2 |
| IO225PB7F21 | J1 |
| IO226PB7F21 | G2 |
| IO227NB7F21 | H3 |
| IO227PB7F21 | H2 |
| IO229NB7F21 | K2 |
| IO229PB7F21 | L2 |
| IO230NB7F21 | K1 |
| IO230PB7F21 | L1 |
| IO231NB7F21 | E2 |
| IO231PB7F21 | F2 |
| IO232NB7F21 | F1 |
| IO232PB7F21 | G1 |
| IO233NB7F21 | L3 |
| IO233PB7F21 | M3 |
| IO234NB7F21 | D1 |
| IO234PB7F21 | E1 |
| IO235NB7F21 | K4 |
| IO235PB7F21 | L4 |
| IO236NB7F22 | M6 |

| CG624 | |
|---|---|
| AX1000 Function | Pin Number |
| IO237NB7F22 | N8 |
| IO237PB7F22 | N7 |
| IO238NB7F22 | M5 |
| IO239NB7F22 | L6 |
| IO239PB7F22 | L5 |
| IO240NB7F22 | M4 |
| IO241NB7F22 | L7 |
| IO241PB7F22 | M7 |
| IO242NB7F22 | J3 |
| IO243NB7F22 | M9 |
| IO243PB7F22 | M8 |
| IO244NB7F22 | P9 |
| IO244PB7F22 | N6 |
| IO245NB7F22 | K8 |
| IO245PB7F22 | L8 |
| IO246NB7F22 | F3 |
| IO246PB7F22 | E3 |
| IO247NB7F23 | K7 |
| IO247PB7F23 | K6 |
| IO248NB7F23 | D2 |
| IO249NB7F23 | G4 |
| IO249PB7F23 | G3 |
| IO251NB7F23 | N10 |
| IO251PB7F23 | N9 |
| IO253NB7F23 | H4 |
| IO253PB7F23 | J4 |
| IO255NB7F23 | J6 |
| IO255PB7F23 | J5 |
| IO257NB7F23 | H5 |
| IO257PB7F23 | H6 |
| **Dedicated I/O** | |
| GND | K5 |
| GND | A18 |
| GND | A2 |
| GND | A24 |
| GND | A25 |

| CG624 | |
|---|---|
| **AX2000 Function** | **Pin Number** |
| IO310NB7F29 | N10 |
| IO310PB7F29 | N9 |
| IO311NB7F29 | K1 |
| IO311PB7F29 | L1 |
| IO313NB7F29 | M5 |
| IO316NB7F29 | L6 |
| IO316PB7F29 | L5 |
| IO317NB7F29 | K2 |
| IO317PB7F29 | L2 |
| IO318NB7F29 | K4 |
| IO318PB7F29 | L4 |
| IO320NB7F29 | J3 |
| IO321NB7F30 | J2 |
| IO321PB7F30 | J1 |
| IO323NB7F30 | L7 |
| IO323PB7F30 | M7 |
| IO324NB7F30 | M9 |
| IO324PB7F30 | M8 |
| IO327NB7F30 | F1 |
| IO327PB7F30 | G1 |
| IO328NB7F30 | K7 |
| IO328PB7F30 | K6 |
| IO329NB7F30 | D1 |
| IO329PB7F30 | E1 |
| IO331PB7F30 | G2 |
| IO332NB7F31 | H3 |
| IO332PB7F31 | H2 |
| IO333NB7F31 | E2 |
| IO333PB7F31 | F2 |
| IO334NB7F31 | H4 |
| IO334PB7F31 | J4 |
| IO335NB7F31 | H5 |

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

| CG624 | |
|---|---|
| **AX2000 Function** | **Pin Number** |
| IO335PB7F31 | H6 |
| IO337NB7F31 | D2 |
| IO338NB7F31 | J6 |
| IO338PB7F31 | J5 |
| IO339NB7F31 | F3 |
| IO339PB7F31 | E3 |
| IO340NB7F31 | G4* |
| IO340PB7F31 | G3* |
| IO341NB7F31 | K8 |
| IO341PB7F31 | L8 |
| **Dedicated I/O** | |
| GND | K5 |
| GND | A18 |
| GND | A2 |
| GND | A24 |
| GND | A25 |
| GND | A8 |
| GND | AA10 |
| GND | AA16 |
| GND | AA18 |
| GND | AA21 |
| GND | AA5 |
| GND | AB22 |
| GND | AB4 |
| GND | AC10 |
| GND | AC16 |
| GND | AC23 |
| GND | AC3 |
| GND | AD1 |
| GND | AD2 |
| GND | AD24 |
| GND | AD25 |

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

| CG624 | |
|---|---|
| **AX2000 Function** | **Pin Number** |
| GND | AE1 |
| GND | AE18 |
| GND | AE2 |
| GND | AE24 |
| GND | AE25 |
| GND | AE8 |
| GND | B1 |
| GND | B2 |
| GND | B24 |
| GND | B25 |
| GND | C10 |
| GND | C16 |
| GND | C23 |
| GND | C3 |
| GND | D22 |
| GND | D4 |
| GND | E10 |
| GND | E16 |
| GND | E21 |
| GND | E5 |
| GND | E8 |
| GND | H1 |
| GND | H21 |
| GND | H25 |
| GND | K21 |
| GND | K23 |
| GND | K3 |
| GND | L11 |
| GND | L12 |
| GND | L13 |
| GND | L14 |
| GND | L15 |

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

# 4 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Revision | Changes | Page |
|---|---|---|
| Revision 18 (March 2012) | Table 2-1 • Absolute Maximum Ratings was updated to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419). | 2-1 |
| | Values for tristate leakage current IOZ, and IIH and IIL were added to Table 2-3 • Standby Current (SARs 35774, 32021). | 2-2 |
| | Figure 2-2 • VCCPLX and VCOMPLX Power Supply Connect was updated to correct the units for the resistance from "W" to Ω (SAR 36415). | 2-9 |
| | In the Introduction to the "User I/Os" section, the following sentence was added to clarify the slew rate setting (SAR 34943):<br>The slew rate setting is effective for both rising and falling edges. | 2-11 |
| | Figure 2-3 • Use of an External Resistor for 5 V Tolerance was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942). | 2-13 |
| | EQ 3 for 5 V tolerance was corrected to change Vdiode from 0.6 V to 0.7 V (SAR 36786). | 2-13 |
| | Additional information was added to the "Using the Weak Pull-Up and Pull-Down Circuits" section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945). | 2-17 |
| | The description for the $C_{INCLK}$ parameter in Table 2-18 • Input Capacitance was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944). | 2-21 |
| | Table 2-19 • I/O Input Rise Time and Fall Time* is new (SAR 34942). | 2-21 |
| | The minimum VIL for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-29 • DC Input and Output Levels and Table 2-33 • DC Input and Output Levels (SAR 34358). | 2-38, 2-40 |
| | Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the *Antifuse Macro Library Guide* was added to the "R-Cell" section (SAR 26413). | 2-58 |
| | The enable signal in Figure 2-32 • R-Cell Delays was corrected to show it is active low rather than active high (SAR 34946). | 2-59 |
| Revision 17 (September 2011) | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "Axcelerator Family Device Status" table indicates the status for each device in the device family. | iii |
| | The "Features" section, "Programmable Interconnect Element" section, and "Security" section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865). | i, 1-1, 2-108 |

| Revision | Changes | Page |
|---|---|---|
| Revision 17 (continued) | The C180 package was removed from product tables and the "Package Pin Assignments" section (PDN 0909). | 3-1 |
| | Package names used in the"Axcelerator Family Product Profile" and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395). | i, 3-1 |
| | The "Introduction" section for "User I/Os" was updated as follows:<br>"The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os" (SARs 24181, 24309). | 2-11 |
| | Power values in Table 2-4 • Default CLOAD/VCCI were updated to reflect those of SmartPower (SAR 33945). | 2-3 |
| | Two parameter names were corrected in Figure 2-10 • Output Buffer Delays. One occurrence of $t_{ENLZ}$ was changed to $t_{ENZL}$ and one occurrence of $t_{ENHZ}$ was changed to $t_{ENZH}$ (SAR 33890). | 2-22 |
| | The "Timing Model" section was updated with new timing values. Timing tables in the "I/O Specifications" section were updated to include enable paths. Values in the timing tables in the "Voltage-Referenced I/O Standards" section and "Differential Standards" section were updated. Table 2-63 • R-Cell was updated (SAR 33945). | 2-8, 2-26 to 2-53 |
| | Figure 2-11 • Timing Model was replaced (SAR 33043). | 2-23 |
| | The timing tables for "RAM" and "FIFO" were updated (SAR 33945). | 2-90 to 2-106 |
| | "Data Registers (DRs)" values were modified for IDCODE and USERCODE (SARs 18257, 26406). | 2-108 |
| | The package diagram for the "CQ208" package was incorrect and has been replaced with the correct diagram (SARs 23865, 26345). | 3-89 |
| Revision 16 (v2.8, Oct. 2009) | The datasheet was updated to include AX2000-CQ2526 information. | N/A |
| | MIL-STD-883 Class B is no longer supported by Axcelerator FPGAs and as a result was removed. | N/A |
| | A footnote was added to the "Introduction" in the "Axcelerator Clock Management System" section. | 2-75 |
| Revision 15 (v2.7, Nov. 2008) | RoHS-compliant information was added to the "Ordering Information". | ii |
| | ACTgen was changed to SmartGen because ACTgen is obsolete. | N/A |
| Revision 14 (v2.6) | In Table 2-4, the units for the $P_{LOAD}$, $P_{10}$, and $P_{I/O}$ were updated from mW/MHz to mW/MHz. | 2-3 |
| | In the "Pin Descriptions"section, the HCLK and CLK descriptions were updated to include tie-off information. | 2-9 |
| | The "Global Resource Distribution" section was updated. | 2-70 |
| | The " CG624" table was updated. | 3-116 |
| Revision 13 (v2.5) | A note was added to Table 2-2. | 2-1 |
| | In the "Package Thermal Characteristics", the temperature was changed from 150°C to 125°C. | 2-6 |