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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	317
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-fg484i

Axcelerator Family Device Status

Axcelerator® Devices	Status
AX125	Production
AX250	Production
AX500	Production
AX1000	Production
AX2000	Production

Temperature Grade Offerings

Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	C, I, M	C, I, M	–	–
CQ208	–	M	M	–	–
CQ256	–	–	–	–	M
FG256	C, I	C, I, M	–	–	–
FG324	C, I	–	–	–	–
CQ352	–	M	M	M	M
FG484	–	C, I, M	C, I, M	C, I, M	–
CG624	–	–	–	M	M
FG676	–	–	C, I, M	C, I, M	–
BG729	–	–	–	C, I, M	–
FG896	–	–	–	C, I, M	C, I, M
FG1152	–	–	–	–	C, I, M

C = Commercial

I = Industrial

M = Military

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std	–1	–2
C	✓	✓	✓
I	✓	✓	✓
M	✓	✓	–

C = Commercial

I = Industrial

M = Military

2 – Detailed Specifications

Operating Conditions

Table 2-1 lists the absolute maximum ratings of Axcelerator devices. Stresses beyond the ratings may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommendations in Table 2-2.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCA	DC Core Supply Voltage	–0.3 to 1.7	V
VCCI	DC I/O Supply Voltage	–0.3 to 3.75	V
VREF	DC I/O Reference Voltage	–0.3 to 3.75	V
VI	Input Voltage	–0.5 to 4.1	V
VO	Output Voltage	–0.5 to 3.75	V
TSTG	Storage Temperature	–60 to +150	°C
VCCDA*	Supply Voltage for Differential I/Os	–0.3 to 3.75	V

Note: * Should be the maximum of all VCCI.

Table 2-2 • Recommended Operating Conditions

Parameter Range	Commercial	Industrial	Military	Units
Ambient Temperature (T_A) ¹	0 to +70	–40 to +85	–55 to +125	°C
1.5 V Core Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.5 V I/O Supply Voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.8 V I/O Supply Voltage	1.71 to 1.89	1.71 to 1.89	1.71 to 1.89	V
2.5 V I/O Supply Voltage	2.375 to 2.625	2.375 to 2.625	2.375 to 2.625	V
3.3 V I/O Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCDA Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VPUMP Supply Voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

Notes:

1. Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.
2. $T_J \text{ max} = 125^\circ\text{C}$

Power-Up/Down Sequence

All Axcelerator I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. VCCDA should be powered up before (or coincidentally with) VCCA and VCCI to ensure the behavior of user I/Os at system start-up. Conversely, VCCDA should be powered down after (or coincidentally with) VCCA and VCCI. Note that VCCI and VCCA can be powered up in any sequence with respect to each other, provided the requirement with respect to VCCDA is satisfied.

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

Table 2-11 • Compatible I/O Standards for Different VREF Values

VREF	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5V and 3.3V Outputs)
0.75 V	HSTL (Class I)

Table 2-12 • Compatible I/O Standards for Different VCCI Values

VCCI ¹	Compatible Standards	VREF
3.3 V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVC MOS 2.5 V, GTL+ 2.5 V, LVDS ²	1.0
2.5 V	LVC MOS 2.5 V, SSTL 2 (Classes I and II), LVDS ²	1.25
1.8 V	LVC MOS 1.8 V	N/A
1.5 V	LVC MOS 1.5 V, HSTL Class I	0.75

Notes:

1. VCCI is used for both inputs and outputs
2. VCCI tolerance is $\pm 5\%$

User I/O Naming Conventions

Due to the complex and flexible nature of the Axcelerator family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (Figure 2-7).

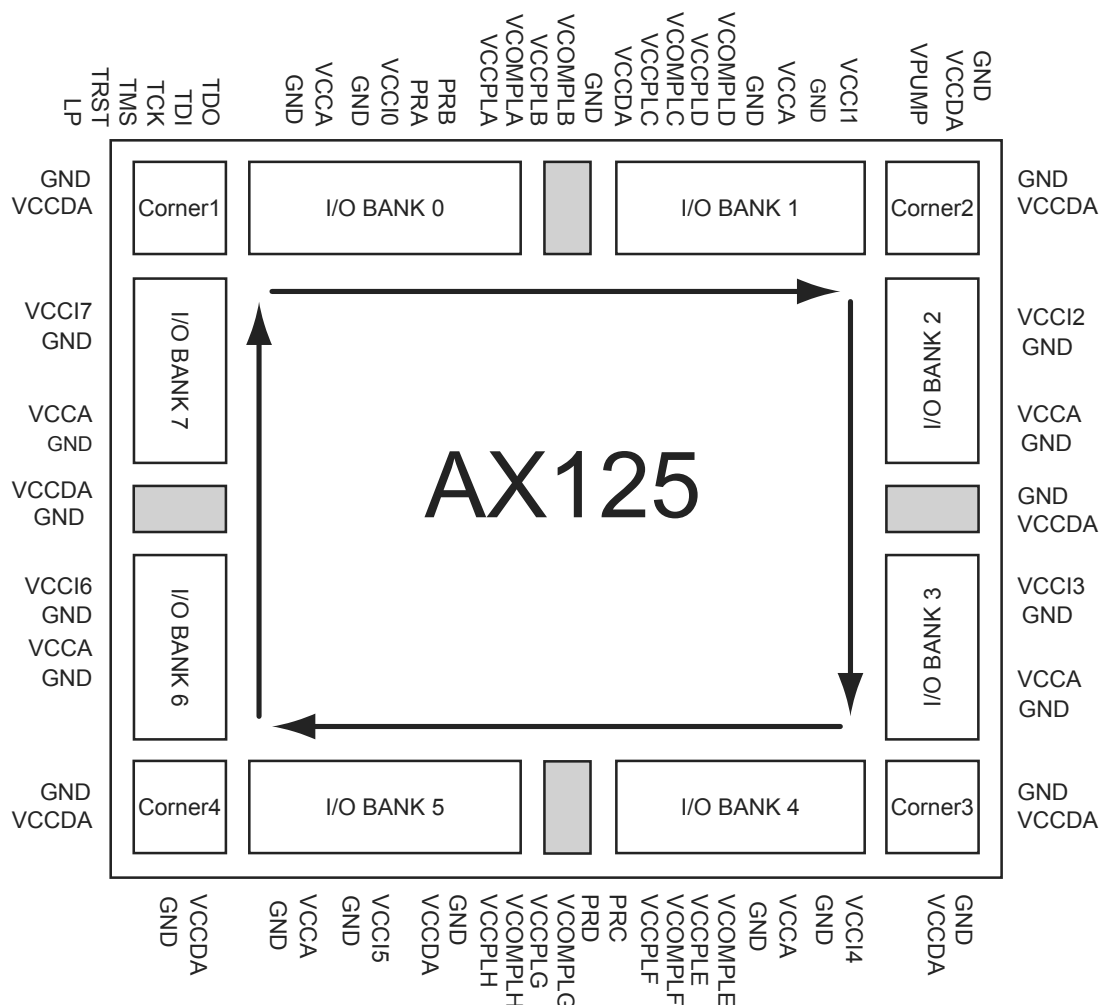
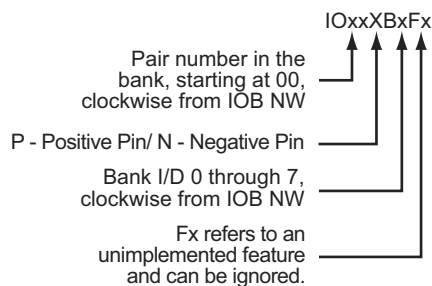


Figure 2-7 • I/O Bank and Dedicated Pin Layout



Examples:

IO12PB1F1 is the positive pin of the thirteenth pair of the first I/O bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair.

For those I/Os that can be employed either as a user I/O or as a special function, the following nomenclature is used:

IOxxXBxFx/special_function_name

IOxxPB1Fx/xCLKx this pin can be configured as a clock input or as a user I/O.

Figure 2-8 • General Naming Schemes

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 1 (8 mA) / High Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		4.23		4.81		5.66	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		4.64		5.28		6.21	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.23		4.81		5.66	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.01		2.02		2.03	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

Table 2-41 • DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
-0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCC – 0.4	8	-8

AC Loadings

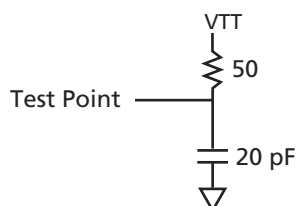


Figure 2-20 • AC Test Loads

Table 2-42 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C _{load} (pF)
VREF – 0.5	VREF + 0.5	VREF	0.75	20

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-43 • 1.5 V HSTL Class I I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.425 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
1.5 V HSTL Class I I/O Module Timing								
t _{DP}	Input Buffer		1.80		2.05		2.41	ns
t _{PY}	Output Buffer		4.90		5.58		6.56	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-57 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.2 – 0.125	1.2 + 0.125	1.2

Note: * Measuring Point = VTRIP

Timing Characteristics

Table 2-58 • LVDS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 2.3 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
LVDS Output Module Timing								
t _{DP}	Input Buffer	1.80		2.05		2.41		ns
t _{PY}	Output Buffer	2.32		2.64		3.11		ns
t _{CLKQ}	Clock-to-Q for the I/O input register	0.67		0.77		0.90		ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	0.67		0.77		0.90		ns
t _{SUD}	Data Input Set-Up	0.23		0.27		0.31		ns
t _{SUE}	Enable Input Set-Up	0.26		0.30		0.35		ns
t _{HD}	Data Input Hold	0.00		0.00		0.00		ns
t _{HE}	Enable Input Hold	0.00		0.00		0.00		ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time	0.13		0.15		0.17		ns
t _{HASYN}	Asynchronous Removal Time	0.00		0.00		0.00		ns
t _{CLR}	Asynchronous Clear-to-Q	0.23		0.27		0.31		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.23		0.27		0.31		ns

Timing Model and Waveforms

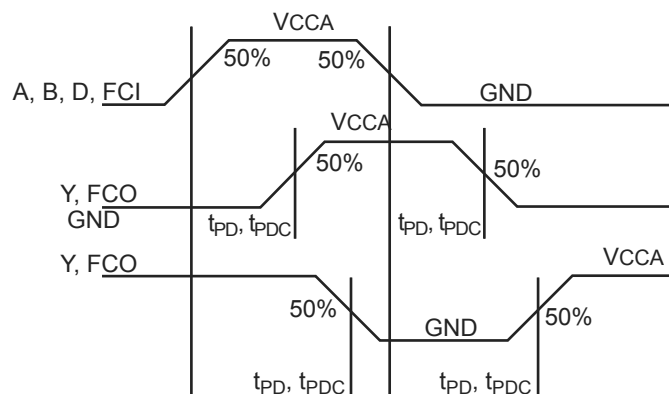


Figure 2-28 • C-Cell Timing Model and Waveforms

Timing Characteristics

Table 2-62 • C-Cell

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t _{PD}	Any input to output Y	0.74		0.84		0.99		ns
t _{PDC}	Any input to carry chain output (FCO)	0.57		0.64		0.76		ns
t _{PDB}	Any input through DB when one input is used	0.95		1.09		1.28		ns
t _{CCY}	Input to carry chain (FCI) to Y	0.61		0.69		0.82		ns
t _{CC}	Input to carry chain (FCI) to carry chain output (FCO)	0.08		0.09		0.11		ns

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-75 • AX125 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t _{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-76 • AX250 Routed Array Clock Networks

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t _{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t _{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t _{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t _{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t _{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t _{RP}	Minimum Period	1.15		1.31		1.54		ns
t _{RMAX}	Maximum Frequency		870		763		649	MHz

Note that the RAM blocks employ little-endian byte order for read and write operations.

Table 2-88 • RAM Signal Description

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus. The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to 15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

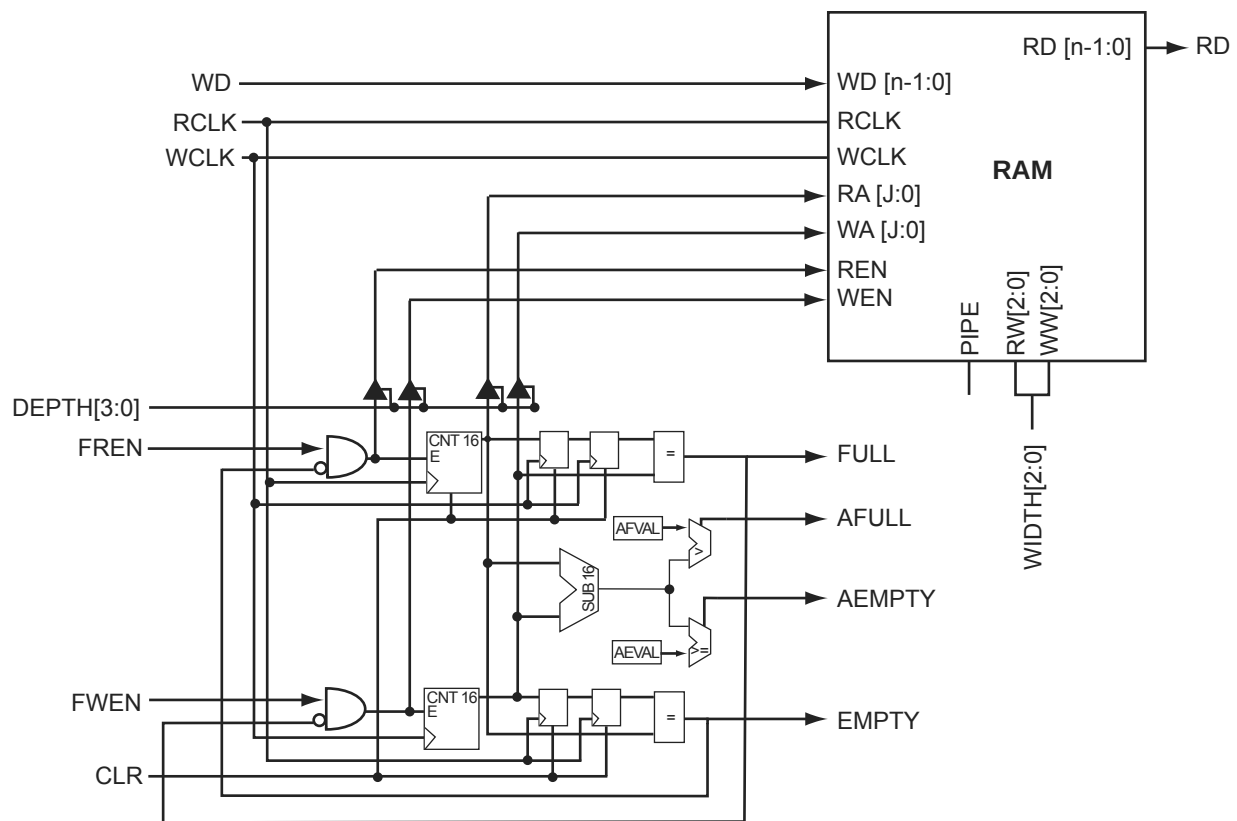
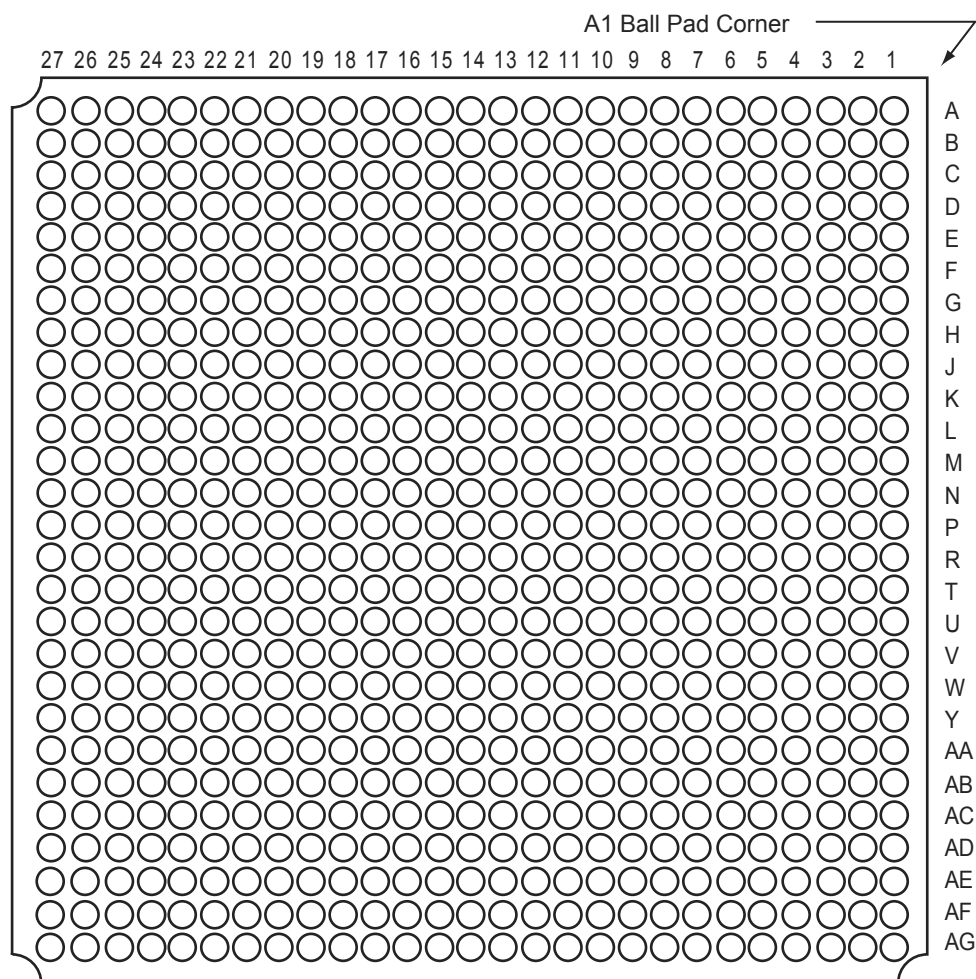


Figure 2-61 • Axcelerator RAM with Embedded FIFO Controller

3 – Package Pin Assignments

BG729



Note

For Package Manufacturing and Environmental information, visit Resource center at <http://www.microsemi.com/soc/products/rescenter/package/index.html>.

FG256-Pin FBGA		FG256-Pin FBGA		FG256-Pin FBGA	
AX125 Function	Pin Number	AX125 Function	Pin Number	AX125 Function	Pin Number
Bank 6		IO81NB7F7	C2	GND	M12
IO60NB6F6	L4	IO81PB7F7	B1	GND	M5
IO60PB6F6	M4	IO82NB7F7	D2	GND	P13
IO61NB6F6	L3	IO82PB7F7	D3	GND	P3
IO61PB6F6	M3	IO83NB7F7	E3	GND	R15
IO63NB6F6	P2	IO83PB7F7	F3	GND	R2
IO63PB6F6	N2	Dedicated I/O		GND	T1
IO64NB6F6	J4	VCCDA	E4	GND	T16
IO64PB6F6	K4	GND	A1	GND/LP	D4
IO65NB6F6	N1	GND	A16	NC	A11
IO65PB6F6	P1	GND	B15	NC	R11
IO67NB6F6	L2	GND	B2	NC	R5
IO67PB6F6	M2	GND	D15	PRA	D8
IO69NB6F6	L1	GND	E12	PRB	C8
IO69PB6F6	M1	GND	E5	PRC	N9
IO70NB6F6	J3	GND	F11	PRD	P9
IO70PB6F6	K3	GND	F6	TCK	D5
IO71NB6F6	J2	GND	G10	TDI	C6
IO71PB6F6	K2	GND	G7	TDO	C4
Bank 7		GND	G8	TMS	C3
IO72NB7F7	J1	GND	G9	TRST	C5
IO72PB7F7	K1	GND	H10	VCCA	D14
IO73NB7F7	G2	GND	H7	VCCA	F10
IO73PB7F7	H2	GND	H8	VCCA	F4
IO74NB7F7	G3	GND	H9	VCCA	F7
IO74PB7F7	H3	GND	J10	VCCA	F8
IO75NB7F7	E1	GND	J7	VCCA	F9
IO75PB7F7	F1	GND	J8	VCCA	G11
IO76NB7F7	G1	GND	J9	VCCA	G6
IO77NB7F7	E2	GND	K10	VCCA	H11
IO77PB7F7	F2	GND	K7	VCCA	H6
IO78NB7F7	G4	GND	K8	VCCA	J11
IO78PB7F7	H4	GND	K9	VCCA	J6
IO79NB7F7	C1	GND	L11	VCCA	K11
IO79PB7F7	D1	GND	L6	VCCA	K6

FG484	
AX1000 Function	Pin Number
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	AB16
VCCDA	AB8
VCCDA	C10
VCCDA	C11
VCCDA	C14
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21

FG484	
AX1000 Function	Pin Number
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13

FG484	
AX1000 Function	Pin Number
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG896	
AX2000 Function	Pin Number
IO180PB4F16	AG24
IO181NB4F17	AK24
IO181PB4F17	AK25
IO182NB4F17	AD22
IO182PB4F17	AC22
IO183NB4F17	AF22
IO183PB4F17	AF23
IO184NB4F17	AE21
IO184PB4F17	AE22
IO185NB4F17	AJ23
IO185PB4F17	AJ24
IO187NB4F17	AH22
IO187PB4F17	AH23
IO188NB4F17	AD21
IO188PB4F17	AC21
IO189PB4F17	AK22
IO190NB4F17	AF20
IO190PB4F17	AF21
IO191NB4F17	AG21
IO191PB4F17	AG22
IO192NB4F17	AE19
IO192PB4F17	AE20
IO195NB4F18	AK21
IO195PB4F18	AJ21
IO196NB4F18	AD19
IO196PB4F18	AD20
IO197NB4F18	AJ20
IO197PB4F18	AK20
IO198NB4F18	AC19
IO198PB4F18	AC20
IO199NB4F18	AG19
IO199PB4F18	AG20
IO200NB4F18	AH19
IO200PB4F18	AH20
IO201NB4F18	AK19

FG896	
AX2000 Function	Pin Number
IO201PB4F18	AJ19
IO202NB4F18	AC18
IO202PB4F18	AB18
IO206NB4F19	AE18
IO206PB4F19	AD18
IO207NB4F19	AJ17
IO207PB4F19	AJ18
IO208NB4F19	AE17
IO208PB4F19	AD17
IO209NB4F19	AK17
IO210NB4F19	AC17
IO210PB4F19	AB17
IO211NB4F19	AJ16
IO211PB4F19	AK16
IO212NB4F19/CLKEN	AG18
IO212PB4F19/CLKEP	AH18
IO213NB4F19/CLKFN	AG16
IO213PB4F19/CLKFP	AG17
Bank 5	
IO214NB5F20/CLKGN	AG14
IO214PB5F20/CLKGP	AG15
IO215NB5F20/CLKHN	AG13
IO215PB5F20/CLKHP	AH13
IO216NB5F20	AB14
IO216PB5F20	AC15
IO217NB5F20	AK15
IO217PB5F20	AJ15
IO218NB5F20	AE14
IO218PB5F20	AD14
IO219NB5F20	AK14
IO219PB5F20	AJ14
IO222NB5F20	AB13
IO222PB5F20	AC14
IO223NB5F21	AJ12
IO223PB5F21	AJ13

FG896	
AX2000 Function	Pin Number
IO225NB5F21	AH11
IO225PB5F21	AH12
IO226NB5F21	AC13
IO226PB5F21	AD13
IO227NB5F21	AE12
IO227PB5F21	AE13
IO228NB5F21	AG11
IO228PB5F21	AG12
IO229NB5F21	AK11
IO229PB5F21	AK12
IO230NB5F21	AC12
IO230PB5F21	AD12
IO232NB5F21	AE11
IO232PB5F21	AF11
IO233NB5F21	AJ10
IO233PB5F21	AJ11
IO234NB5F21	AC11
IO234PB5F21	AD11
IO236NB5F22	AK9
IO236PB5F22	AK10
IO237NB5F22	AG9
IO237PB5F22	AG10
IO238NB5F22	AF9
IO238PB5F22	AF10
IO239NB5F22	AH8
IO239PB5F22	AH9
IO240NB5F22	AC10
IO240PB5F22	AD10
IO242NB5F22	AE9
IO242PB5F22	AE10
IO243NB5F22	AJ7
IO243PB5F22	AJ8
IO244NB5F22	AK6
IO244PB5F22	AK7
IO245NB5F23	AF8

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO207PB4F19	AL20	IO224PB5F21	AP14	IO242NB5F22	AG11
IO208NB4F19	AG19	IO225NB5F21	AK13	IO242PB5F22	AG12
IO208PB4F19	AF19	IO225PB5F21	AK14	IO243NB5F22	AL9
IO209NB4F19	AN18	IO226NB5F21	AE15	IO243PB5F22	AL10
IO209PB4F19	AP18	IO226PB5F21	AF15	IO244NB5F22	AM8
IO210NB4F19	AE19	IO227NB5F21	AG14	IO244PB5F22	AM9
IO210PB4F19	AD19	IO227PB5F21	AG15	IO245NB5F23	AH10
IO211NB4F19	AL18	IO228NB5F21	AJ13	IO245PB5F23	AJ10
IO211PB4F19	AM18	IO228PB5F21	AJ14	IO246NB5F23	AF10
IO212NB4F19/CLKEN	AJ20	IO229NB5F21	AM13	IO246PB5F23	AF11
IO212PB4F19/CLKEP	AK20	IO229PB5F21	AM14	IO247NB5F23	AJ9
IO213NB4F19/CLKFN	AJ18	IO230NB5F21	AE14	IO247PB5F23	AK9
IO213PB4F19/CLKFP	AJ19	IO230PB5F21	AF14	IO248NB5F23	AN7
Bank 5		IO231NB5F21	AN12	IO248PB5F23	AP7
IO214NB5F20/CLKGN	AJ16	IO231PB5F21	AP12	IO249NB5F23	AL7
IO214PB5F20/CLKGP	AJ17	IO232NB5F21	AG13	IO249PB5F23	AL8
IO215NB5F20/CLKHN	AJ15	IO232PB5F21	AH13	IO250NB5F23	AE10
IO215PB5F20/CLKHP	AK15	IO233NB5F21	AL12	IO250PB5F23	AE11
IO216NB5F20	AD16	IO233PB5F21	AL13	IO251NB5F23	AK8
IO216PB5F20	AE17	IO234NB5F21	AE13	IO251PB5F23	AJ8
IO217NB5F20	AM17	IO234PB5F21	AF13	IO252NB5F23	AH8
IO217PB5F20	AL17	IO235NB5F22	AN11	IO252PB5F23	AH9
IO218NB5F20	AG16	IO235PB5F22	AP11	IO253NB5F23	AN6
IO218PB5F20	AF16	IO236NB5F22	AM11	IO253PB5F23	AP6
IO219NB5F20	AM16	IO236PB5F22	AM12	IO254NB5F23	AG9
IO219PB5F20	AL16	IO237NB5F22	AJ11	IO254PB5F23	AG10
IO220NB5F20	AP16	IO237PB5F22	AJ12	IO255NB5F23	AJ7
IO220PB5F20	AN16	IO238NB5F22	AH11	IO255PB5F23	AK7
IO221NB5F20	AN15	IO238PB5F22	AH12	IO256NB5F23	AL6
IO221PB5F20	AP15	IO239NB5F22	AK10	IO256PB5F23	AM6
IO222NB5F20	AD15	IO239PB5F22	AK11	Bank 6	
IO222PB5F20	AE16	IO240NB5F22	AE12	IO257NB6F24	AG6
IO223NB5F21	AL14	IO240PB5F22	AF12	IO257PB6F24	AH6
IO223PB5F21	AL15	IO241NB5F22	AN10	IO258NB6F24	AD9
IO224NB5F21	AN14	IO241PB5F22	AP10	IO258PB6F24	AE9

FG1152	
AX2000 Function	Pin Number
VCOMPLD	K18
VCOMPLE	AH19
VCOMPLF	AF18
VCOMPLG	AH16
VCOMPLH	AD17
VPUMP	J26

PQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

PQ208	
AX250 Function	Pin Number
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEN	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

PQ208	
AX250 Function	Pin Number
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

CQ256	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	248
IO01PB0F0	249
IO04NB0F0	246
IO04PB0F0	247
IO05NB0F0	242
IO05PB0F0	243
IO08NB0F0	240
IO08PB0F0	241
Bank 0	
IO37NB0F3	234
IO37PB0F3	235
IO41NB0F3/HCLKAN	232
IO41PB0F3/HCLKAP	233
IO42NB0F3/HCLKBN	228
IO42PB0F3/HCLKBP	229
Bank 1 -	
IO43NB1F4/HCLKCN	220
IO43PB1F4/HCLKCP	221
IO44NB1F4/HCLKDN	216
IO44PB1F4/HCLKDP	217
Bank 1	
IO65NB1F6	210
IO65PB1F6	211
IO69NB1F6	208
IO69PB1F6	209
IO70NB1F6	199
IO71NB1F6	204
IO71PB1F6	205
IO73NB1F6	202
IO73PB1F6	203
IO74NB1F6	197
IO74PB1F6	198
Bank 2	
IO87NB2F8	187

CQ256	
AX2000 Function	Pin Number
IO87PB2F8	188
IO89PB2F8	186
Bank 2	
IO107NB2F10	184
IO107PB2F10	185
IO110NB2F10	180
IO110PB2F10	181
IO111NB2F10	178
IO111PB2F10	179
IO112NB2F10	174
IO112PB2F10	175
IO113NB2F10	172
IO113PB2F10	173
IO114NB2F10	168
IO114PB2F10	169
IO115NB2F10	166
IO115PB2F10	167
IO117NB2F10	162
IO117PB2F10	163
Bank 3	
IO139NB3F13	158
IO139PB3F13	159
IO141NB3F13	154
IO141PB3F13	155
IO142NB3F13	152
IO142PB3F13	153
IO145NB3F13	148
IO145PB3F13	149
IO146NB3F13	146
IO146PB3F13	147
IO147NB3F13	140
IO147PB3F13	141
IO148NB3F13	142
IO148PB3F13	143
IO149NB3F13	136

CQ256	
AX2000 Function	Pin Number
IO149PB3F13	137
Bank 3	
IO165NB3F15	135
IO167NB3F15	133
IO167PB3F15	134
Bank 4	
IO181NB4F17	124
IO181PB4F17	125
IO182NB4F17	122
IO182PB4F17	123
IO183NB4F17	118
IO183PB4F17	119
IO184NB4F17	116
IO184PB4F17	117
IO190NB4F17	112
IO190PB4F17	113
IO192NB4F17	110
IO192PB4F17	111
Bank 4	
IO212NB4F19/CLKEN	104
IO212PB4F19/CLKEP	105
IO213NB4F19/CLKFN	100
IO213PB4F19/CLKFP	101
Bank 5	
IO214NB5F20/CLKGN	92
IO214PB5F20/CLKGP	93
IO215NB5F20/CLKHN	88
IO215PB5F20/CLKHP	89
Bank 5	
IO236NB5F22	82
IO236PB5F22	83
IO238NB5F22	80
IO238PB5F22	81
IO240NB5F22	76
IO240PB5F22	77

CQ352		CQ352		CQ352	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
Bank 0		IO60NB1F5	275	Bank 3	
IO02NB0F0	341	IO60PB1F5	276	IO96NB3F9	217
IO02PB0F0	342	IO61NB1F5	271	IO96PB3F9	218
IO03PB0F0	343	IO61PB1F5	272	IO97NB3F9	219
IO04NB0F0	337	IO63NB1F5	269	IO97PB3F9	220
IO04PB0F0	338	IO63PB1F5	270	IO99NB3F9	213
IO08NB0F0	331	Bank 2		IO99PB3F9	214
IO08PB0F0	332	IO64NB2F6	259	IO108NB3F10	211
IO09NB0F0	335	IO64PB2F6	260	IO108PB3F10	212
IO09PB0F0	336	IO67NB2F6	261	IO109NB3F10	207
IO24NB0F2	325	IO67PB2F6	262	IO109PB3F10	208
IO24PB0F2	326	IO68NB2F6	255	IO111NB3F10	205
IO25NB0F2	323	IO68PB2F6	256	IO111PB3F10	206
IO25PB0F2	324	IO69NB2F6	253	IO112NB3F10	199
IO30NB0F2/HCLKAN	319	IO69PB2F6	254	IO112PB3F10	200
IO30PB0F2/HCLKAP	320	IO74NB2F7	249	IO113NB3F10	201
IO31NB0F2/HCLKBN	313	IO74PB2F7	250	IO113PB3F10	202
IO31PB0F2/HCLKBP	314	IO75NB2F7	247	IO115NB3F10	195
Bank 1		IO75PB2F7	248	IO115PB3F10	196
IO32NB1F3/HCLKCN	305	IO76NB2F7	243	IO116NB3F10	193
IO32PB1F3/HCLKCP	306	IO76PB2F7	244	IO116PB3F10	194
IO33NB1F3/HCLKDN	299	IO77NB2F7	241	IO117NB3F10	189
IO33PB1F3/HCLKDP	300	IO77PB2F7	242	IO117PB3F10	190
IO38NB1F3	295	IO78NB2F7	237	IO124NB3F11	183
IO38PB1F3	296	IO78PB2F7	238	IO124PB3F11	184
IO54NB1F5	287	IO79NB2F7	235	IO125NB3F11	187
IO54PB1F5	288	IO79PB2F7	236	IO125PB3F11	188
IO55NB1F5	289	IO82NB2F7	231	IO127NB3F11	181
IO55PB1F5	290	IO82PB2F7	232	IO127PB3F11	182
IO56NB1F5	281	IO83NB2F7	229	IO128NB3F11	179
IO56PB1F5	282	IO83PB2F7	230	IO128PB3F11	180
IO57NB1F5	283	IO94NB2F8	225	Bank 4	
IO57PB1F5	284	IO94PB2F8	226	IO130NB4F12	172
IO59NB1F5	277	IO95NB2F8	223	IO130PB4F12	173
IO59PB1F5	278	IO95PB2F8	224	IO131NB4F12	170