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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	317
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-fgg484

Figure 1-8 • **AX Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-2).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (V_{PUMP}) to the device to bypass the internal charge pump (See "Low Power Mode" on page 2-106 for more information).

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common VREF (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common VCCI.

Table 2-11 • **Compatible I/O Standards for Different VREF Values**

VREF	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5V and 3.3V Outputs)
0.75 V	HSTL (Class I)

Table 2-12 • **Compatible I/O Standards for Different VCCI Values**

VCCI[1]	Compatible Standards	VREF
3.3 V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3 V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVCMOS 2.5 V, GTL+ 2.5 V, LVDS[2]	1.0
2.5 V	LVCMOS 2.5 V, SSTL 2 (Classes I and II), LVDS[2]	1.25
1.8 V	LVCMOS 1.8 V	N/A
1.5 V	LVCMOS 1.5 V, HSTL Class I	0.75

Notes:

1. *VCCI is used for both inputs and outputs*
2. *VCCI tolerance is* ±5%

Table 2-13 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank.

***Table 2-13* • Legal I/O Usage Matrix**

I/O Standard	LVTTL 3.3 V	LVCMOS 2.5 V	LVCMOS1.8 V	LVCMOS1.5 V (JESD8-11)	3.3V PCI/PCI-X	GTL + (3.3 V)	GTL + (2.5 V)	HSTL Class I (1. 5V)	SSTL2 Class I & II (2.5 V)	SSTL3 Class I & II (3.3 V)	LVDS (2.5 V)	LVPECL (3.3 V)
LVTTL 3.3 V (VREF=1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVTTL 3.3 V(VREF=1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVCMOS 2.5 V (VREF=1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVCMOS 2.5 V (VREF=1.25V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVCMOS1.8 V	–	–	✓	–	–	–	–	–	–	–	–	–
LVCMOS1.5 V (VREF = 1.75 V) (JESD8-11)	–	–	–	✓	–	–	–	✓	–	–	–	–
3.3 V PCI/PCI-X (VREF = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
3.3 V PCI/PCI-X (VREF= 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
GTL + (3.3 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
GTL + (2.5 V)	–	✓	–	–	–	–	✓	–	–	–	–	–
HSTL Class I	–	–	–	✓	–	–	–	✓	–	–	–	–
SSTL2 Class I & II	–	✓	–	–	–	–	–	–	✓	–	✓	–
SSTL3 Class I & II	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVDS (VREF = 1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVDS (VREF = 1.25 V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVPECL (VREF = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVPECL (VREF = 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓

Notes:

1. *Note that GTL+ 2.5 V is not supported across the full military temperature range.*
2. *A "✓" indicates whether standards can be used within a bank at the same time.*
   Examples:
   a) LVTTL can be used with 3.3V PCI and GTL+ (3.3V), when V_{REF} = 1.0V (GTL+ requirement).
   b) LVTTL can be used with 3.3V PCI and SSTL3 Class I and II, when V_{REF} = 1.5V (SSTL3 requirement).

Note that two I/O standards are compatible if:

- Their VCCI values are identical.
- Their VREF standards are identical (if applicable).

For example, if LVTTL 3.3 V (VREF= 1.0 V) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTL 3.3 V PCI/PCI-X, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank.

I/O Standard Electrical Specifications

***Table 2-18* • Input Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	VIN = 0, f = 1.0 MHz		10	pF
C_{INCLK}	Input Capacitance on HCLK and RCLK Pin	VIN = 0, f = 1.0 MHz		10	pF

Table 2-19* • I/O Input Rise Time and Fall Time

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTL	No Requirement	50 ns
LVCMOS 2.5V	No Requirement	50 ns
LVCMOS 1.8V	No Requirement	50 ns
LVCMOS 1.5V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

*Note: *Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, refer to the IBIS models for extraction.*

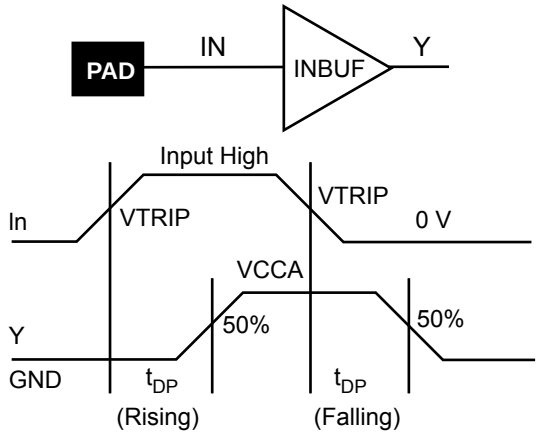


***Figure 2-9 •* Input Buffer Delays**

***Table 2-22* • 3.3 V LVTTL I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength = 2 (12 mA) / High Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		3.30		3.76		4.42	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.74		4.26		5.00	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		3.06		3.49		4.10	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.89		1.91		1.91	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.29		2.30		2.31	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

2.5 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

***Table 2-23* • DC Input and Output Levels**

VIL		VIH		VOL	VOH	IOL	IOH
Min., V	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**
-0.3	0.7	1.7	3.6	0.4	2.0	12	–12

AC Loadings

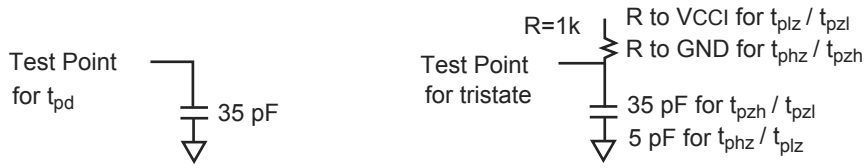


***Figure 2-16* • AC Test Loads**

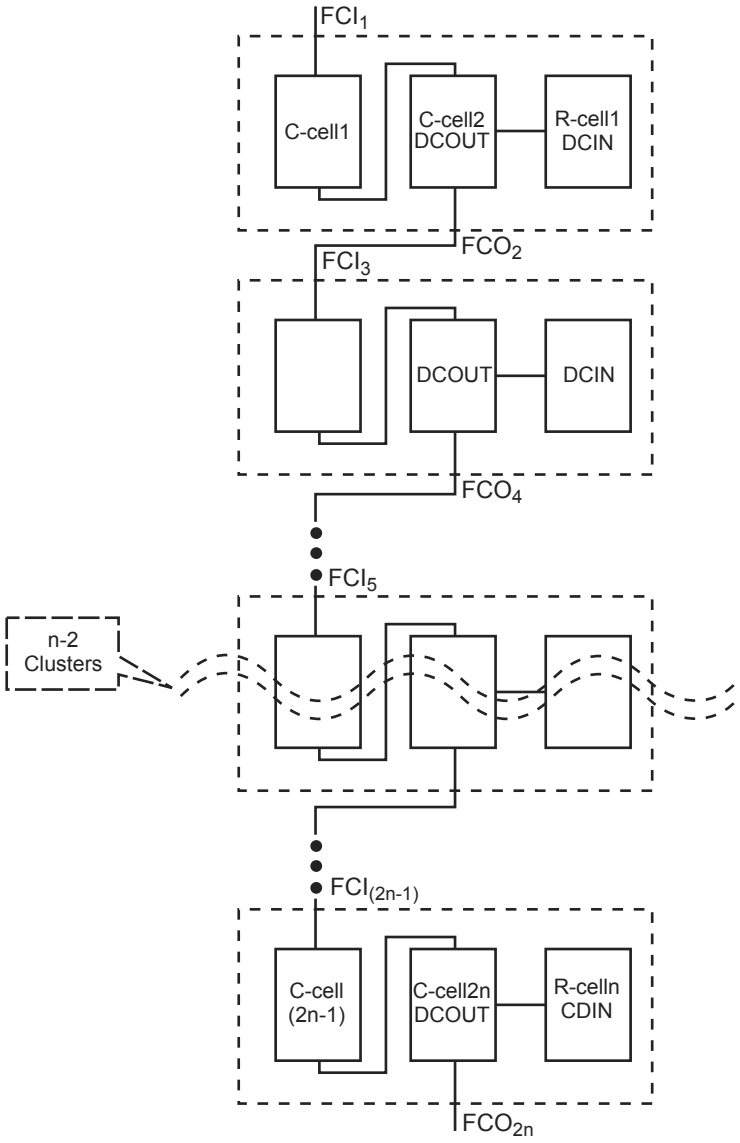
***Table 2-24* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ) (V)	C_{load} (pF)
0	2.5	1.25	N/A	35

*Note: * Measuring Point = VTRIP*

***Table 2-40* • 3.3 V GTL+ I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V GTL+I/O Module Timing								
t_{DP}	Input Buffer		1.71		1.95		2.29	ns
t_{PY}	Output Buffer		1.13		1.29		1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns



Note: The carry-chain sequence can end on either C-cell.

Figure 2-30 • **Carry-Chain Sequencing of C-Cells**

Timing Characteristics

Refer to Table 2-62 on page 2-55 for more information on carry-chain timing.

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

***Table 2-70* • AX125 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

***Table 2-71* • AX250 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t_{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-75 • **AX125 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		3.08		3.50		4.12	ns
t_{RCKH}	Input High to Low		3.13		3.56		4.19	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

Table 2-76 • **AX250 Routed Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks								
t_{RCKL}	Input Low to High		2.52		2.87		3.37	ns
t_{RCKH}	Input High to Low		2.59		2.95		3.47	ns
t_{RPWH}	Minimum Pulse Width High	0.57		0.64		0.75		ns
t_{RPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{RCKSW}	Maximum Skew		0.35		0.39		0.46	ns
t_{RP}	Minimum Period	1.15		1.31		1.54		ns
t_{RMAX}	Maximum Frequency		870		763		649	MHz

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-86). Each block has independent read and write ports which enable simultaneous read and write operations.

***Table 2-86* • Memory Block WxD Options**

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in Table 2-87.

***Table 2-87* • Allowable RW and WW Values**

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

Note that the RAM blocks employ little-endian byte order for read and write operations.

***Table 2-88* • RAM Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge)
- Read Pipelined (synchronous – two clock edges)
- Write (synchronous – one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the "Timing Characteristics" section on page 2-89.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-61):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

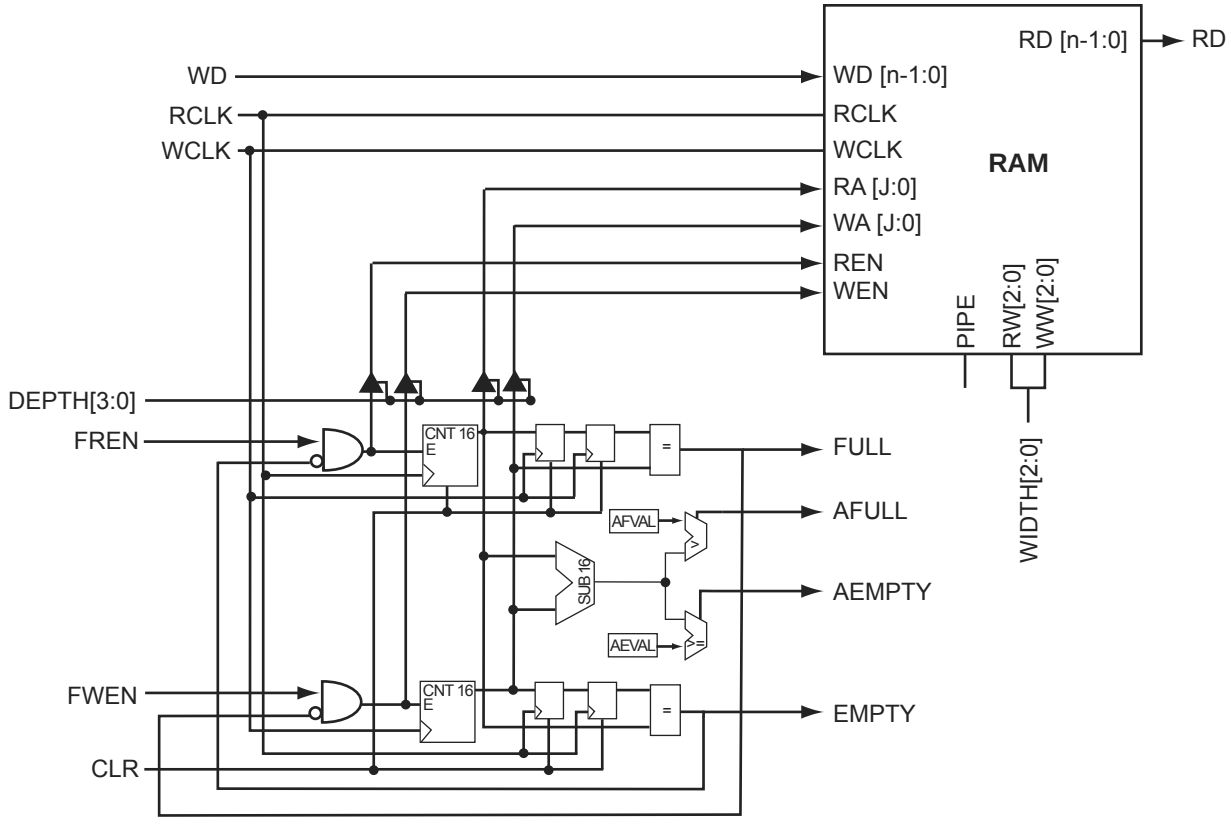
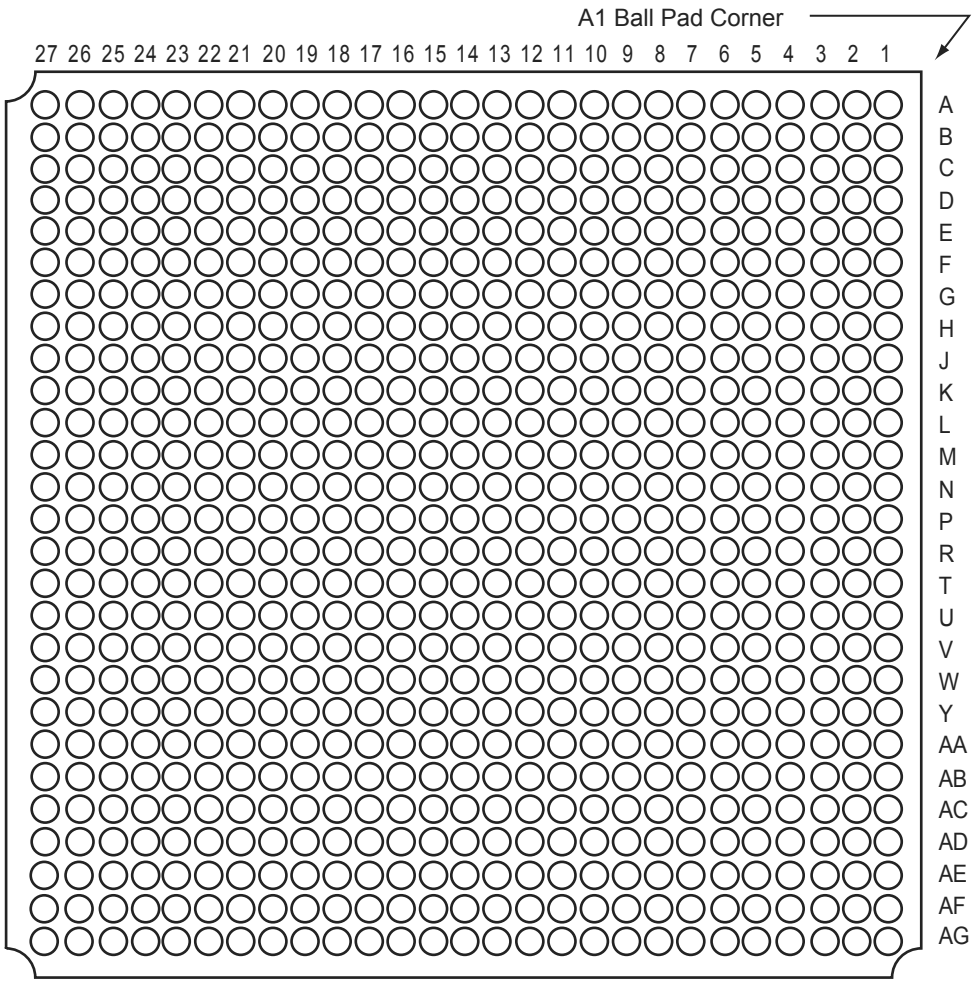


Figure 2-61 • **Axcelerator RAM with Embedded FIFO Controller**

3 – Package Pin Assignments

BG729



Note

For Package Manufacturing and Environmental information, visit Resource center at http://www.microsemi.com/soc/products/rescenter/package/index.html.

FG256	
AX250 Function	**Pin Number**
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A11
VCCDA	A2
VCCDA	C13
VCCDA	D9
VCCDA	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCDA	R11
VCCDA	R5
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10

FG256	
AX250 Function	**Pin Number**
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

FG896	
AX2000 Function	Pin Number
GND	W19
GND	Y11
GND	Y20
GND/LP	E4
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20

FG896	
AX2000 Function	Pin Number
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCDA	AD24
VCCDA	AD7
VCCDA	AE15
VCCDA	AE16
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18
VCCDA	AF19
VCCDA	AH27
VCCDA	AH4
VCCDA	C13
VCCDA	C27
VCCDA	C5
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F15
VCCDA	F16
VCCDA	F26

FG896	
AX2000 Function	Pin Number
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29

*Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

FG1152	
AX2000 Function	**Pin Number**
VCOMPLD	K18
VCOMPLE	AH19
VCOMPLF	AF18
VCOMPLG	AH16
VCOMPLH	AD17
VPUMP	J26

CQ208	
AX250 Function	Pin Number
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

CQ208	
AX250 Function	Pin Number
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193

CQ208	
AX250 Function	Pin Number
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

CQ352	
AX250 Function	**Pin Number**
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX250 Function	**Pin Number**
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

CQ352	
AX500 Function	Pin Number
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138

CQ352	
AX500 Function	Pin Number
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267