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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	317
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-fgg484m

$$P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po}$$

C_{load} = the output load (technology dependent)
 V_{CCI} = the output voltage (technology dependent)
 po = the number of outputs
 F_{po} = the average output frequency

$$P_{\text{memory}} = P_{11} * N_{\text{block}} * FR_{\text{CLK}} + P_{12} * N_{\text{block}} * FW_{\text{CLK}}$$

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
 F_{RCLK} = the read-clock frequency of the memory
 F_{WCLK} = the write-clock frequency of the memory

$$P_{\text{PLL}} = P_{13} * F_{\text{CLK}}$$

F_{RefCLK} = the clock frequency of the clock input of the PLL
 F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
 F_s = 100 MHz
 s = 1080

$$\Rightarrow P_{\text{HCLK}} = (P_1 + P_2 * s + P_3 * \text{sqrt}[s]) * F_s = 79 \text{ mW}$$

and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{R-cells}} = P_7 * ms * F_s = 173 \text{ mW}$$

mc = 1 (1 C-cell in this shift-register)
and $F_s = 100 \text{ MHz}$

$$\Rightarrow P_{\text{C-cells}} = P_8 * mc * F_s = 0.14 \text{ mW}$$

$F_{pi} \sim 0 \text{ MHz}$

and $pi = 1$ (1 reset input => this is why $F_{pi} = 0$)

$$\Rightarrow P_{\text{inputs}} = P_9 * pi * F_{pi} = 0 \text{ mW}$$

$F_{po} = 50 \text{ MHz}$

and $po = 1$

$$\Rightarrow P_{\text{outputs}} = P_{\text{I/O}} * po * F_{po} = 27.10 \text{ mW}$$

No RAM/FIFO in this shift-register

$$\Rightarrow P_{\text{memory}} = 0 \text{ mW}$$

No PLL in this shift-register

$$\Rightarrow P_{\text{PLL}} = 0 \text{ mW}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}} = 276 \text{ mW}$$

$$P_{\text{dc}} = 7.5\text{mA} * 1.5\text{V} = 11.25 \text{ mW}$$

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}} = 11.25 \text{ mW} + 276\text{mW} = 290.30 \text{ mW}$$

Timing Characteristics

Table 2-22 • 3.3 V LVTTL I/O Module

Worst-Case Commercial Conditions $V_{CCA} = 1.425\text{ V}$, $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTL Output Drive Strength = 1 (8 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		14.28		16.27		19.13	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		15.25		17.37		20.42	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		14.26		16.24		19.09	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.56		1.57		1.58	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		1.95		1.96		1.97	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-22 • 3.3 V LVTTTL I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVTTTL Output Drive Strength = 2 (12 mA) / Low Slew Rate								
t _{DP}	Input Buffer		1.68		1.92		2.26	ns
t _{PY}	Output Buffer		12.14		13.83		16.26	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		12.43		14.16		16.65	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		12.17		13.86		16.30	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.73		1.74		1.75	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.22		2.23		2.24	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.38		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-32 • 1.5V LVCMOS I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 1.4 V, TJ = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
LVCMOS15 (JESD8-11) I/O Module Timing								
t _{DP}	Input Buffer		3.59		4.09		4.81	ns
t _{PY}	Output Buffer		6.05		6.89		8.10	ns
t _{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		3.31		3.34		3.34	ns
t _{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		4.56		4.58		4.59	ns
t _{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		6.37		7.25		8.52	ns
t _{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		6.94		7.90		9.29	ns
t _{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t _{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-40 • 3.3 V GTL+ I/O Module

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3 V GTL+I/O Module Timing								
t _{DP}	Input Buffer		1.71		1.95		2.29	ns
t _{PY}	Output Buffer		1.13		1.29		1.52	ns
t _{CLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t _{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t _{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t _{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t _{HD}	Data Input Hold		0.00		0.00		0.00	ns
t _{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t _{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t _{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t _{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t _{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t _{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t _{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t _{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Timing Characteristics

Table 2-65 • AX125 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t _{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t _{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t _{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t _{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t _{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t _{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t _{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t _{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t _{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

Table 2-66 • AX250 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		-2 Speed	-1 Speed	Std Speed	Units
Parameter	Description	Typical	Typical	Typical	
Predicted Routing Delays					
t _{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t _{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t _{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t _{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t _{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t _{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t _{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t _{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t _{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t _{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t _{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t _{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

PLL Configurations

The following rules apply to the different PLL inputs and outputs:

Reference Clock

The RefCLK can be driven by (Figure 2-50):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. CLK1 output of an adjacent PLL
3. [H]CLKxP (single-ended or voltage-referenced)
4. [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Feedback Clock

The feedback clock can be driven by (Figure 2-51 on page 2-78):

1. Global routed clocks (CLKE/F/G/H) or user-created clock network
2. External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
3. An internal signal from the PLL block

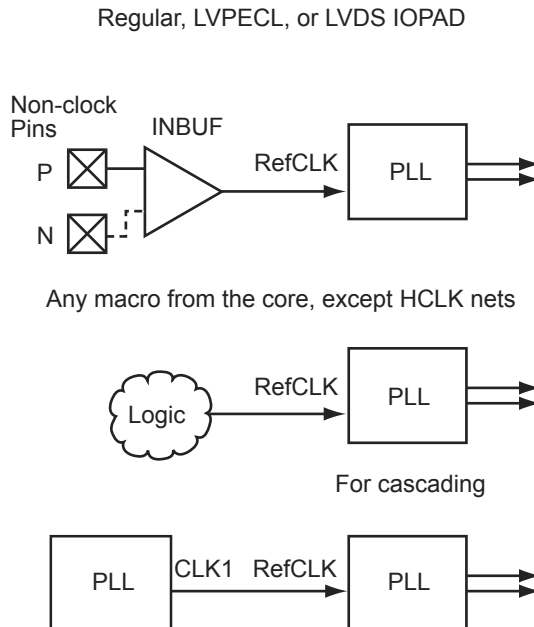


Figure 2-50 • Reference Clock Connections

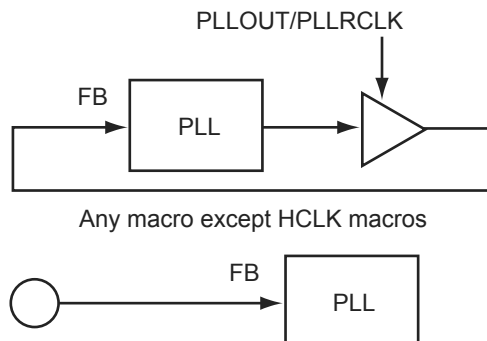


Figure 2-51 • Feedback Clock Connections



Table 2-89 • One RAM Block

Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
Write Mode								
t _{WDASU}	Write Data Setup vs. WCLK		1.08		1.23		1.45	ns
t _{WDAHD}	Write Data Hold vs. WCLK		0.22		0.25		0.30	ns
t _{WADSU}	Write Address Setup vs. WCLK		1.08		1.23		1.45	ns
t _{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t _{WENSU}	Write Enable Setup vs. WCLK		1.08		1.23		1.45	ns
t _{WENHD}	Write Enable Hold vs. WCLK		0.22		0.25		0.30	ns
t _{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t _{WCLK}	WCLK Minimum Low Pulse Width	0.88		0.88		0.88		ns
t _{WCKP}	WCLK Minimum Period	1.63		1.63		1.63		ns
Read Mode								
t _{RADSU}	Read Address Setup vs. RCLK		0.81		0.92		1.08	ns
t _{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RENSU}	Read Enable Setup vs. RCLK		0.81		0.92		1.08	ns
t _{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
t _{RCK2RD1}	RCLK-to-OUT (Pipelined)		1.32		1.51		1.77	ns
t _{RCK2RD2}	RCLK-to-OUT (Non-Pipelined)		2.16		2.46		2.90	ns
t _{RCLKH}	RCLK Minimum High Pulse Width	0.77		0.77		0.77		ns
t _{RCLKL}	RCLK Minimum Low Pulse Width	0.93		0.93		0.93		ns
t _{RCKP}	RCLK Minimum Period	1.70		1.70		1.70		ns

Note: Timing data for this single block RAM has a depth of 4,096. For all other combinations, use Microsemi's timing software.

Figure 2-63 illustrates flag generation.

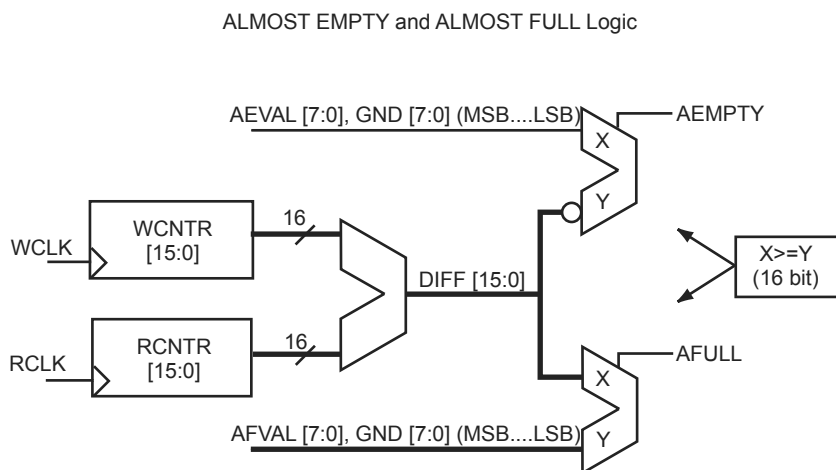


Figure 2-63 • ALMOST-EMPTY and ALMOST-FULL Logic

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >= {AFVAL[7:0], 8'b00000000})?1:0;
assign AE = ({AEVAL[7:0], 8'b00000000} >= DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-95).

Table 2-95 • Number of Available Configuration Bits

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-100.

Timing Characteristics

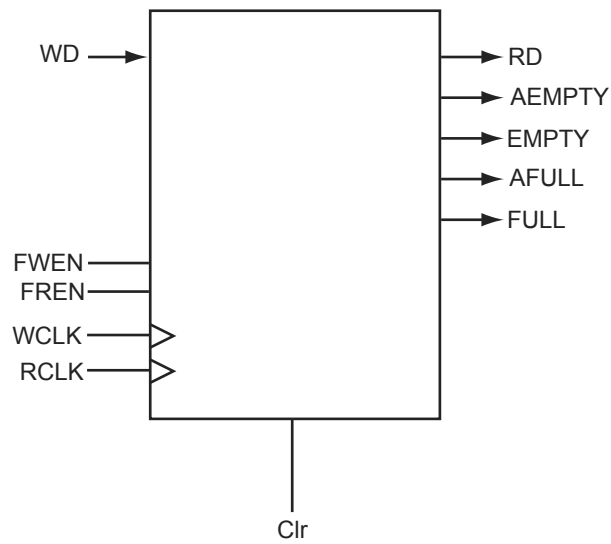


Figure 2-66 • FIFO Model

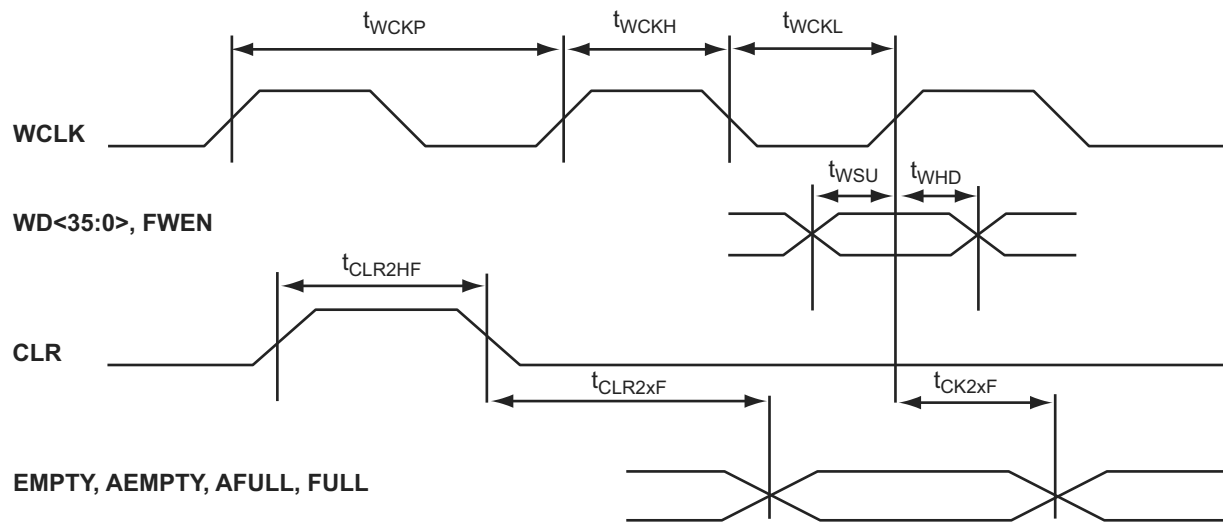


Figure 2-67 • FIFO Write Timing

Table 2-99 • Two FIFO Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
FIFO Module Timing								
t _{WSU}	Write Setup		13.75		15.66		18.41	ns
t _{WHD}	Write Hold		0.00		0.00		0.00	ns
t _{WCKH}	WCLK High		0.75		0.75		0.75	ns
t _{WCKL}	WCLK Low		1.76		1.76		1.76	ns
t _{WCKP}	Minimum WCLK Period	2.51		2.51		2.51		ns
t _{RSU}	Read Setup		14.33		16.32		19.19	ns
t _{RHD}	Read Hold		0.00		0.00		0.00	ns
t _{RCKH}	RCLK High		0.73		0.73		0.73	ns
t _{RCKL}	RCLK Low		1.89		1.89		1.89	ns
t _{RCKP}	Minimum RCLK period	2.62		2.62		2.62		ns
t _{CLRHF}	Clear High		0.00		0.00		0.00	ns
t _{CLR2FF}	Clear-to-flag (EMPTY/FULL)		1.92		2.18		2.57	ns
t _{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)		4.39		5.00		5.88	ns
t _{CK2FF}	Clock-to-flag (EMPTY/FULL)		2.13		2.42		2.85	ns
t _{CK2AF}	Clock-to-flag (AEMPTY/AFULL)		5.04		5.75		6.75	ns
t _{RCK2RD1}	RCLK-To-OUT (Pipelined)		1.43		1.63		1.92	ns
t _{RCK2RD2}	RCLK-To-OUT (Nonpipelined)		2.26		2.58		3.03	ns

Note: Timing data for these two cascaded FIFO blocks uses a depth of 8,192. For all other combinations, use Microsemi's timing software.

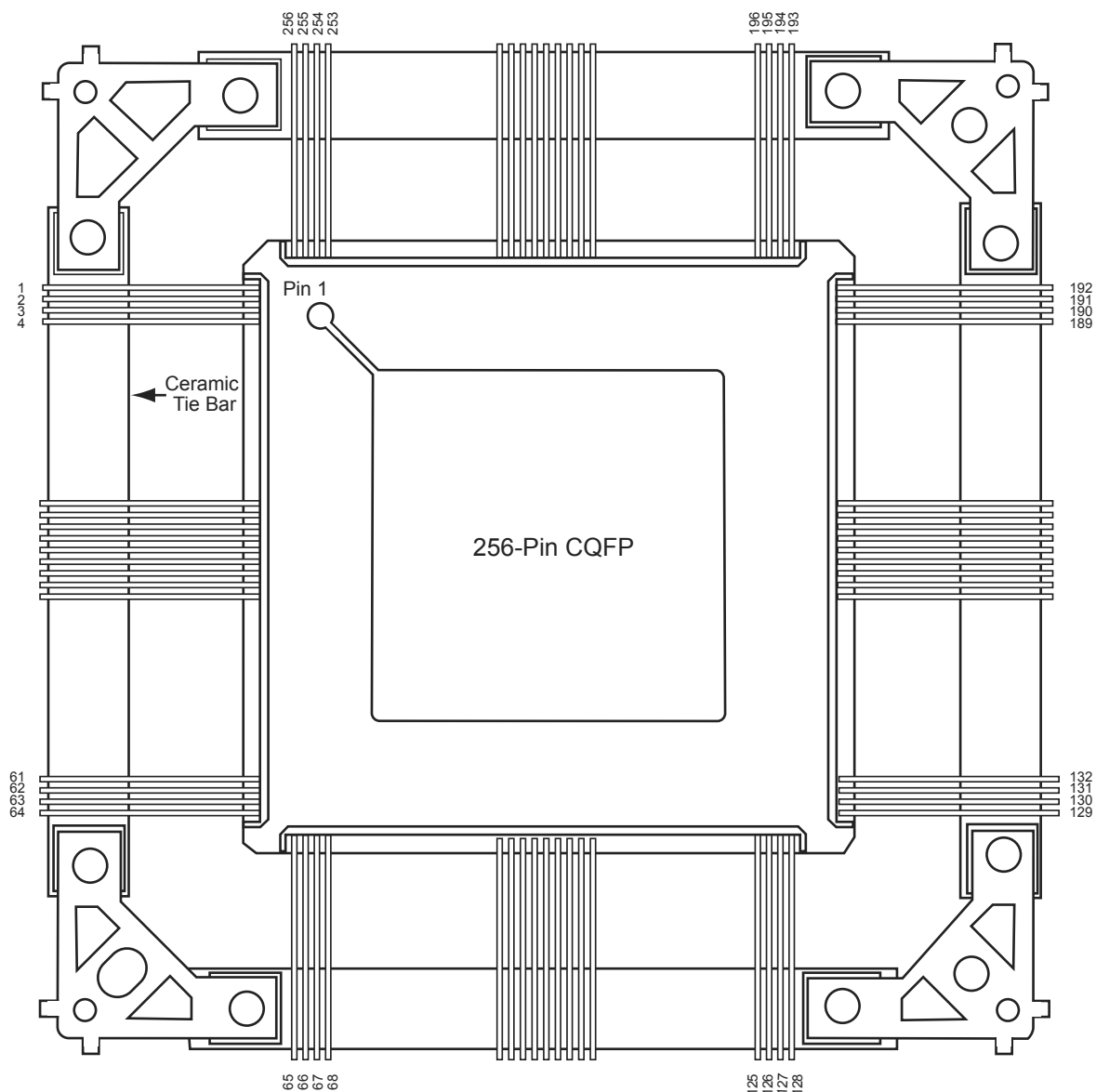
FG676		FG676		FG676	
AX500 Function	Pin Number	AX500 Function	Pin Number	AX500 Function	Pin Number
IO153PB7F14	M6	GND	A8	GND	L11
IO154NB7F14	K2	GND	AC23	GND	L12
IO154PB7F14	L2	GND	AC4	GND	L13
IO155NB7F14	K3	GND	AD24	GND	L14
IO155PB7F14	L3	GND	AD3	GND	L15
IO156NB7F14	L5	GND	AE2	GND	L16
IO156PB7F14	L4	GND	AE25	GND	L17
IO157NB7F14	L6	GND	AF1	GND	M10
IO157PB7F14	L7	GND	AF13	GND	M11
IO158NB7F15	J1	GND	AF14	GND	M12
IO158PB7F15	K1	GND	AF19	GND	M13
IO159NB7F15	J4	GND	AF26	GND	M14
IO159PB7F15	K4	GND	AF8	GND	M15
IO160NB7F15	H2	GND	B2	GND	M16
IO160PB7F15	J2	GND	B25	GND	M17
IO161NB7F15	K6	GND	B26	GND	N1
IO161PB7F15	K5	GND	C24	GND	N10
IO162NB7F15	H3	GND	C3	GND	N11
IO162PB7F15	J3	GND	G20	GND	N12
IO163NB7F15	G2	GND	G7	GND	N13
IO163PB7F15	G1	GND	H1	GND	N14
IO164NB7F15	G4	GND	H19	GND	N15
IO164PB7F15	H4	GND	H26	GND	N16
IO165NB7F15	F3	GND	H8	GND	N17
IO165PB7F15	G3	GND	J18	GND	N26
IO166NB7F15	E2	GND	J9	GND	P1
IO166PB7F15	F2	GND	K10	GND	P10
IO167NB7F15	F5	GND	K11	GND	P11
IO167PB7F15	G5	GND	K12	GND	P12
Dedicated I/O		GND	K13	GND	P13
GND	A1	GND	K14	GND	P14
GND	A13	GND	K15	GND	P15
GND	A14	GND	K16	GND	P16
GND	A19	GND	K17	GND	P17
GND	A26	GND	L10	GND	P26

FG896	
AX2000 Function	Pin Number
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10

FG896	
AX2000 Function	Pin Number
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

FG1152		FG1152		FG1152	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO51PB1F4	J20	IO69NB1F6	C27	IO86NB2F8	J28
IO52NB1F4	B20	IO69PB1F6	C26	IO86PB2F8	J27
IO52PB1F4	A20	IO70NB1F6	H24	IO87NB2F8	M25
IO53NB1F4	F20	IO70PB1F6	G24	IO87PB2F8	L25
IO53PB1F4	E20	IO71NB1F6	H23	IO88NB2F8	L26
IO54NB1F5	B21	IO71PB1F6	G23	IO88PB2F8	K26
IO54PB1F5	A21	IO72NB1F6	B28	IO89NB2F8	G31
IO55NB1F5	K21	IO72PB1F6	A28	IO89PB2F8	F31
IO55PB1F5	J21	IO73NB1F6	E26	IO90NB2F8	H29
IO56NB1F5	D21	IO73PB1F6	E25	IO90PB2F8	G29
IO56PB1F5	C21	IO74NB1F6	F26	IO91NB2F8	K28
IO57NB1F5	G22	IO74PB1F6	F25	IO91PB2F8	K27
IO57PB1F5	G21	IO75NB1F6	K25	IO92NB2F8	J30
IO58NB1F5	E22	IO75PB1F6	K24	IO92PB2F8	H30
IO58PB1F5	E21	IO76NB1F7	D27	IO93NB2F8	L28
IO59NB1F5	D22	IO76PB1F7	D26	IO93PB2F8	L27
IO59PB1F5	C22	IO77NB1F7	B29	IO94NB2F8	K29
IO60NB1F5	B23	IO77PB1F7	A29	IO94PB2F8	J29
IO60PB1F5	A23	IO78NB1F7	D28	IO95NB2F8	K31
IO61NB1F5	H22	IO78PB1F7	C28	IO95PB2F8	J31
IO61PB1F5	H21	IO79NB1F7	H25	IO96NB2F9	J32
IO62NB1F5	C24	IO79PB1F7	G25	IO96PB2F9	H32
IO62PB1F5	C23	IO80NB1F7	F27	IO97NB2F9	M27
IO63NB1F5	F23	IO80PB1F7	E27	IO97PB2F9	M26
IO63PB1F5	F22	IO81NB1F7	J25	IO98NB2F9	L30
IO64NB1F6	B24	IO81PB1F7	J24	IO98PB2F9	K30
IO64PB1F6	A24	IO82NB1F7	D29	IO99NB2F9	N25
IO65NB1F6	J22	IO82PB1F7	C29	IO99PB2F9	N26
IO65PB1F6	K22	IO83NB1F7	H26	IO100NB2F9	M29
IO66NB1F6	B25	IO83PB1F7	G26	IO100PB2F9	L29
IO66PB1F6	A25	IO84NB1F7	F28	IO101NB2F9	L33
IO67NB1F6	K23	IO84PB1F7	E28	IO101PB2F9	L32
IO67PB1F6	J23	IO85NB1F7	H27	IO102NB2F9	K34
IO68NB1F6	F24	IO85PB1F7	G27	IO102PB2F9	K33
IO68PB1F6	E24	Bank 2		IO103NB2F9	N28

CQ256



Note

For Package Manufacturing and Environmental information, visit the Resource center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

CQ256		CQ256		CQ256	
AX2000 Function	Pin Number	AX2000 Function	Pin Number	AX2000 Function	Pin Number
IO242NB5F22	74	IO315PB7F29	21	GND	121
IO242PB5F22	75	IO316NB7F29	18	GND	128
IO243NB5F22	70	IO316PB7F29	19	GND	129
IO243PB5F22	71	IO317NB7F29	14	GND	132
IO244NB5F22	68	IO317PB7F29	15	GND	139
IO244PB5F22	69	IO318NB7F29	12	GND	145
Bank 6		IO318PB7F29	13	GND	151
IO257PB6F24	60	IO320NB7F29	8	GND	157
IO258NB6F24	58	IO320PB7F29	9	GND	161
IO258PB6F24	59	Bank 7		GND	165
Bank 6		IO341NB7F31	6	GND	171
IO279NB6F26	56	IO341PB7F31	7	GND	177
IO279PB6F26	57	Dedicated I/O		GND	183
IO280NB6F26	52	GND	1	GND	190
IO280PB6F26	53	GND	5	GND	192
IO281NB6F26	50	GND	11	GND	193
IO281PB6F26	51	GND	17	GND	201
IO282NB6F26	46	GND	23	GND	207
IO282PB6F26	47	GND	29	GND	213
IO284NB6F26	44	GND	33	GND	219
IO284PB6F26	45	GND	37	GND	225
IO285NB6F26	40	GND	43	GND	231
IO285PB6F26	41	GND	49	GND	239
IO286NB6F26	38	GND	55	GND	245
IO286PB6F26	39	GND	62	GND	256
IO287NB6F26	34	GND	64	PRA	227
IO287PB6F26	35	GND	65	PRB	226
Bank 7 9		GND	73	PRC	99
IO310NB7F29	30	GND	79	PRD	98
IO310PB7F29	31	GND	85	TCK	253
IO311NB7F29	26	GND	91	TDI	252
IO311PB7F29	27	GND	97	TDO	250
IO312NB7F29	24	GND	103	TMS	254
IO312PB7F29	25	GND	109	TRST	255
IO315NB7F29	20	GND	115	VCCA	3

CG624		CG624		CG624	
AX1000 Function	Pin Number	AX1000 Function	Pin Number	AX1000 Function	Pin Number
GND	A8	GND/LP	E8	GND	V1
GND	AA10	GND	H1	GND	V25
GND	AA16	GND	H21	GND	V5
GND	AA18	GND	H25	NC	A14
GND	AA21	GND	K21	NC	AA20
GND	AA5	GND	K23	NC	AB13
GND	AB22	GND	K3	NC	AD4
GND	AB4	GND	L11	NC	AE12
GND	AC10	GND	L12	NC	F21
GND	AC16	GND	L13	NC	G10
GND	AC23	GND	L14	PRA	F13
GND	AC3	GND	L15	PRB	A13
GND	AD1	GND	M11	PRC	AB12
GND	AD2	GND	M12	PRD	AE13
GND	AD24	GND	M13	TCK	F5
GND	AD25	GND	M14	TDI	C5
GND	AE1	GND	M15	TDO	F6
GND	AE18	GND	N11	TMS	D6
GND	AE2	GND	N12	TRST	E6
GND	AE24	GND	N13	VCCA	AB20
GND	AE25	GND	N14	VCCA	F22
GND	AE8	GND	N15	VCCA	F4
GND	B1	GND	P11	VCCA	J17
GND	B2	GND	P12	VCCA	J9
GND	B24	GND	P13	VCCA	K10
GND	B25	GND	P14	VCCA	K11
GND	C10	GND	P15	VCCA	K15
GND	C16	GND	R11	VCCA	K16
GND	C23	GND	R12	VCCA	L10
GND	C3	GND	R13	VCCA	L16
GND	D22	GND	R14	VCCA	R10
GND	D4	GND	R15	VCCA	R16
GND	E10	GND	T21	VCCA	T10
GND	E16	GND	T23	VCCA	T11
GND	E21	GND	T3	VCCA	T15
GND	E5	GND	T5	VCCA	T16

CG624	
AX2000 Function	Pin Number
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20*
IO85PB1F7	D19*
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17*
IO89PB2F8	G22*
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23*
IO107PB2F10	N16*
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9

Note: **Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*

CG624	
AX2000 Function	Pin Number
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

Note: **Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.*