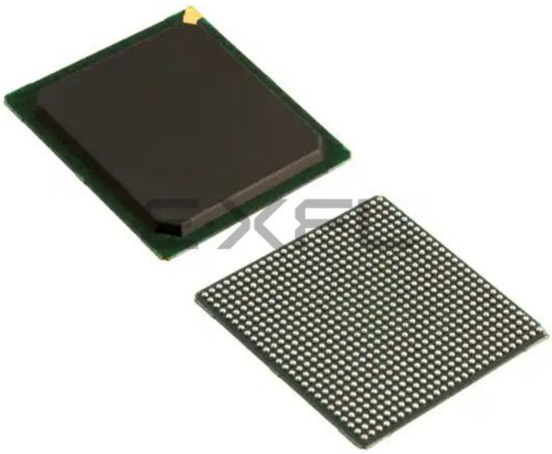


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8064
Number of Logic Elements/Cells	-
Total RAM Bits	73728
Number of I/O	336
Number of Gates	500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ax500-fgg676i

Axcelerator Family Device Status

Axcelerator® Devices	Status
AX125	Production
AX250	Production
AX500	Production
AX1000	Production
AX2000	Production

Temperature Grade Offerings

Package	AX125	AX250	AX500	AX1000	AX2000
PQ208	–	C, I, M	C, I, M	–	–
CQ208	–	M	M	–	–
CQ256	–	–	–	–	M
FG256	C, I	C, I, M	–	–	–
FG324	C, I	–	–	–	–
CQ352	–	M	M	M	M
FG484	–	C, I, M	C, I, M	C, I, M	–
CG624	–	–	–	M	M
FG676	–	–	C, I, M	C, I, M	–
BG729	–	–	–	C, I, M	–
FG896	–	–	–	C, I, M	C, I, M
FG1152	–	–	–	–	C, I, M

C = Commercial
I = Industrial
M = Military

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std	–1	–2
C	✓	✓	✓
I	✓	✓	✓
M	✓	✓	–

C = Commercial
I = Industrial
M = Military

Two C-cells, a single R-cell, two Transmit (TX), and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

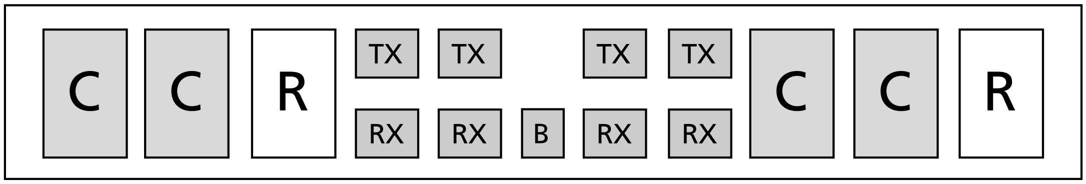


Figure 1-4 • **AX SuperCluster**

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

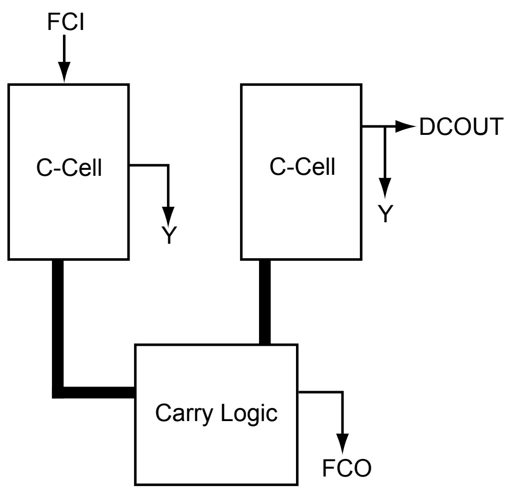


Figure 1-5 • **AX 2-Bit Carry Logic**

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the AX1000 is composed of a 3x3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1). Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the AX250).

Table 1-1 **• Number of Core Tiles per Device**

Device	Number of Core Tiles
AX125	1 regular tile
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

Poutputs = PI/O * po * Fpo

C_{load} = the output load (technology dependent)
VCCI = the output voltage (technology dependent)
po = the number of outputs
F_{po} = the average output frequency

Pmemory = P11 * Nblock * FRCLK + P12 * Nblock * FWCLK

N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
F_{RCLK} = the read-clock frequency of the memory
F_{WCLK} = the write-clock frequency of the memory

PPLL = P13 * FCLK

F_{RefCLK} = the clock frequency of the clock input of the PLL
F_{CLK} = the clock frequency of the first clock output of the PLL

Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

ms = 1,080 (in a shift register - 100% of R-cells are toggling at each clock cycle)
Fs = 100 MHz
s = 1080
=> P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs = 79 mW
and Fs = 100 MHz
=> $P_{R\text{-}cells}$ = P7 * ms * Fs = 173 mW
mc = 1 (1 C-cell in this shift-register)
and Fs = 100 MHz
=> $P_{C\text{-}cells}$ = P8 * mc * Fs = 0.14 mW
F_{pi} ~ 0 MHz
and pi= 1 (1 reset input => this is why F_{pi}=0)
=> P_{inputs} = P9 * pi * F_{pi} = 0 mW
F_{po} = 50 MHz
and po = 1
=> $P_{outputs}$ = $P_{I/O}$ * po * F_{po}= 27.10 mW
No RAM/FIFO in this shift-register
=> P_{memory} = 0 mW
No PLL in this shift-register
=> P_{PLL} = 0 mW
$P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$ = 276 mW
P_{dc} = 7.5mA * 1.5V = 11.25 mW
$P_{total} = P_{dc} + P_{ac}$ = 11.25 mW + 276mW = 290.30 mW

Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 kΩ). These are weak transistors with the gates tied on, so the on resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors; they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8 mA, 12 mA, 16 mA, or 24 mA – that can be specified in Designer.[5]

***Table 2-14* • Bank-Wide Delay Values**

Bits Setting	Delay (ns)	Bits Setting	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

5. *These values are minimum drive strengths.*

Table 2-22 • 3.3 V LVTTL I/O Module
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C (continued)

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
LVTTL Output Drive Strength =3 (16 mA) / Low Slew Rate								
t_{DP}	Input Buffer		1.68		1.92		2.26	ns
t_{PY}	Output Buffer		11.03		12.56		14.77	ns
t_{ENZL}	Enable to Pad Delay through the Output Buffer—Z to Low		11.42		13.01		15.29	ns
t_{ENZH}	Enable to Pad Delay through the Output Buffer—Z to High		11.04		12.58		14.79	ns
t_{ENLZ}	Enable to Pad Delay through the Output Buffer—Low to Z		1.86		1.88		1.88	ns
t_{ENHZ}	Enable to Pad Delay through the Output Buffer—High to Z		2.50		2.51		2.52	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O Input Register		0.67		0.77		0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O Output Register and the I/O Enable Register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-40 **• 3.3 V GTL+ I/O Module**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3 V GTL+I/O Module Timing								
t_{DP}	Input Buffer		1.71		1.95		2.29	ns
t_{PY}	Output Buffer		1.13		1.29		1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.67		0.77		0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register		0.67		0.77		0.90	ns
t_{SUD}	Data Input Set-Up		0.23		0.27		0.31	ns
t_{SUE}	Enable Input Set-Up		0.26		0.30		0.35	ns
t_{HD}	Data Input Hold		0.00		0.00		0.00	ns
t_{HE}	Enable Input Hold		0.00		0.00		0.00	ns
t_{CPWHL}	Clock Pulse Width High to Low	0.39		0.39		0.39		ns
t_{CPWLH}	Clock Pulse Width Low to High	0.39		0.39		0.39		ns
t_{WASYN}	Asynchronous Pulse Width	0.37		0.37		0.37		ns
t_{REASYN}	Asynchronous Recovery Time		0.13		0.15		0.17	ns
t_{HASYN}	Asynchronous Removal Time		0.00		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.23		0.27		0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.23		0.27		0.31	ns

Table 2-69 • AX2000 Predicted Routing Delays
Worst-Case Commercial Conditions VCCA = 1.425 V, T_J = 70°C

		–2 Speed	–1 Speed	Std Speed	
Parameter	**Description**	**Typical**	**Typical**	**Typical**	**Units**
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.50	0.56	0.66	ns
t_{RD2}	Routing delay for FO2	0.59	0.67	0.79	ns
t_{RD3}	Routing delay for FO3	0.70	0.80	0.94	ns
t_{RD4}	Routing delay for FO4	0.76	0.87	1.02	ns
t_{RD5}	Routing delay for FO5	0.98	1.11	1.31	ns
t_{RD6}	Routing delay for FO6	1.48	1.68	1.97	ns
t_{RD7}	Routing delay for FO7	1.65	1.87	2.20	ns
t_{RD8}	Routing delay for FO8	1.73	1.96	2.31	ns
t_{RD16}	Routing delay for FO16	2.58	2.92	3.44	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-70 **• AX125 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		3.02		3.44		4.05	ns
t_{HCKH}	Input High to Low		3.03		3.46		4.06	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

Table 2-71 **• AX250 Dedicated (Hardwired) Array Clock Networks**
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

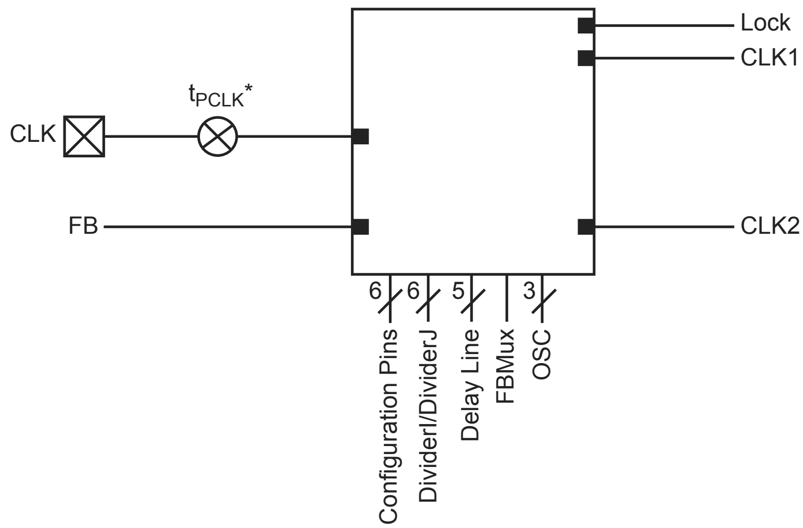
		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input Low to High		2.57		2.93		3.45	ns
t_{HCKH}	Input High to Low		2.61		2.97		3.50	ns
t_{HPWH}	Minimum Pulse Width High	0.58		0.65		0.77		ns
t_{HPWL}	Minimum Pulse Width Low	0.52		0.59		0.69		ns
t_{HCKSW}	Maximum Skew		0.06		0.07		0.08	ns
t_{HP}	Minimum Period	1.15		1.31		1.54		ns
t_{HMAX}	Maximum Frequency		870		763		649	MHz

User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL is to create custom PLL blocks using Microsemi's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

Timing Model



Note: t_{PCLK} is the delay in the clock signal

***Figure 2-52* • PLL Model**

Table 2-91 • Four RAM Blocks Cascaded
Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

		–2 Speed		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Write Mode								
t_{WDASU}	Write Data Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WDAHD}	Write Data Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WADSU}	Write Address Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WADHD}	Write Address Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WENSU}	Write Enable Setup vs. WCLK		2.37		2.70		3.17	ns
t_{WENHD}	Write Enable Hold vs. WCLK		0.00		0.00		0.00	ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		0.75		ns
t_{WCLK}	WCLK Minimum Low Pulse Width	2.51		2.51		2.51		ns
t_{WCKP}	WCLK Minimum Period	3.26		3.26		3.26		ns
Read Mode								
t_{RADSU}	Read Address Setup vs. RCLK		3.08		3.51		4.13	ns
t_{RADHD}	Read Address Hold vs. RCLK		0.00		0.00		0.00	ns
t_{RENSU}	Read Enable Setup vs. RCLK		3.08		3.51		4.13	ns
t_{RENHD}	Read Enable Hold vs. RCLK		0.00		0.00		0.00	ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		2.36		2.69		3.16	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		2.83		3.23		3.79	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	2.96		2.96		2.96		ns
t_{RCKP}	RCLK Minimum Period	3.69		3.69		3.69		ns

Note: Timing data for these four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Microsemi's timing software.

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 2-64). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 2-64).

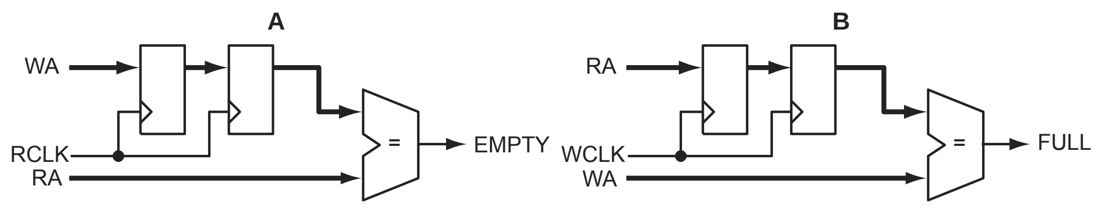


Figure 2-64 **• Overflow and Underflow Control**

FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 2-96.

Table 2-96 **• FIFO Width Configurations**

WIDTH(2:0)	W x D
000	1 x 4k
001	2 x 2k
010	4 x 1k
011	9 x 512
100	18 x 256
101	36 x 128
11x	reserved

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-86 on page 2-87 describes the FIFO depth options for various data width and memory blocks.

Interface

Figure 2-65 on page 2-99 shows a logic block diagram of the Axcelerator FIFO module.

Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using SmartGen, the user only needs to specify the depth and width of the necessary FIFO blocks. SmartGen automatically configures these blocks to optimize performance.

FG256-Pin FBGA	
AX125 Function	Pin Number
Bank 6	
IO60NB6F6	L4
IO60PB6F6	M4
IO61NB6F6	L3
IO61PB6F6	M3
IO63NB6F6	P2
IO63PB6F6	N2
IO64NB6F6	J4
IO64PB6F6	K4
IO65NB6F6	N1
IO65PB6F6	P1
IO67NB6F6	L2
IO67PB6F6	M2
IO69NB6F6	L1
IO69PB6F6	M1
IO70NB6F6	J3
IO70PB6F6	K3
IO71NB6F6	J2
IO71PB6F6	K2
Bank 7	
IO72NB7F7	J1
IO72PB7F7	K1
IO73NB7F7	G2
IO73PB7F7	H2
IO74NB7F7	G3
IO74PB7F7	H3
IO75NB7F7	E1
IO75PB7F7	F1
IO76NB7F7	G1
IO77NB7F7	E2
IO77PB7F7	F2
IO78NB7F7	G4
IO78PB7F7	H4
IO79NB7F7	C1
IO79PB7F7	D1

FG256-Pin FBGA	
AX125 Function	Pin Number
IO81NB7F7	C2
IO81PB7F7	B1
IO82NB7F7	D2
IO82PB7F7	D3
IO83NB7F7	E3
IO83PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6

FG256-Pin FBGA	
AX125 Function	Pin Number
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
NC	A11
NC	R11
NC	R5
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6

FG324	
AX125 Function	**Pin Number**
IO50NB4F4/CLKFN	U9
IO50PB4F4/CLKFP	U10
Bank 5	
IO51NB5F5/CLKGN	R8
IO51PB5F5/CLKGP	R9
IO52NB5F5/CLKHN	T7
IO52PB5F5/CLKHP	T8
IO53NB5F5	U6
IO53PB5F5	U7
IO54NB5F5	V8
IO54PB5F5	V9
IO55NB5F5	V6
IO55PB5F5	V7
IO56NB5F5	U4
IO56PB5F5	U5
IO57NB5F5	T4
IO57PB5F5	T5
IO58NB5F5	V4
IO58PB5F5	V5
IO59NB5F5	V2
IO59PB5F5	V3
Bank 6	
IO60NB6F6	P5
IO60PB6F6	P6
IO61NB6F6	T2
IO61PB6F6	U3
IO62NB6F6	T1
IO62PB6F6	U1
IO63NB6F6	P1
IO63PB6F6	R1
IO64NB6F6	R3
IO64PB6F6	P3
IO65NB6F6	P2
IO65PB6F6	R2
IO66NB6F6	M3
IO66PB6F6	N3
IO67NB6F6	M2
IO67PB6F6	N2
IO68NB6F6	M1
IO68PB6F6	N1
IO69NB6F6	K4
IO69PB6F6	L4
IO70NB6F6	K1
IO70PB6F6	L1
IO71NB6F6	K3
IO71PB6F6	L3
Bank 7	
IO72NB7F7	H4
IO72PB7F7	J4
IO73NB7F7	K2
IO73PB7F7	L2
IO74NB7F7	H2
IO74PB7F7	H1
IO75NB7F7	H3
IO75PB7F7	J3
IO76NB7F7	F2
IO76PB7F7	G2
IO77NB7F7	F1
IO77PB7F7	G1
IO78NB7F7	D2
IO78PB7F7	E2
IO79NB7F7	F3
IO79PB7F7	G3
IO80NB7F7	E3
IO80PB7F7	E4
IO81NB7F7	D1
IO81PB7F7	E1
IO82NB7F7	D3
IO82PB7F7	C2
IO83NB7F7	B1
IO83PB7F7	C1
Dedicated I/O	
VCCDA	F5
GND	A1
GND	A18
GND	B17
GND	B2
GND	C16
GND	C3
GND	E16
GND	F13
GND	F6
GND	G12
GND	G7
GND	H10
GND	H11
GND	H8
GND	H9
GND	J10
GND	J11
GND	J8
GND	J9
GND	K10
GND	K11
GND	K8
GND	K9
GND	L10
GND	L11
GND	L8
GND	L9
GND	M12
GND	M7
GND	N13
GND	N6
GND	R14

FG324	
AX125 Function	Pin Number
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

FG484	
AX250 Function	Pin Number
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13

FG484	
AX250 Function	Pin Number
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

FG484	
AX1000 Function	Pin Number
Bank 0	
IO01NB0F0	E3
IO01PB0F0	D3
IO02NB0F0	E7
IO02PB0F0	E6
IO05NB0F0	D2
IO05PB0F0	E2
IO06NB0F0	C5
IO06PB0F0	C4
IO12NB0F1	D7
IO12PB0F1	D6
IO13NB0F1	B5
IO13PB0F1	B4
IO14NB0F1	E9
IO14PB0F1	E8
IO15NB0F1	C7
IO15PB0F1	C6
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	B7
IO17PB0F1	B6
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	C9
IO19PB0F1	C8
IO20NB0F1	D9
IO20PB0F1	D8
IO21NB0F1	B9
IO21PB0F1	B8
IO22NB0F2	A9
IO22PB0F2	A8
IO23NB0F2	B10
IO23PB0F2	A10
IO26NB0F2	A14
IO26PB0F2	A13

FG484	
AX1000 Function	Pin Number
IO29NB0F2	B12
IO29PB0F2	B11
IO30NB0F2/HCLKAN	E11
IO30PB0F2/HCLKAP	E10
IO31NB0F2/HCLKBN	D12
IO31PB0F2/HCLKBP	D11
Bank 1	
IO32NB1F3/HCLKCN	F13
IO32PB1F3/HCLKCP	F12
IO33NB1F3/HCLKDN	E14
IO33PB1F3/HCLKDP	E13
IO34NB1F3	C13
IO34PB1F3	C12
IO37NB1F3	B14
IO37PB1F3	B13
IO38NB1F3	A16
IO38PB1F3	A15
IO40NB1F3	C15
IO42NB1F4	A18
IO42PB1F4	A17
IO43NB1F4	B16
IO43PB1F4	B15
IO44NB1F4	B18
IO44PB1F4	B17
IO45NB1F4	B19
IO45PB1F4	A19
IO46NB1F4	C19
IO46PB1F4	C18
IO48NB1F4	F15
IO48PB1F4	F14
IO49NB1F4	D16
IO49PB1F4	D15
IO50NB1F4	C17
IO50PB1F4	C16
IO51NB1F4	E22

FG484	
AX1000 Function	Pin Number
IO51PB1F4	D22
IO52NB1F4	E16
IO52PB1F4	E15
IO57NB1F5	E21
IO57PB1F5	D21
IO60NB1F5	G16
IO60PB1F5	G15
IO61NB1F5	D18
IO61PB1F5	E17
IO63NB1F5	E20
IO63PB1F5	D20
Bank 2	
IO64NB2F6	F18
IO64PB2F6	F17
IO67NB2F6	F19
IO67PB2F6	E19
IO68NB2F6	J16
IO68PB2F6	H16
IO70NB2F6	J17
IO70PB2F6	H17
IO74NB2F7	J18
IO74PB2F7	H18
IO75NB2F7	G20
IO75PB2F7	F20
IO79NB2F7	H19
IO79PB2F7	G19
IO80NB2F7	L16
IO80PB2F7	K16
IO84NB2F7	L17
IO84PB2F7	K17
IO85NB2F8	G21
IO85PB2F8	F21
IO86NB2F8	G22
IO86PB2F8	F22
IO87NB2F8	J20

FG676	
AX500 Function	Pin Number
IO153PB7F14	M6
IO154NB7F14	K2
IO154PB7F14	L2
IO155NB7F14	K3
IO155PB7F14	L3
IO156NB7F14	L5
IO156PB7F14	L4
IO157NB7F14	L6
IO157PB7F14	L7
IO158NB7F15	J1
IO158PB7F15	K1
IO159NB7F15	J4
IO159PB7F15	K4
IO160NB7F15	H2
IO160PB7F15	J2
IO161NB7F15	K6
IO161PB7F15	K5
IO162NB7F15	H3
IO162PB7F15	J3
IO163NB7F15	G2
IO163PB7F15	G1
IO164NB7F15	G4
IO164PB7F15	H4
IO165NB7F15	F3
IO165PB7F15	G3
IO166NB7F15	E2
IO166PB7F15	F2
IO167NB7F15	F5
IO167PB7F15	G5
Dedicated I/O	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26

FG676	
AX500 Function	Pin Number
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10

FG676	
AX500 Function	Pin Number
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26

FG896	
AX1000 Function	**Pin Number**
IO51PB1F4	E21
IO52NB1F4	F22
IO52PB1F4	E22
IO53NB1F4	B25
IO53PB1F4	B24
IO54NB1F5	D24
IO54PB1F5	D23
IO55NB1F5	F23
IO55PB1F5	E23
IO56NB1F5	H21
IO56PB1F5	G21
IO57NB1F5	D25
IO57PB1F5	C25
IO58NB1F5	F24
IO58PB1F5	E24
IO59NB1F5	D26
IO59PB1F5	C26
IO60NB1F5	G23
IO60PB1F5	G22
IO61NB1F5	B27
IO61PB1F5	A27
IO62NB1F5	F25
IO62PB1F5	E25
IO63NB1F5	H23
IO63PB1F5	H22
Bank 2	
IO64NB2F6	K23
IO64PB2F6	J23
IO65NB2F6	J24
IO65PB2F6	H24
IO66NB2F6	H26
IO66PB2F6	H25
IO67NB2F6	G26
IO67PB2F6	G25
IO68NB2F6	K25

FG896	
AX1000 Function	**Pin Number**
IO68PB2F6	K24
IO69NB2F6	F27
IO69PB2F6	E27
IO70NB2F6	J26
IO70PB2F6	J25
IO71NB2F6	H27
IO71PB2F6	G27
IO72NB2F6	J28
IO72PB2F6	H28
IO73NB2F6	G28
IO73PB2F6	F28
IO74NB2F7	L23
IO74PB2F7	L24
IO75NB2F7	L26
IO75PB2F7	K26
IO76NB2F7	M25
IO76PB2F7	L25
IO77NB2F7	K27
IO77PB2F7	J27
IO78NB2F7	M27
IO78PB2F7	L27
IO79NB2F7	K30
IO79PB2F7	K29
IO80NB2F7	M23
IO80PB2F7	M24
IO81NB2F7	M28
IO81PB2F7	L28
IO82NB2F7	N26
IO82PB2F7	M26
IO83NB2F7	N25
IO83PB2F7	N24
IO84NB2F7	N22
IO84PB2F7	N23
IO85NB2F8	M29
IO85PB2F8	L29

FG896	
AX1000 Function	**Pin Number**
IO86NB2F8	N28
IO86PB2F8	N27
IO87NB2F8	P29
IO87PB2F8	P30
IO88NB2F8	P25
IO88PB2F8	P24
IO89NB2F8	P28
IO89PB2F8	P27
IO90NB2F8	P22
IO90PB2F8	P23
IO91NB2F8	R26
IO91PB2F8	P26
IO92NB2F8	R24
IO92PB2F8	R25
IO93NB2F8	R29
IO93PB2F8	R30
IO94NB2F8	R22
IO94PB2F8	R23
IO95NB2F8	T27
IO95PB2F8	R27
Bank 3	
IO96NB3F9	T29
IO96PB3F9	T30
IO97NB3F9	U29
IO97PB3F9	U30
IO98NB3F9	T22
IO98PB3F9	T23
IO99NB3F9	U26
IO99PB3F9	T26
IO100NB3F9	U24
IO100PB3F9	T24
IO101NB3F9	V28
IO101PB3F9	U28
IO102NB3F9	U23
IO102PB3F9	U22

FG896	
AX1000 Function	Pin Number
NC	K1
NC	K2
NC	L30
NC	M30
NC	N29
NC	T1
NC	U1
NC	W30
NC	Y1
NC	Y2
NC	Y30
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11

FG896	
AX1000 Function	Pin Number
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCCDA	AD24
VCCDA	AD7
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18

FG896	
AX1000 Function	Pin Number
VCCDA	AF19
VCCDA	C13
VCCDA	C5
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F26
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21

CG624	
AX2000 Function	Pin Number
IO229PB5F21	AD10
IO230NB5F21	V11
IO233NB5F21	AD7
IO233PB5F21	AD8
IO234NB5F21	V9
IO234PB5F21	V10
IO236NB5F22	AC9
IO238NB5F22	W8
IO238PB5F22	W9
IO239NB5F22	AE4
IO239PB5F22	AE5
IO240NB5F22	AB9
IO242NB5F22	AA9
IO242PB5F22	Y9
IO243NB5F22	AD5
IO243PB5F22	AD6
IO244NB5F22	U8
IO246NB5F23	AB8
IO246PB5F23	AC8
IO247NB5F23	AB7
IO247PB5F23	AC7
IO250NB5F23	AA8
IO250PB5F23	Y8
IO251NB5F23	V8
IO251PB5F23	V7
IO252NB5F23	Y7
IO252PB5F23	W7
IO253NB5F23	AC5
IO253PB5F23	AC6
IO254NB5F23	Y6
IO254PB5F23	W6
IO256NB5F23	AB6*

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO256PB5F23	AA6*
Bank 6	
IO257NB6F24	Y3
IO257PB6F24	AA3
IO258NB6F24	V3
IO258PB6F24	W3
IO259NB6F24	AA2
IO259PB6F24	AB2
IO260NB6F24	V6*
IO260PB6F24	W4*
IO262NB6F24	U4
IO262PB6F24	V4
IO263NB6F24	Y5
IO263PB6F24	W5
IO268NB6F25	U6
IO268PB6F25	U5
IO269PB6F25	U3
IO272NB6F25	T2
IO272PB6F25	U2
IO273NB6F25	W2
IO273PB6F25	Y2
IO274NB6F25	R6
IO274PB6F25	T6
IO275NB6F25	T7
IO275PB6F25	U7
IO277NB6F25	V2
IO278NB6F26	R4
IO278PB6F26	T4
IO279PB6F26	R3
IO280NB6F26	R5
IO281NB6F26	AA1
IO281PB6F26	AB1

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

CG624	
AX2000 Function	Pin Number
IO284NB6F26	R8
IO284PB6F26	T8
IO285NB6F26	W1
IO285PB6F26	Y1
IO286NB6F26	P2
IO286PB6F26	R2
IO287NB6F26	T1
IO287PB6F26	U1
IO288NB6F26	P5
IO290NB6F27	P6
IO291NB6F27	P1
IO291PB6F27	R1
IO292NB6F27	P7
IO292PB6F27	R7
IO293NB6F27	M1
IO293PB6F27	N1
IO294NB6F27	P8
IO296NB6F27	N3
IO296PB6F27	P3
IO298NB6F27	N4
IO298PB6F27	P4
IO299NB6F27	M2
IO299PB6F27	N2
Bank 7	
IO300NB7F28	P9*
IO300PB7F28	N6*
IO302NB7F28	M6
IO304NB7F28	N8
IO304PB7F28	N7
IO308NB7F28	M4
IO309NB7F28	L3
IO309PB7F28	M3

Note: *Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.